TM 11-5820-595-35

TECHNICAL MANUAL

DIRECT SUPPORT, GENERAL SUPPORT AND DEPOT MAINTENANCE MANUAL

RADIO SET
AN/GRC-143
(NSN 5820-00-926-7355)

This copy is a reprint which includes current pages from Changes 1 through 3. The title was changed by Change 2 as shown above.

HEADQUARTERS, DEPARTMENT OF THE ARMY

APRIL 1971

WARNING

ELECTROMAGNETIC

RADIATION

ELECTROMAGNETIC RADIATION HAZARDS EXIST AT THE WAVEGUIDE OUTPUT FROM THE POWER AMPLIFIER AND WITHIN THE DIRECTIONAL PATTERN OF THE ANTENNA! DO NOT STAND IN THE DIRECT PATH OF THE ANTENNA NOR WORK ON WAVEGUIDES WHILE POWER IS ON!

High frequency electromagnetic radiation can cause fatal burns. It can literally "cook" internal organs and flesh. If you feel the slightest warming effect while near this equipment MOVE AWAY QUICKLY !

WARNING

EXTREMELY HIGH VOLTAGE IN EXCESS OF 8,000 VOLTS IS PRESENT IN THE AMPLIFIER RADIO FREQUENCY AM-6090/GRC-143.

Disconnect power source and discharge capacitors before making any connections within the enclosed portion of the cabinet. DO NOT PLACE HANDS OR TOOLS NEAR TERMINALS CARRYING VOLTAGES ABOVE 500 VOLTS BECAUSE OF THE DANGER OF ARCING.

Technical Manual

No. 11-5820-595-35

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, *1 April 1971*

DIRECT SUPPORT, GENERAL SUPPORT AND DEPOT MAINTENANCE MANUAL RADIO SET ANIGRC-143 (NSN 5820-00-926-7355)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028 (Recommended Changes to Publications and Blank Forms) direct to: Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703.

In either case, a reply will be furnished direct to you.

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CHAPTER 1
FUNCTIONING OF EQUIPMENT
Section I. INTRODUCTION

1-1. Scope

a. This manual contains instructions covering direct support (chap. 2 through chap. 6) and depot (chap. 7) maintenance for Radio Set AN/GRC-143. It includes instructions for periodic checks and calibration, troubleshooting, testing, aligning, and repairing the equipment. It also lists tools, materials, and test equipment to perform the maintenance of the equipment. Operation and organizational maintenance are covered in TM 11-5820-59512.

b. Appendix A contains, a list of publications applicable to this manual. Appendix B lists the expendable supplies and materials applicable to the equipment.

1-1.1. Maintenance Forms, Records, and Reports.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.

b. Report of Packaging and Handling Deficiencies .ill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/DSAR4140.55; NAVSUPINST 4440.127E; AFR 400-54;MC04430.3E.

c. Discrepancy in Shipment Report IDISREP) (SF 361). Fill out and forward Discrepancy in 'Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/ NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-1.2. Destruction of Army Electronics Materiel

Demolition and destruction of electronic equipment will be under the direction of the commander and in accordance with TM 750-244-2.

1-1.3. Administrative Storage

Administrative storage instructions are provided in TM 740-90-1.

1-1.4. Reporting Equipment Improvement Recommendations (EIR)

If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703. We'll send you a reply.

Section II. OVERALL RADIO SET OPERATION

1-2. General

This section describes major functions of the radio set at the block diagram level. Functional signal paths through the radio set are described as they are implemented by the various units of the radio set. Functional relationships of the transmitter, receiver, and power amplifier are also described. Detailed descriptions and circuit analysis of the transmitter, receiver, power amplifier, and ancilliary equipment are covered in sections III, IV, and V respectively. The antenna alignment indicator is covered in section VI.

-3. Radio Set Block Diagram Description

The signal paths through the radio set and the functional relationships between the transmitter and power amplifier and between the transmitter and receiver are shown in figure 8-3. The major signal flow paths are indicated by bold lines on the diagram. Paragraph 1-4 describes the transmitting signal path and paragraph 1-5 describes the receiving signal path.

1-4. Transmitting Signal Path (fig. 8-3)

a. A combined pcm and order wire signal is applied to the *from* cable input of the transmitter. This combined signal is applied to the digital data modem 1A12 where the order wire signal is extracted from the pcm signal and applied to order wire assembly 1A13. The pcm signal is reshaped and retimed in the digital data modem for application to modulator 1A8 via pcm attenuator AF-RF amplifier 1A4, and 1.3-MHz low pass filter 1A6.

b. Order wire assembly 1A13 distributes the through order wire *(from* cable) voice signal to the receive circuits

of the local handset 4A4, Remote Telephone TA-312 / PT, and the order wire monitoring speaker on the transmitter meter panel. The transmit order wire signal and voice, frequencies from the microphone circuits of the local handset and remote telephone are amplified in the order wire assembly for application to modulator 1A8 via pcm attenuator 1A3, AF-RF amplifier 1A4, and 1.3-MHz low pass filter 1A6. The pcm and order wire signals are combined at the output of AF-RF amplifier 1A4 and applied to modulator 1A8 as a combined baseband signal. The combined baseband signal frequency modulates a 150-MHz carrier in modulator 1A8. Electronic Frequency control 1A7 stabilizes the center frequency of the 150 MHz carrier.

c. The 150-MHz fm output of modulator 1A8,is applied to frequency mixer 1A9 where it is translated to the 4.4to 5.0-GHz band. The local oscillator signal input (4.55 to 4.85 GHi) to frequency mixer 1A9 is provided by frequency synthesizer 1A14 and a times 16 frequency multiplier chain. The 4.4to 5.0-GHz frequency mixer carrier output is applied to the power amplifier cabinet interconnecting cable via filters 1FL3 and 1FL4 and directional coupler 1DC2. The transmitter output carrier level is 150 milliwatts.

d. The 150-milliwatt transmitter carrier is adjusted in the power amplifier to the required klystron drive level by variable attenuator 3A9AT1. The beam voltage for the klystron is provided by the high voltage power supply. Inverter regulator control module 3A1 regulates the beam voltage. The low RF-mismatch, alarm and control module 3A4, time-delay control module 3A5, and beam gate-dc overload control module 3A6 control application of the beam voltage to the klystron. The klystron produces a 1KW carrier output to the antenna via output directional coupler 3A9DC2, harmonic filter 3A9FLS, and the vaveguide switch.

e. A power amplifier summary alarm signal is sent from the power amplifier to the central alarm circuits in the transmitter orderwire assembly to provide a CNTRL ALARM indication when a power amplifier alarm condition occurs. Summary alarm signals from alarm monitor 1AS and digital data modem 1A12 in the transmitter unit and alarm monitor 2A20 in the receiver unit are also applied to this circuit to provide a CNTRL ALARM indication when an alarm condition occurs. Each unit (transmitter, receiver, and power amplifier) provides individual alarm circuits for detecting specific alarm conditions.

f. An interlock is provided between the transmitter and the waveguide switch. When the waveguide switch is being operated (between end positions), the supply voltage for amplifier frequency multiplier module 1A11 is removed causing transmitter excitation to be removed.

g. The output of the transmitter is also applied through directional coupler 1DC2 to the radio ter set. The radio test set provides test signals receiver channels A and B and is used for local testing of radio set operation.

1-5. Receiving Signal Path (fig. 8-3)

a. Two input signals (channel A and channel B) are applied to the receiver from the space diversity antennas through directional couplers 4A5 and 4A6. Each input channel receives identical traffic information, but not of the same instantaneous signal level. Both channels are tuned to the same frequency within the 4400-to 5000-MHz band and are separated by a minimum of 90 MHz from the transmitter frequency to permit duplex communication without cross-channel interference between the transmitter and receiver.

b. Each channel input signal is applied through a preselector (2FL4, 2FLS), TDA (2A1, 2A2), post selector (2FL6, 2FL7) and 4.4-to 5.0 GHz circulator (2HY1, 2HY2) to a mixer predmplifier (2A4, 2All), At the mixer preamplifier (2A4, 2A11), the 4.4to 5.0-GHz signal is mixed with a 4.33-t 5.07-GHz local oscillator signal from the locI oscillator filter (2FL8, 2FL9) producing a final output of 70 MHz which is applied to 70-MHz IF filter (2A5, 2A10).

c. The 4.33-to 5.07-GHz local oscillator signal from the local oscillator filter (2FL8, 2FL9) is developed in the frequency mixer) 2A6, 2A9) in the following manner. A 284to 303-MHz output signal from the frequency synthesizer (2A21) is applied to the amplifier multiplier (2A8) where it is multiplied four times producing an output of 1137 to 1213 MHz. The 1137-to 1213-MHz signal is then applied to the frequency multiplier group (2A7) through a 1137-to 1213-MHz bandpass filter (2FL10) and 1137-to 1213-MHz circulator (2HY3). At the frequency multiplier group (2A7) the 1137to 1213-MHz input signal is multiplied four times producing an output in band range of 4550 to 4850 MHz which is applied to frequency mixer which is applied to frequency mixer (2A6, 2A9). At the frequency mixer (2A6, 2A9) the 4550 to 4850-1M-Hz signal is mixed with a 220-MHz signal from 220 MHz vco (2A13, 2A14) producing a final locI oscillator output signal in the fluency rage of 4330 to 5070 MHz which is applied to local oscillator filter (2FL8, 2FL9).

d. The 70-MHz IF output from the 70-MHz IF filters (2A5, 2A10) is applied to the combiner 2A16 through IF amplifiers (2A12, 2A15). The combiner monitors the 70-MHz signals of both channels for demodulation. When the channel signal levels are within a predetermined level ratio with respect to each other, the channel signals are combined and applied to demodulator 2A17. When the predetermined ratio is exceeded, the combiner circuits inhibit the weaker signal and only the stronger signal is applied to the demodulator. Automatic gain control (age) signals are fed back from the combiner circuits to each channel's 70-MHz IF amplifier. Additional automatic gain control is provided by the age cross-connect between the IF amplifiers. Automatic phase control (apc) signals are fed back from the combiner to control the phase of the 220 MHz vco (2A13, 2A14) associated with each channel. An agc signal is also applied from combiner 2A16 to digital data modem 1A12 in the transmitter. This age signal is used to control the system clock timing correction circuits in the digital data modem. When the received signal is fading to a very weak level or is absent, the age will be correspondingly low. If the age signal level falls below a predetermined level, the system clock timing correction circuits are disabled until a satisfactory age level reappears.

e. Demodulator 2A17 extracts the pcm and order wire signals from the 70-MHz IF signal. The signal is applied through a low pass filter 2A18 and AF-RF amplifier 2A19 to digital data modem 1A12 in the transmitter unit. The digital data modem reshapes and retimes the pcm signal. The order wire signal is separated from the pem TM 11-5820-595-35 in the digital data modem 1A12 and is applied to order wire assembly 1A13 as the recovered order wire signal. Order wire assembly 1A13 amplifies and distributes the recovered order wire signal to the local handset 4A4, remote telephone TA-312/PT and a speaker mounted on the transmitter meter panel. In addition, order wire assembly 1A13 applies an order wire signal to digital data modem 1A12. The pcm and order wire signal appears at the to cable output of the transmitter for transmission through the cable and cable restorers (when required) to the terminal equipment.

f. Alarm monitor 2A20 receives monitor signals (traffic, channel A and B carrier IF, vco A and B lock and synthesizer) and controls the associated alarm indicators on the receiver meter panel. The alarm monitor also contains a summary alarm circuit which is enabled when any one of the alarm conditions occur. The traffic monitor signal is received from AF-RF amplifier 2A19 and indicates the composite pcm and order wire signal level at the output of the receiver. Channel A and B carrier IF alarm monitor signals are received from combiner 2A16 and indicate the condition of the channel A and the channel B 70-MHz IF carrier signals. The vco A and B lock alarm monitor signals are received from oscillator-multipliers 2A13 and 2A14 respectively and indicate if the 220-MHz signals from frequency multipliers 2A13A1 and 2A14Ai are frequency locked. The synthesizer alarm signal is received directly from frequency synthesizer 2A21 and indicates if the signals from variable frequency divider No. 2 (2A21A5) and standard RF oscillator 2A21A7 are phase-locked (para 1-27a(3).

Section III. FUNCTION OF TRANSMITTER

1-6. General

This section provides block diagram descriptions and circuit level theory for the transmitter. The areas covered are: block diagram description of major signal flow; block diagram descriptions of complex assemblies and modules; and,. circuit theory of the modules at the schematic diagram level.

1-7. Transmitter Block Diagram Description

a. The signal paths through the transmitter and the functional relationships of the transmitter modules are shown in figure 8-4. The major signal flow paths are indicated by bold lines on the diagram. The transmit signal path is shown from left to right, starting at the pcm and order wire input to digital data modem 1A12 and leaving from directional coupler 1DC2 as an RF output signal to the power amplifier. The receive signal path from the receiver is also shown. The pcm order wire input from the receiver is shown on the left entering digital data modem 1A12 and order wire assembly 1A13, and leaving the transmitter from digital data modem 1A12 as the pcm and order wire signal to terminal equipment. The order wire assembly provides order wire communication on a party line basis between the terminal

equipment, local handset, remote telephone, and remote radio station. Order wire communication is monitored by the speaker on the transmitter meter panel. The RING pushbutton on the meter panel provides in-band tone signaling to initiate communication with the remote order wire stations.

b. In the transmit signal path the combined pcm and order wire signal enters the transmitter at the *from* cable input and is applied to digital data modem 1A12. Under normal conditions, the CABLE TO RADIO MODEM indicator on the meter panel is lighted green. A red light indicates a failure in the cable to radio path of digital data modem 1A12. The *from* cable order wire signal is separated from the pcm signal in the digital data modem 1A12 and is applied to order wire assembly 1A13. The order wire signal is amplified and distributed to the order wire stations (local handset, remote telephone) and to pcm attenuator 1A3. The pcm signal is reshaped and retimed in digital data modem 1A12 and applied to pcm attenuator 1A3.

c. PCM attenuator 1A3 provides attenuation and phase shift circuits for the pcm signal and attenuation for the transmit order wire signal input. The signals are then combined at the output of AF-RF amplifier 1A4. A detected traffic level signal (representative of the input to modulator 1A8) is fed back from modulator 1A8 to alarm monitor 1A5 through pcm attenuator 1A3. The detected traffic level signal can also be monitored at the meter panel. PCM attenuator 1A3 also provides a detected order wire signal (order wire level) which can be monitored at the meter panel.

d. AF-RF amplifier 1A4 amplifies the pcm signal for application to modulator 1A8. As stated previously, the transmit order wire signal is combined with the amplified pcm signal at the output of AF-RF amplifier 1A4. The combined pcm and order wire baseband signal is applied to 1.3-MHz low pass filter 1A6 which, in conjunction with other filters in the transmitter, provides the necessary pcm pulse band shaping. The output of 1.3-MHz low pass filter 1A6 is applied to modulator 1A8 where it frequency modulates a 150-MHz carrier. Electronic frequency control module 1A7 provides automatic frequency control (afc) of the 150-MHz carrier. The frequency modulated 150MHz carrier output of modulator 1A8 is applied to frequency mixer 1A9 where it is mixed with a 4.55-to 4.85-GHz local oscillator signal to provide a 4.4-to 5.0-GHz carrier signal. Various signal levels are detected within the electronic frequency control, modulator, and frequency mixer and are: applied to the meter selector switch for monitoring at the transmitter meter panel.

e. The 4.55-to 4.85-GHz local oscillator signal is, produced by frequency synthesizer 1A14, amplifier-frequency multiplier 1All, and frequency multiplier group 1A10. The frequency synthesizer generates a highly stable frequency in the range of 284.375 to 303.125 MHz. The detected frequency synthesizer output level is applied to the meter selector switch and can be monitored at the transmitter meter panel. The SYNTHOVEN lamp on the meter panel lights white when the frequency synthesizer oven is at the correct temperature. The 284.375-to 303.125-MHz frequency synthesizer output signal is amplified and multiplied to 1137 to 1213 MHz by amplifier-frequency multiplier 1All. The +28v supply voltage to amplifier-frequency multiplier 1All is interlocked through contacts of interlock relay K1 (mounted in the transmitter cabinet). Relay K1 is normally deenergized allowing +28v supply voltage to be applied to the amplifier-frequency multiplier and causing the INTERLOCK indicator on the meter panel to light green. When the waveguide switch is being operated and is between end positions, relay K1 becomes energized removing the +28v supply voltage from the amplifier-frequency multiplier which disables the transmitter output and causes the INTERLOCK indicator to light red. Also, in event of a' malfunction, a synthesizer alarm signal is sent to alarm monitor 1A5.

f. The 1137 to 1213 MHz output of amplifier frequency multiplier 1A11 is applied through 1137-to 1213-MHz bandpass filter 1FL5 and 1137-to 1213-MHz circulator 1HY1 to frequency multiplier group lA10. The 1137-to 1213-MHz circulator provides isolation between the frequency multiplier circuits. Frequency multiplier group 1A10 multiples the 1137-to 1213-MHz signal to the 4.55-to 4.85-GHz local oscillator frequency for application to frequency mixer stage 1A9. The detected outputs of the frequency multiplier group (2ND MULT) and amplifier-frequency multiplier (AMP-MULT) are applied to the meter selector switch and can be monitored at the transmitter meter panel.

g. The 4.55-to 4.85-GHz signal is mixed with the 150-MHz frequency modulated signal (containing the pcm signal and order wire) in frequency mixer stage 1A9 to produce the 4.4-to

5.0-GHz carrier output signal which is applied to 4.4-to 5.0-GHz bandpass filter 1FL3. The filter has a bandpass of 38 MHz and can be tuned to the required transmitter carrier frequency. The lower band frequency (local oscillator minus 150 MHz) is selected for the low band carrier output frequencies of 4.4 to 4.7 GHz. The upper band frequency (local oscillator plus 150 MHz) is selected for the high band output frequencies of 4.7 to 5.0 GHz. The selected carrier frequency is passed through 5.0-GHz low pass filter 1FL4 to directional coupler 1DC2. The main output of the directional coupler is applied to the power amplifier. A secondary output is sent to the radio test set. In addition, detected forward and reflected RF power signals are sent to alarm monitor 1A5 and to the meter selector switch for monitoring at the meter panel.

h. The secondary output of the directional coupler 1DC2 is applied to crystal mixer 1Z1 in the radio test set. The 4.4-to 5.0-GHz transmitter output signal is mixed with the 100-MHz signal from 100-MHz RF oscillator 1A2 to provide the proper test signal frequency to the receiver. The test signal is applied to RF power divider 1DC1 which provides two test signals of equal power for application to receiver channels A and B. The channel A and channel B test signal levels can be independently adjusted by variable attenuators 1AT3 and 1AT4.

i. In the receive signal path through the transmitter a combined pcm signal and order wire signal from the receiver is applied to digital data modem 1A12 and order wire assembly 1A13. Under normal operating conditions, an energized relay in the order wire assembly prevents the combined pcm signal and order wire signal from entering order wire circuits, and the combined signal is applied to digital data modem 1A12. The digital data modem circuits separate the order wire signal from the pcm signal which will be reshaped and retimed. The recovered order wire signal is applied to the order wire circuits where it is amplified and distributed to the order wire stations (local handset and remote telephone) and as a through order wire signal applied back to the digital data modem. The through order wire signal is recombined with the pcm signal in the digital data modem circuits. The recombined pcm signal and order wire signal appears at the to cable output of the transmitter for transmission to the terminal equipment. Under normal conditions, the RADIO TO CABLE indicator on the meter panel is lighted green. The RADIO TO CABLE indicator lights red when a failure occurs in the radio to-cable path of the digital data modem.

j. When a pcm traffic failure occurs, the relay in the order wire assembly becomes deenergized which allows the combined pcm pulse train and order wire signal to be applied to the order wire circuits. The order wire portion of the signal is amplified and distributed to the local handset, remote telephone, and fed back through the digital data modem 1A12 to the terminal equipment by the to cable transmitter output. Thus, order wire communication is maintained if a pcm failure occurs.

k. Alarm monitor 1A5 receives alarm signals from a number of transmitter modules and circuits, and controls associated alarm indicators on the meter panel. Normal operating conditions cause the indicators to light green. An alarm condition causes the associated indicator lamp to light red. When any transmitter alarm conditions occur, the alarm monitor provides a transmitter summary alarm signal to central alarm circuits in order wire assembly 1A13. The central alarm circuits also receive a pcm summary alarm signal from digital data modem 1A12 and summary alarm signals from the receiver and the power amplifier. When a summary alarm occurs, the central alarm circuits in order wire assembly 1A13 cause the CNTRL ALARM indicator on the meter panel to light red and an audible alarm sounds at the meter panel speaker. Pressing the RESET pushbutton on the meter panel silences the alarm. Normal operating conditions cause the CNTRL ALARM indicator to be lighted green and the audible alarm to be silent.

1-8. Digital Data Interface

a. Digital data modem 1A12 interfaces the cable system and the radio set. In the radio receive direction (radio-to-cable), the digital data modem receives the combined pcm and order wire signal from the radio receiver and separates the pcm from the order wire signal. The pcm signal is processed by the digital data modem into a form which is compatible with the cable system. This is explained in c below. The recovered order wire signal is applied to order wire assembly 1A13 for further processing. Before applying the processed pcm signal to the cable, the digital data modem recombines it with the order wire signal from the order wire assembly. There is a continuous do current path between the cable input terminal of the digital data modem and the cable output ter

minal, so the output signal is comprised of pcm/ order wire/dc.

b. In the radio transmit direction (cable-to-radio), the digital data modem receives a combined pcm/order wire/dc signal from the cable system. The digital data modem separates the two signal components and loops the dc current back to the cable output terminal to complete the closed circuit dc current path. The extracted pcm signal is processed by the digital data modem into the form required for radio transmission. This is explained in c below. The *from* cable order wire signal is applied to order wire assembly 1A13 for further processing.

c. Radio Set AN/GRC-143 transmits and receives information in a pulse code modulation (pcm) system of 12 or 24 separate information channels. The signal is in the form of a serial stream of voltage pulses (bits) representing the pcm code and is divided into segments called frames. The pcm code bits are either logic one, represented by a positive voltage level, or logic zero, represented by a zero voltage level. The time allotted for each bit is referred to as baud. When a logic one bit is represented by the plus voltage level for the entire baud time, the signal is designated full-baud. If it is represented by the plus voltage level for only one half the baud time and the signal level is zero volts for the other half of baud time, the signal is designated one half baud. The frames are generated at the multiplexing equipment. The data codes generated during one scanning operation of the 12 channels being encoded in pcm comprise one frame. In a frame, the first six bits (voltage pulses, logic one or logic zero) are the pcm code for the information in channel 1; the next six bits are the pcm code for the information in channel 2, and so on for 12 channels. This gives a count of 72 bits for one frame. The pcm code for the last (12th) channel in a frame has only 5 bits because the 6th bit is used as an identifying bit to mark the end of the frame and it is called the sync bit. In the 12channel mode of operation, the bit rate is 576 kilobits per second, so one baud (bit) time is 1.736 microsecond and the time of one frame is 125 microseconds. In 24-channel mode, two separate 12-channel signals, designated PCM-1 and PCM-2, are combined into one signal. The bit rate for 24-channel mode is 1152 kilobits per second, therefore a baud is 868 nanoseconds. The 12channel and 24-channel bit rates just explained are used for radio transmission. The bit rate of the cable signal is always 2304 kilobits per second and the baud time is 434 nanoseconds. In the cable-to-radio direction of transmission, the signal received from the cable (waveform L, fig. 1-6) is at the cable bit rate and is converted to the applicable bit rate (12 or 24-channel rate) for radio transmission (see waveform N, fig. 1-e). In the radio-to-cable direction of transmission, the signal received from the radio (waveform N, fig. 1-13) is at the applicable bit rate (12- or 24-channel) and is converted to the cable rate (waveform M, fig. 1-13) for cable transmission. The radio signal is full-baud; the cable signal is one half baud.

d. The radio-to-cable and cable-to-radio interface functions of the digital data modem are described at the block diagram level in paragraphs 1-9 and 1-10. The individual printed wiring boards that comprise the digital data modem are described at the block diagram level' " paragraphs 1-11 through 1-21. The basic signal mnemonics used in the digital data modem block diagram descriptions are listed in the following chart. As used on the diagrams, and in the descriptions the mnemonics have a prefix 1 for logic one or 0 for logic zero to indicate the active logic state of the signal at that point. The mnemonics listed in the chart do not have the prefix 1 or 0, as the basic meaning of the mnemonic is the same for either prefix. Thus, 1RRIFAIL (output pin 10, fig. 8-30) means that logic one at this point indicates a radio receiver interface failure. 0RRIFAIL (output pin 7, fig. 8-28) means that logic zero at this point indicates a radio receiver interface failure. In addition, mnemonics for signals associated with PCM-1 or PCM-2 indicate which one is referred to by including either (1) or (2) in the mnemonic.

Mnemonic	Meaning
BP	Full baud data pulse
BPOW	Bypass order wire
CCEXOW	Cable extracted order wire
CCFAIL	Cable comparator failure
CCOWIN	Cable order wire in
CCROW	Cable receive order wire
CCTOW	Cable transmit order wire
CFFL	Cable-to-radio functional failure

Mnemonic	Meaning
CLPCM	Cable loopback pcm
CP	Clock pulse
CRFAIL	Cable regenerator failure
CRLFAIL	Cable-to-radio logic failure
CRPCM	Cable retimed pcm
CSPCM	Cable sliced pcm
CTFL	Cable-to-radio traffic failure
CVCOI	Cable voltage controlled oscillator modulation
DCSPCM	Cable sliced pcm data
DP	Data pulse
DMM	Dummy mismatches
DMF	Dummy match failure
DS	Dummy sample
F (1) FAIL	Frame circuit 4 kHz failure (PCM-1 PROCESSOR FAILURE
F(2)FAIL	Frame circuit 2 kHz failure (PCM-2 PROCESSOR FAILURE
FP	Phase pulse
FRCX	Pcm/order wire-de
FRCXOW	Order wire-de
FRPCM	Pcm/order wire
FRFAIL	From radio pcm failure
HALT	Halt timing
INHP	Inhibit phase-lock loop clock
LIM	Limit of mismatches
MARY	Major alarm summary
MM(1)	Match/mismatch PCM-1
MM(2)	Match/mismatch PCM-2
MMF	Mismatch flip-flop
MØ	Match frame output
MT(1)	Match time PCM-1
MT(2)	Match time PCM-2
M12C	12/24-Channel mode select
N2304	2304-kHz narrow clock
NØR	To cable signal normal
NP	Negative pulse
ØW	Order wire
ØW1	Order wire in
PP	Positive pulse
PLL	Phase-lock loop
PS	Pcm sample (1152 kHz for 24-channel operation and 576 kHz for 12-channel operation)
R576	576-kHz radio-to-cable clock
R1152	1152-kHz radio-to-cable clock
R2304	2304-kHz radio-to-cable clock
R4608	4608-kHz radio-to-cable clock
RAGC	Receiver age
RAGC-SW	Receiver age switched
RCFAIL	Radio comparator failure
RCVR FAIL	Radio receiver failure
REF(1)	4-kHz frame reference signal (PCM-1)
REF(2)	2-kHz frame reference signal (PCM-2)
RES	Reset
RFFL	Radio-to-cable functional failure
RPCM	Retimed pcm
REFAIL	Radio digital processor failure
RPFAIL	Radioaprocessor failure
RRIFAIL	Radio receiver interface failure
RROW	Radio recovered orderwire
RSPCM	Reshaped pcm
RTFL	Radio-to-cable traffic failure
RVCI	Radio voltage controlled oscillator modulation
SA	Squelch audio
SCLK	Square wave clock signal
SHC	Shift clock for finding frame

Mnemonic	Meaning
SL	Sync loss
SM	Search/sense mode
ST	Sync time
T288	288-kHz cable-to-radio clock
T576	576-kHz cable-to-radio clock
T1152	1152-kHz cable-to-radi6 clock
T2304	2304-kHz cable-to-radio clock
T4608	408-kHz cable-to-radio clock
TA through TL	Control processor timing signals
TEST	Not in cable-loopback-mode
T∅	CX To cable
TRPCM	To radio pcm
XCPCM	Cable traffic

1-9. Radio-to-Cable Interface Block Diagram Description (fig. 8-5)

a. The radio-to-cable interface circuits of the digital data modem provide processing of the pcm/order wire -signal input from the radio receiver. The radio-to-cable circuits separate the pcm signal and order wire signal. The recovered order wire is applied to order wire assembly 1A13 for further processing. After the pcm signal has been processed, it is recombined with the order wire signal (from order wire assembly 1A13) and the cable dc current and applied to the cable system.

b. Radio traffic consisting of the pcm/order wire signal is applied to radio digital regenerator 1A12A8 and to amplifier-detector 1A12A7. In radio digital regenerator 1A12A8, the pcm signal is separated from the order wire signal. The pcm signal which is distorted after radio transmission, is reshaped by generating square wave pulses under control of the input pcm signal. The reshaped pcm signal is applied to radio control comparator 1A12A9 and amplifier-detector 1A12A7. Radio control comparator 1A12A9 functions in conjunction with 4,608 kHz vco 1A12A14 to retime the pcm signal and to generate the signal voltage which controls the output frequency of 1A12A14. Amplifier-detector 1A12A7 uses the reshaped pcm signal (from 1A12A8) in conjunction with the pcm/order wire signal from the receiver to separate the radio order wire signal from the pcm component. The order wire signal is then applied to order wire assembly 1A13.

c. Radio control comparator 1A12A9 forms a phase-locked loop with 4,608 kHz vco 1A12A14. The 4,608 kHz voc generates the 4,608 kHz radio to-cable clock timing signal from which radio-to cable clock signals of 2304 kHz, 1152 kHz, and 576 kHz are generated. The radio-to-cable signals correspond to the cable (2304 kHz), 24 channel (1152 kHz), and 12 channel (576 kHz) data rates and are generated within radio control comparator 1A12A9. Depending upon the channel mode (12 or 24) at which the radio set is operating, the corresponding radio-to-cable clock signal (1152 kHz or 576 kHz) is compared with the reshaped pcm signal input from radio digital regenerator 1lA12A8. If a phase difference between the two: signals is detected, radio control comparator 1A12A9 applies a correction voltage (radio vco modulation) to 4,680 kHz vco 1A12A14 which responds by changing the radio-to-cable clock frequency (4,608 kHz) output in such a manner as to correct the phase difference between the clock signal (derived from the 4,608 kHz vco) and the reshaped pcm signal. The radio-to-cable clock signal and the reshaped pcm signal are, therefore, phase-locked when the voltage to the vco is correct.

d. The 4,608-kHz radio-to-cable clock signal is used within radio control comparator 1A12A9 to retime the reshaped pcm signal so that its output is full-baud. The retimed pcm signal is then applied to control processors 1A12A10 and 1A12A12 for processing of the frame sync data. The retimed pcm signal is also applied to radio digital processor 1A12A13 where it is reformatted for cable system compatibility (para 1-8c). Radio control comparator 1A12A9 also applies the squarewave clock signals, developed from the 4,608-kHz radio-to-cable clock signal, to the control processors 1A12.10 and 1A12A12 and radio digital processor 1A12A8. In addition, radio control comparator 1A12A9 applies the square wave clock to radio digital regenerator 1A12A8.

e. The square wave clock is used in radio digital regenerator 1A12A8 in conjunction with the receiver agc input from the receiver. If the receiver age input indicates that the receiver signal-to-noise ratio is low (which can be caused by a temporary radio fade), radio digital regenerator 1A12A8 applies an inhibit phase-lock loop clock signal to radio control comparator 1A12A9. The inhibit signal disables the radio control comparator phase comparison function and thus prevents any change in the correction voltage. Receiver traffic therefore is processed even though the signal-to-noise ratio is low (as indicated by the receiver agc input), however, the internal timing correction circuits within the digital data modem are not activated. As a result, a certain amount of faulty pcm data is possible, but this condition is tolerated in an attempt to maintain communication with the cable system.

f. Control processors 1A12A10 and 1A12A12 are identical circuits that function in conjunction with pulse decoder 1A12All (which contains two identical framing control circuits, one associated with each control processor). Each processor receives the retimed pcm full-baud signal from radio control comparator 1A12A9 as well as the square wave clock. In addition, the control processors receive pcm sync search/sense and pcm sync loss control inputs from the associated framing control circuit of pulse decoder 1A12A11. The control processors determine the location of the sync bit in the pcm signal. In the 24-channel mode, 1A12A10 locates the sync bit of PCM-1 and 1A12A12 locates the sync bit of PCM-2. In 12channel mode, 1A12A10 locates the sync bit of the pcm signal and 1A12A12 is not used. The output data of the control processors is analyzed by pulse decoder 1A12A11 to determine whether the sync bit has been located. If it has not been located, 1A12A11 supplies signals to the control processors that enable them to operate in search mode. When the sync bit is tentatively located, 1A12A11 holds the control processors in an in-between mode designated sense mode. When location of the sync bit is confirmed, 1A12A11 allows the control processors to operate in normal mode. The purpose of locating the sync bit is to eliminate error bits that occur at sync bit time. This is important because the individual channels are identified by counting from sync time at the demultiplexing station in the transmission system. When the sync time has been located, the control processors send a frame sync time signal to radio digital processor 1A12A13. This signal enables 1A12A13 to substitute a correct sync bit in the pcm signal in place of the original sync bit and thus assures the reliability of the sync bit.

g. Radio digital processor 1A12A13 provides final processing of the pcm signal prior to application to the cable system. It performs the following functions:

(1) It passes the pcm signal if it is present. It substitutes signal 0R288 (288 kHz) for the pcm signal when there is a pcm signal failure.

(2) It substitutes an error-free sync bit in place of the pcm sync bit when the control processors are in normal mode. It passes the original pcm sync bit unchanged when the control processors are in sense or search mode.

(3) In 12-channel mode, it converts the 12channel pcm signal to 24-channel bit rate.

(4) It converts the 24-channel rate to cable rate and retimes the signal.

(5) It amplifies the pcm signal and combines it with the order wire signal.

(6) It provides cable simulation networks to equalize the signal for various cable lengths.

(7) It provides the cable loopback capability. This is a cable test arrangement which connects the processed cable-to-radio pcm signal (output of cable digital processor 1A12A4) to the input of 1A12A13. When the radio set is placed in the test mode, the input pcm signal (from cable signal) is fed back through 1A12A13 and returned to the source (to cable signal).

h. The digital data modem radio-to-cable circuits also include an alarm monitoring capability. Radio-to-cable fault conditions are detected in radio digital. regenerator 1A12A8, radio control comparator 1A12A9, control processors 1A12A10 and 1A12A12, and radio digital processor 1A12A13. The detected fault signals are applied then to alarm monitor 1A12A6. The alarm monitor generates applicable fault alarm signals that control digital data modem and transmitter fault indicators. Alarm monitor 1A12A6 also generates an alarm summary (which can also be generated for cable-to-radio faults) for control of a radio set shelter summary alarm. When a radio pcm failure is detected, alarm monitor 1A12A6 applies an alarm signal to radio digital processor 1A12A13 which responds by substituting a constant pattern timing signal for the pcm output to the cable (g(l) above). The alarm signal is also applied to the order wire circuit and causes it to use the radio receiver signal (which under this alarm condition contains only order wire) directly,

bypassing the radio order wire amplifier detector 1A12A7.

1-10. Cable-to-Radio Interface Block Diagram Description
(fig. 1-1)

a. The cable-to-radio interface circuits of the digital data modem provide processing of the pcm/order wire/dc signal received from the cable system. The pcm and order wire signals are separated for individual processing. The order wire signal is applied to order wire assembly 1A13. The pcm signal is processed in the digital data modem. Upon completion of processing, the pcm and order wire (from 1A13) signals are recombined and applied to the transmitter.

b. The pcm/order wire/dc signal is applied to cable digital regenerator 1A12A2 which separates the signals. The pcm signal is reshaped into a digital form (A and B, fig. 1-3) and applied to cable control comparator 1A12A3 as the cable sliced pcm signal. The order wire/dc signal is applied to transformer 1A12A15A1T1. The order wire signal is coupled to the transformer secondary and applied to AF amplifier 1A12A5. The dc current path is maintained through the primary of the transformer and other digital data modem components for subsequent return to the cable system. The cable extracted order wire signal is amplified by AF amplifier 1A12A5 and applied to order wire assembly 1A13.

c. Cable control comparator 1A12A3 functions in conjunction with 4,608 kHz vco 1A12A1 to develop a system data timing signal for internal use and for use in cable digital processor 1A12A4. Cable control comparator 1A12A3 compares the phase of the cable sliced pcm input (which is at the cable rate of 2304 kilobits/second) with the phase of a 2304-kHz timing signal developed from the 4608-kHz cable-to-radio clock input from 4,608 kHz vco 1A12A1. If the pcm signal and the 2304kHz timing signal are not in phase, cable control comparator 1A12A3 generates a correction voltage (cable vco modulation) that is applied to 1A12A1 and causes it to change the frequency (4608 kHz) output such that the phase of the 2304-kHz timing signal coincides with the phase of the pcm data. Thus, cable control comparator 1A12A3 and 1A12A1 form a phase-locked loop that phase-locks the 2304-kHz clock output of cable control comparator 1A12A3 to the pcm data. The cable sliced pcm and the phase-locked 2304kHz timing signals are applied to cable digital processor 1A12A4 for retiming of the pcm pulse train.

d. Cable digital processor 1A12A4 retimes the half-baud, cable bit rate pcm signal (fig. 1-6, waveform L) into a full-baud signal (fig. 1-6, waveform N) at a rate equal to the mode of operation (12 or 24 channel) of the radio set. Using the 2304-kHz clock input, cable digital processor 1A12A4 derives the timing signals used in reformatting and retiming the pcm signal. The reformatted and retimed pcm output (to radio) of cable digital processor 1A12A4 is applied to the transmitter for combining with the order wire signal and subsequent radio transmission.

e. Cable digital processor 1A12A4 also includes a cable loopback function. When the test enable input is present, cable digital processor 1A12A4 applies the cable sliced pcm signal input (which is received by cable digital regenerator 1A12A2 from the cable system) to the radio-to-cable digital data modem circuits as a cable loopback pcm signal. The radio-to-cable circuits loop the pcm signal back to the cable system for system maintenance purposes.

f. The digital data modem cable-to-radio circuits also include an alarm monitoring capability. Cable-to-radio fault conditions are detected in cable digital regenerator 1A12A2, cable control comparator 1A12A3, and cable digital processor 1A12A4 and applied to alarm monitor 1A12A6. Alarm monitor 1A12A6 generates applicable fault alarm signals that control digital data modem and transmitter fault indicators. Alarm monitor 1A12A6 also generates an alarm summary (which can also be generated for radio-to-cable faults) which is sent to the radio set shelter summary alarm.

1-11. Cable Digital Regenerator 1A12A2 Block Diagram Description
(figs. 1-2 and 8-24)

a. The input signal to cable digital regenerator 1A12A2 is designated FRCX (pcm/order wire/ dc). Since the length of cable through which the signal is transmitted may vary up to a maximum of 1 mile, a cable simulation network, variable in increments which provide attenuation equivalent to 1/4 mile of cable, is provided to terminate the line. This consists of three 1/4-mile sections which can be selected by the operator. The section or sections selected modify the input signals to an equivalent that would be delivered by 1 mile of cable.

b. The original FRCX signal from the source end of the cable is comprised of a dc signal plus squared voltage pulses representing the one bits in the pcm modulation code. When the order wire circuit is in use, the order wire audio signal is the third component of the FRCX signal. This signal, at the input to 1A12A2, is greatly degraded in quality after transmission through 1 mile of cable (or equivalent). A typical input FRCX signal is illustrated in figure 1-3, waveform A.

c. When the FRCX signal is coupled to 1A12A2, the dc is blocked from this path by capacitor C1 and the order wire is rejected by high pass filter C1/L7. The pcm portion of the input signal is coupled to the cable simulation networks and transformer T1. Transformer T1 provides a voltage gain of two. Overvoltage protection for following amplifiers is provided by diodes CR1-CR4 which limit the maximum amplitude of the input signal. The order wire and dc signals go through low pass filter L1, L2: and L3 and are sent to chassis mounted transformer lA12A15AlTl as the FRCX0W signal.

d. The pcm signal at the secondary of transformer T1 is degraded because of high frequency losses during cable transmission. The pcm voltage pulses are no longer clearly defined and square and are low in amplitude. Circuit Q1, of the 2304kHz peaking circuit, amplifies the pcm voltage pulses to provide a more sharply defined signal. Circuit Q1 is tuned to 2304 kHz which is the frequency used to time pcm voltage pulses for cable transmission. Circuit Q2, with a voltage gain of 35, then greatly increases the sharpness and definition of the pcm voltage pulses. The output of circuit Q2 is coupled through impedance matching emitter follower Q3 and transformer T2 to amplifier Q5A. Amplifier Q5A is a temperature compensated linear amplifier which further amplifies the signal. Peak detector circuit Q7/Q8 rectifies the pcm signal output of amplifier Q5A and develops a filtered positive dc voltage across R40. The center arm of R40 is connected to the reference input of slicer A1. The pcm signal from Q5A also is connected to the other input of slicer A1. Slicer A1 is a high speed differential comparator. It produces a pulse output with a steep vertical rise for positive voltage transitions of the input and a sharp vertical drop for negative transitions. Thus, the pcm is sliced into separate voltage pulses, logic ones, which represent the logic one bits in the pcm code as shown in figure 1-3, waveform B. The output of slicer Al is zero for logic zero bits. The dc voltage developed by peak detector Q7/Q8 assures that the center of each voltage pulse corresponds to the peak of the pcm signal. The pcm signal, now designated 1CSPCM, is sent to cable control comparator 1A12A3 for retiming.

e. In addition, the 1CSPCM signal is integrated by Q9 which develops a dc output signal as long as logic one bits keep occurring at the input. Lamp driver Q10 then provides a ground output and lamp DS1 lights to indicate traffic activity. In the absence of traffic, lamp DS1 does not light and a signal, designated 1CRFAIL, is sent to alarm monitor 1A12A6.

1-12. Cable Control Comparator 1A12A3 Block Diagram Description
(figs. 1-4 and 8-25)

a. The function of cable control comparator 1A12A3 is to determine the phase difference between the clock and data signals and from this information to generate a control signal. The control signal is then used to shift the phase of the clock signal until data and clock are in phase. Cable control comparator 1A12A3 receives the 1T4608 signal (4608-kHz cable-to-radio clock) from 4608 kHz vco 1A12..A and the 1CSPCM signal (cable sliced pcm) from cable digital regenerator 1A12A2. The 1CSPCM signal is inverted by inverter A3B. The inverted signal (OCSPCM) is sent to cable digital processor 1A12A4 and is also connected to the trigger input of flip-flop A7B which divides the signal by two. The output of A7B is connected to both inputs of and gate A1B, directly to pin 6 and through delay inverters A11C, D and A to pin 5 (E24). Because of the propagation delay through the three inverters, the input signals to A11B are simultaneously logic one only for a short time immediately following a positive transition at the output of flip-flop A7B (1DP waveform, fig. 8-25). The resulting logic zero output of A11B sets phase comparator A10A and B. Tracing this action back to the input signal (1CSPCM), it can be seen that it occurs at the positive-going or leading edge of a data logic one. Generation of the reset pulse for the phase comparator is discussed in b below.

b. Input signal 1T4608 (4608-kHz cable-to-radio clock) is divided by two by flip-flop A7A. The logic one output of A7A is designated 1T2304 (2304kHz cable-to-radio clock) and is sent to cable digital processor 1A12A4. The logic zero output of A7A is connected to the trigger input of strobe clock generator A5 which is a monostable multivibrator.

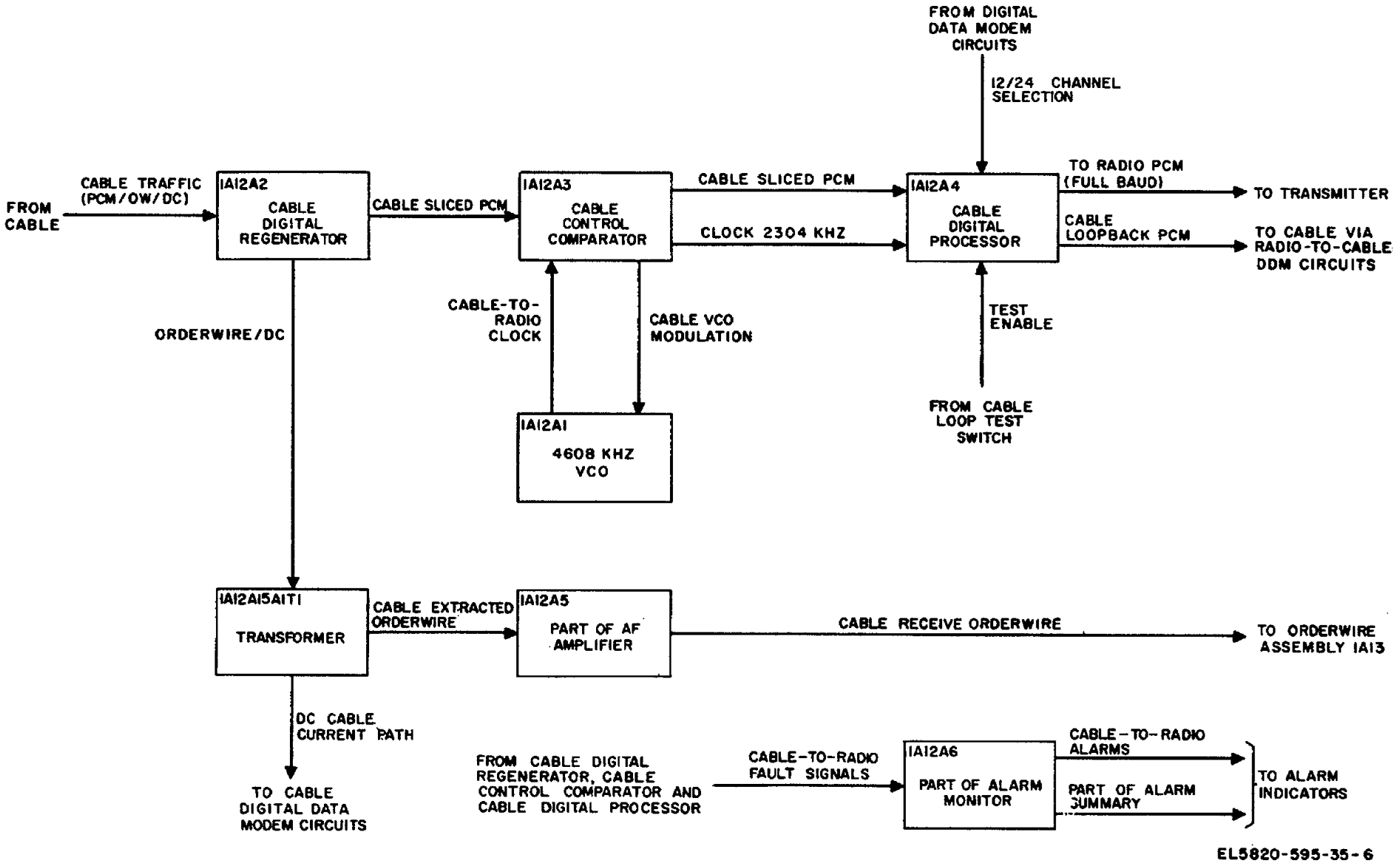


Figure 1-1. Digital data modem 1A12, cable-to-radio functional block diagram

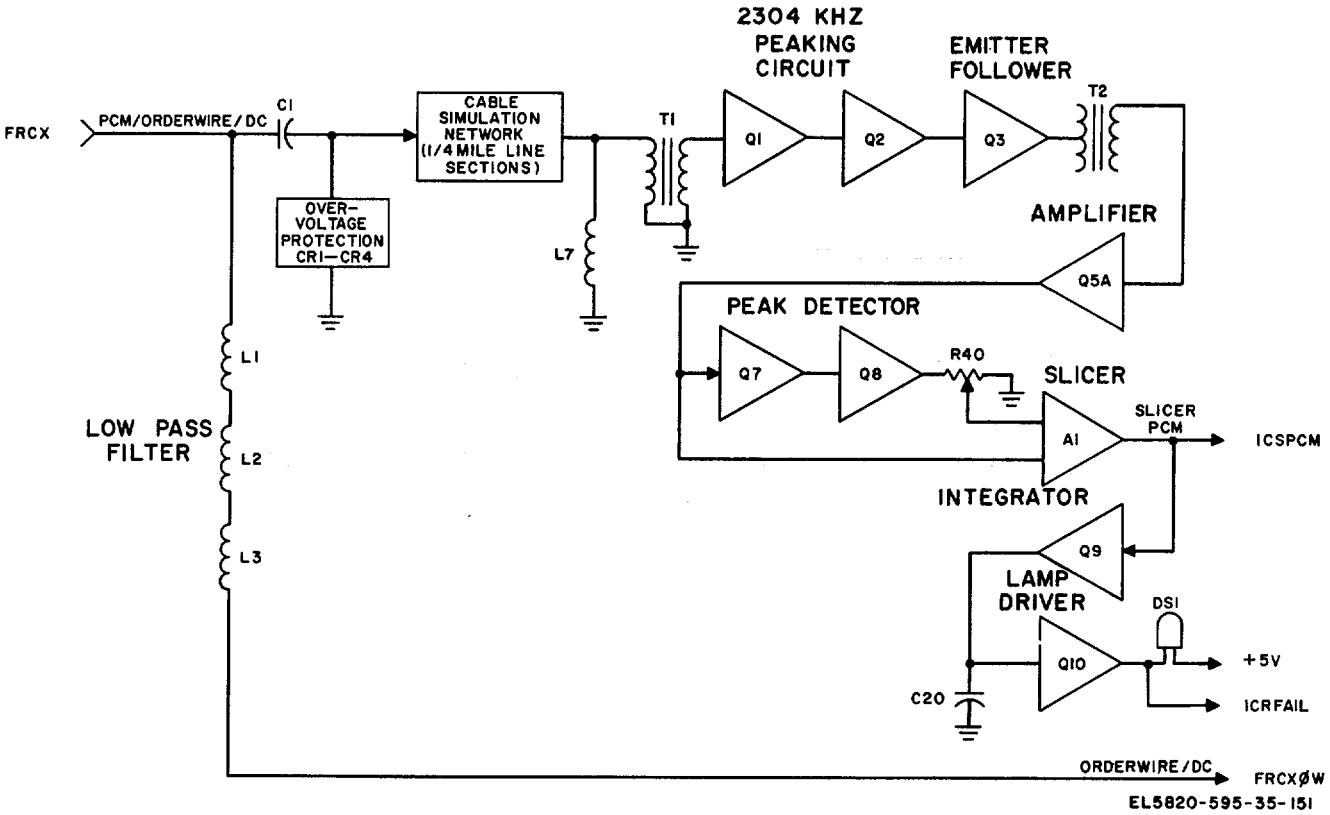


Figure 1-2. Cable digital regenerator 1A12A2, block diagram.

It generates a negative 120-nanosecond output pulse for each input pulse. This signal is inverted by inverter A3A and designated 1N2304 (2304-kHz narrow clock). It is sent to cable digital processor 1A12A4 and is also connected to inverter A3D. The output of A3D is connected to both inputs of and gate A2B, directly to pin 6 and through delay inverters A2C, D and A to pin 5. Because of the propagation delay through the three inverters, the input signals to A2B are simultaneously logic one only for a short time immediately following a negative transition at the output of A3D (1CP waveform, fig. 8-25). The resulting logic zero output of A2B resets phase comparator A10A and B. Tracing this action back to the input signal (1T4608), it can be seen that it occurs at the positive-going or leading edge of clock pulses. The difference in time between set (iDP, data pulse) and reset (lCP, ·clock pulse) pulses to the phase comparator is then a measure of the phase difference between the data input, 1CSPCM and clock input, 1T4608.

c. The output (E24) of the delay circuit in the data pulse generator (a above) is also connected to 48-channel baud generator Al which is a monostable multivibrator. It generates a negative pulse each time the input signal goes to logic zero. The duration of the negative pulse is adjusted so that the total time from the start of 1DP to the end of the baud pulse is 434 nanoseconds. This signal is inverted by inverter A3C and applied as one input (1BP) to AND gate A6A (1BP waveform, fig. 8-25).

d. The output signal of the phase comparator (1FP) (1FP waveforms, fig. 8-25), which represents the phase difference between data and clock signals, is inverted by inverter ACB. The output signal of inverter A6B (1PP waveform, fig. 8-25) through the positive pulse generator generates the positive pulse input to differential integrator A8. The inverted output of the 48-channel baud generator (1BP) with 1FP causes AND gate A6A to provide an output signal (1NP waveform, fig. 8-25) through the negative pulse generator, which generates the negative pulse input to differential integrator A8. Thus, at the start of each data pulse (corresponding to a logic one bit in the data signal) 1DP goes negative, 1FP goes negative and 1PP goes positive. This condition holds and a positive pulse input to the integrator is generated until 1CP goes negative. When 1CP goes negative, 1FP goes positive and since 1BP is

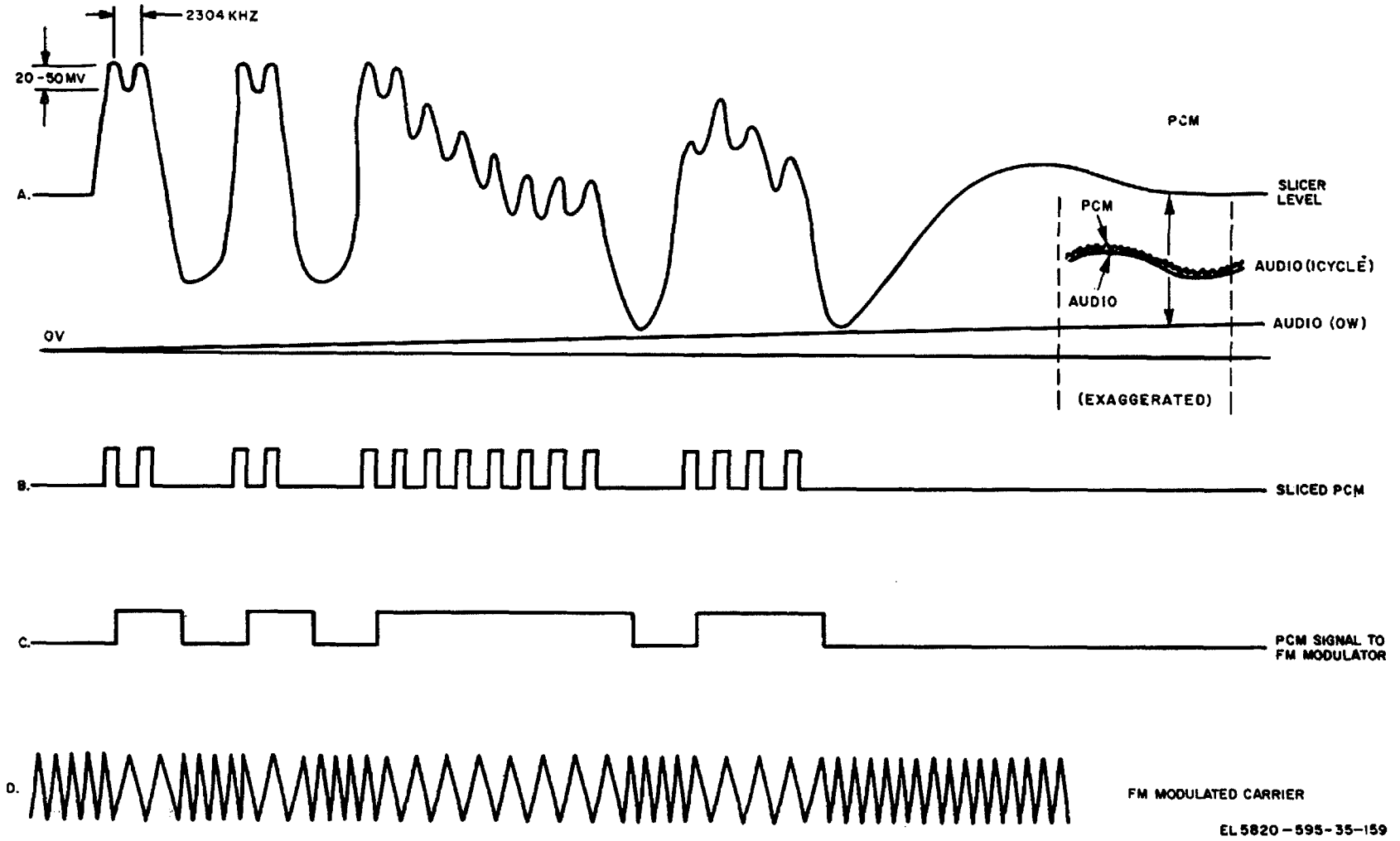


Figure 1-3. Cable digital renegenerator 1A12A2, timing diagram

positive, 1NP goes negative. This condition holds and a negative pulse input to the integrator is generated until 1BP goes negative. When zero bits occur in the input signal (1CSPCM), 1DP remains high and the phase comparator flip-flop is not set, so 1FP remains high. Thus, 1PP remains low and positive pulses to the integrator are not generated. Also 1BP remains low, so 1NP is high and negative pulses to the integrator are not generated.

e. The output signal of differential integrator A8 is connected to the frequency control input of 4608 kHz vco 1A12A1. When the input to A8 is a positive pulse, the output is a negative-going change in voltage. When the input is a negative pulse, the output is a positive-going change in voltage. This means that the output voltage starts to rise (or fall) at a fixed rate of change (slope). When clock and data are in synchronism, positive and negative pulse inputs to A8 are approximately equal, and the positive-and negative-going changes in output voltage cancel since the slopes are equal. These low amplitude excursions of the output signal are filtered at the input of 1A12A1 and the output frequency remains constant. When the positive pulse inputs to A8 are longer than the negative pulses, the negative-going output caused by the positive pulse is not entirely canceled by the return in the zero direction caused by the following negative pulse. The net result is that the signal remains negative and will go more negative as long as this condition (longer positive pulses) holds. However, the negative output signal causes the frequency of 1A12A1 to increase, clock pulse 1CP then occurs sooner and positive pulses are shortened and the length of negative pulses is increased. This action and reaction occurs until positive and negative pulses are equal. When the negative pulses are longer than positive pulses, the same kind of action in the opposite direction takes place. The output of A8 goes positive, clock frequency is decreased and clock pulse 1CP is delayed. This shortens the negative pulses. The result is that the output of A8 always produces a frequency change at 1A12A1 that tends to equalize positive and negative pulses and when equality is established to maintain it. When the data signal has logic zero bits, neither positive nor negative pulses are sent to integrator A8, however, it has a long time constant which holds its output to bridge over these short intervals.

f. The output of differential integrator A8 is also connected to positive/negative clamp detector A9. Normally, the output of differential integrator A8 will be close to zero volt as it holds the clock signal in synchronism with data. However, when correction is required, the output of A8 can vary from -F3 volts to -3 volts. Positive/negative clamp detector A9 detects output signals of A8 that exceed the indicated limits. When either limit is exceeded its output goes high. This signal, inverted twice by the lamp driver, is sent to alarm monitor 1A12A6 and also turns off lamp DS1.

1-13. Cable Digital Processor 1A12A4 Block Diagram Description

(figs. 1-5 and 8-26)

a. The OCSPCM signal input to data delay A4 is the signal received from the cable and reshaped by cable digital regenerator 1A12A2 (para 1-11) and inverted by cable control comparator 1A12A3 (para 1-12). The output signal from data delay A4 is inverted by inverter A6A which provides one input signal to and gate A5B. Another input to A5B is 1N2304 (2304-kHz narrow clock) which consists of 120 nanosecond positive pulses at 2304 kHz and coincides with 1T2304 (2304-kHz cable to-radio clock). These two inputs to A5B go to logic one at the same time (whenever a data one occurs) because clock/data synchronism was established in cable control comparator 1A12A3. The third input (0 TEST from pin 2) to A5B is logic zero, so the output is logic one, when cable loop test switch 1A12A15A1S1 is in normal position. When this switch is in test position, the 0 TEST input to A5B is logic one and data bits are gated through at clock time. Data one bits which are 434 nanoseconds in duration at the input are shortened to 120 nanoseconds at the output. The output signal 0CLPCM (cable loopback pcm) is sent to radio digital processor 1A12A13. See paragraph 1-21 for a discussion of cable loop-back function.

b. The signal at the trigger input of flip-flop A7A is 1T2304. A7A divides by two and its logic zero output, designated OT1152, is connected to NAND gates A3A, A3B and A5C and also to flipflop A2A. The logic one output of A7A is connected to NAND gate A8B. The signal at pin 6 of A8B is normally logic one (see g, below, for explanation of logic zero input at pin 6) so the 1152-kHz signal is inverted by A8B and inverted again by A8A. The 1152-kHz signal is divided by two by flip-flop A7B and its outputs are designated 1T576 and 0T576. 1T576 is connected to NAND gates A3A and A5C; output 0T576 is connected to NAND gates A3A and A5C; output 0T576 is connected to NAND gate A3B and to flip-flop

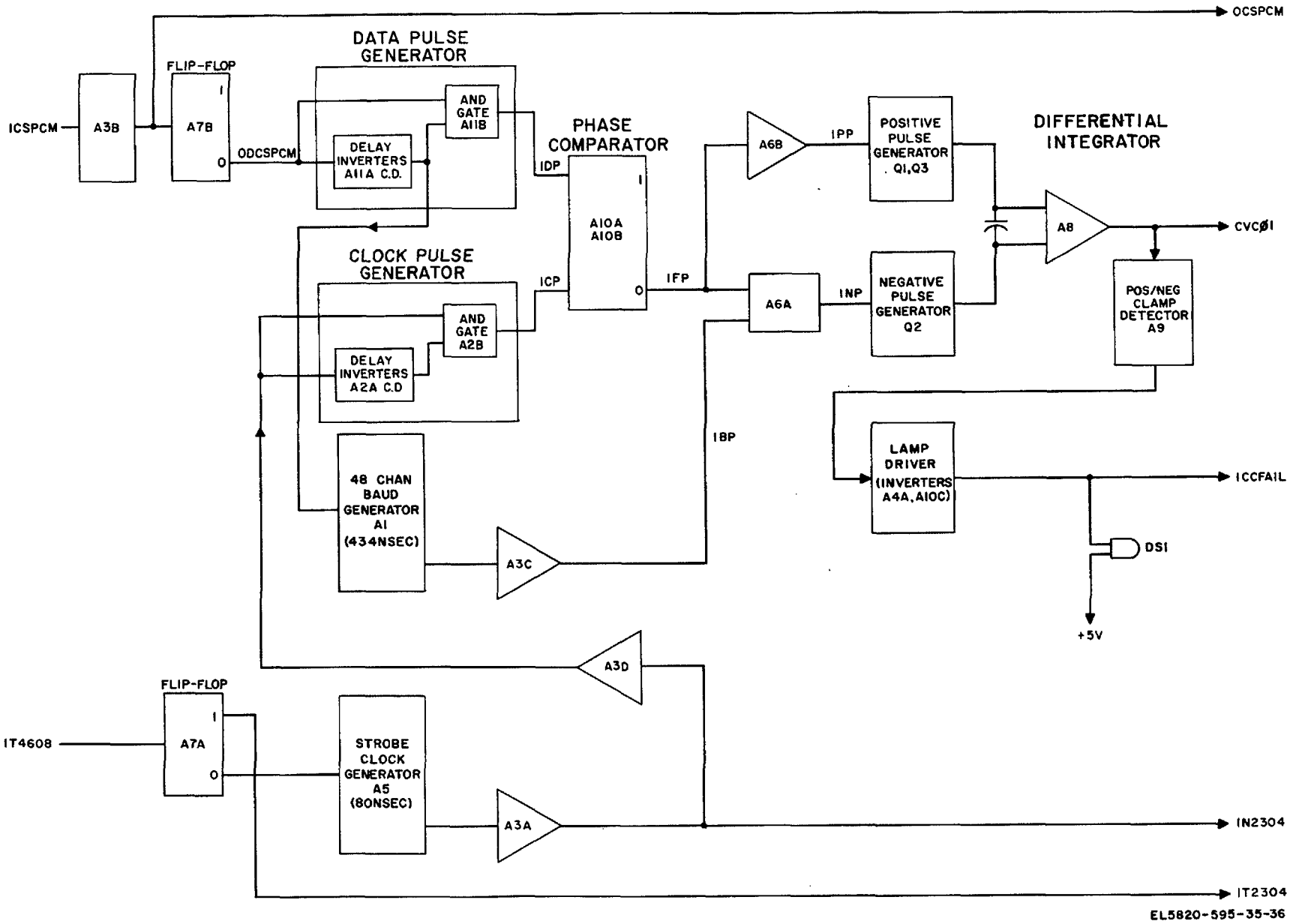


Figure 1-4. Cable control comparator 1A12A3 block diagram.

A2B. Flip-flop A2B divides by two and its outputs are designated 1T288 and 0T288. Note that all these clock signals are in synchronism because they are derived by successively dividing 1T2304 by two. Waveforms for the clocks are shown in figure 1-6, waveforms A through E.

c. The output of data delay A4 is inverted by inverter A6B and becomes 1CSPCM. It is connected to the D (data) input of data retimer flip-flop A10A. When the trigger (E16) input of A10A goes positive the output at pin 5 goes to logic one if D is at logic one and to logic zero if D is at logic zero. The signal at pin 6 is always the complement of the signal at pin 5. The signal at the trigger input of A1OA is determined by A3A, A3B and A8D. When the traffic select switch 1A12A15AlS2 is in the 12-channel position, the signal at pin 1 of A3A is logic zero and A3A is inoperative. NAND gate A3B has clock signals connected at all inputs; 0T1152 at pin 5, 0T576 at pins 6 and 9, and 1N2304 (narrow clock) at pin 7. When these three clock signals are simultaneously logic one (positive), the output of A3B goes to logic zero for 120 nanoseconds. But this occurs only once every fourth narrow clock pulse, at intervals of 1.736 μsec or a clock rate of 576 kHz. This is the data rate for 12-channel mode of operation. The 120 nanosecond negative pulse output of A3B is inverted by A8D (fig. 1-6, waveform J) and triggers A10A. Thus A10A is triggered at a 576kHz rate in synchronism with the data time because clock and data have been synchronized (para 1-12). Each time A10A is triggered, its output (pin 6) goes to logic 0 if D is at logic 1. If D is at logic 1 for several successive clock pulses, the output remains' at zero. When D goes to logic zero, the clock pulse switches the output to logic 1. In effect the one half baud data at the input of A10A (waveform L) is converted to full-baud at the output. This signal is inverted by level converter A11A and the retimed data, designated 1TRPCM, is sent to the radio modulation circuits. The waveform is illustrated in figures 1-3 and 1-6, waveform N.

d. When traffic select switch 1A12A15A1S2 is in the 24-channel position, the signal at pin 1 of A3A is logic one. The other three inputs are the same as the inputs to A3B except that the opposite phase of the 576-kHz signal is used at A3A (1T576 at pin 2). The output of A3A is the same as that of A3B (narrow clock pulses at a clock rate of 576 kHz) but because of the difference in phase of 1T576, these pulses (waveform F, fig. 1-6) are located exactly halfway between the pulses from A3B. Since the outputs of A3A and A3B pass. through OR gate A8D, the clock rate at the trigger input of A10A is now twice what it was for the 12-channel mode of operation. Compare waveforms Hand J. A10A is now triggered at 1152 kHz, which is the 24-channel rate. Data retiming in A10A is the same as explained (c above) for 12-channel rate, with clock and data rate both doubled.

e. The pcm input signal to data retimer flip-flop A10A (1CSPCM) is always at the cable bit rate, 2304 kilobits per second. For 24-channel mode, each logic one in the pcm-coded channel information is represented by two successive half-baud logic ones in the cable sliced pcm signal (CSPCM). For 12-channel mode, each logic one in the pcm-coded channel information is also represented by two successive half-baud logic ones, however, this leaves one-half of the cable rate signal time unused. To maintain the cable bit rate, dummy pulses are inserted in the 12-channel pcm signal at the source. The dummy pulses are alternate pairs of logic ones and logic zeros (waveform L, fig. 1-6) inserted between the pcm pairs. The waveform of the 24-channel signal is the same as that of the 12-channel, with PCM-1 for the 12channel pcm and PCM-2 in place of the dummy pulses. Only every fourth pcm bit is passed through data retimer flip-flop A10A in the 12channel mode (c above) and only every other bit is passed in the 24-channel mode (d above). Since the signal is to be converted to full-baud at the 24-channel bit rate, it is necessary to pass only one of the two successive logic ones through A10A in 24-channel mode. The reason for transmitting only every fourth bit of the 12-channel signal is explained in f below.

f. When data (in the 12-channel mode of operation) is retimed by data retimer flip-flop A10A, as explained in c above, the trigger signal (E16) to A10A from A8D was described as occurring in coincidence with every fourth clock (1T2304) pulse (waveform J). Thus, the operation of A10A assured the retiming and transmission of every fourth bit in the 1CSPCM signal. However, out of every four consecutive bits in 1CSPCM two bits are data bits and two bits are dummy bits (waveform L). To identify which one of the four was retimed and transmitted, signal 1T288 is used. The time of one-half cycle of 1T288 equals four baud times of signal 1CSPCM, so it is used to select four consecutive bits from data signal 1CSPCM. These signals, four consecutive bits of 1CSPCM and 1T288, are compared in an exclusive

OR gate and the result of only one of these comparisons is checked by dummy match failure gate A2A, as timed by signal 1DS. Only one combination in the comparison will not give a mismatch. This results when 1DS is so timed that it checks the comparison of a dummy pulse that is a logic one when 1T288 is logic one. This is a match and will continue to be match at each sample time because when 1T288 changes to logic zero, the dummy pulse will also be zero. When this condition exists, signals 1DS (E19) and the trigger pulse (E16) of data retimer flip-flop A10A both occur every fourth data bit time (when the radio set is in 12-channel mode) but are exactly 180° out of phase (waveforms J and K). Therefore, when IDS corresponds to a dummy bit, the trigger signal at E16 must correspond to a data bit and it is assured that data bits and not dummy bits are being retimed and transmitted through A10A. Exclusive OR gate A9, dummy sample flipflop A10B and the circuits following them are used to establish this required condition.

g. NAND gate A5C has the same clock inputs as A3A, so its output (1DS) is the same; 120 nanosecond negative pusles occurring in coincidence with every fourth 1T2304 pulse. This signal, which is at the 12-channel data rate, is inverted by NAND gate A8C (waveform K). The output of A8C is connected to the trigger input of dummy sample flip-flop A1OB. Operation of A10B is the same as that already explained for A10A (c above). NAND gates A9A and A9B have four inputs, 1T288, 0T288, 1CSPCM and OCSPCM. With OR gate A9C they operate as an exclusive OR gate, so that whenever 1T288 (waveform E) and 1CSPCM (waveform L) are opposite (either of them at logic one, the other at logic zero), the output of A9C (waveform M) is logic one. This output is connected to the D input of A10B. The 1DS signal at the trigger of A1OB switches the output at pin 9 to logic one and the output at pin 8 (ODMM) to logic zero, when D is logic one. If dummy bits are being sampled by A10B, under the required condition (f above), the output of A10B at pin 8 will always be logic one. The logic one is inverted to logic zero by A12B and the signal is integrated by A13. Under this condition the output of A13 is a positive voltage (logic one). The output of A15 then goes positive (logic one) and the output of inverter A12A (1LIM) is logic zero, inhibiting NAND gate A5A and no further action takes place. This is the required and normal condition of the dummy sampling circuits. When this condition exists, the D input of dummy match failure flip-flop A2A is logic zero and the output of A2A at pin 5 (ODMF) is logic one. This logic one at NAND gate A8B enables gating of the trigger signal for A7B and thus controls signals 1T576 and 0T576. However, when lDS (at pin 11 of A10B) is comparing a bit sample at any time other than under the required condition as explained in f above, the output of A10B at pin 8 will average 50 percent logic ones and 50 percent logic zeros instead of all logic ones. The ODMM signal is inverted by A12B and integrated by A13. The output of A13 changes to a low voltage (logic zero). The output of A15 goes negative (logic zero) and A12A inverts this to logic one. 1LIM is now logic one and NAND gate A5A has two logic one inputs; the input at pin 2 is always logic one when the radio set is operating in 12-channel mode. Also, the output of AIOB at pin 9 is a logic one which causes the output of A5A to be logic zero. The next time 0T1152 goes positive, the outputs of A2A switch and 0DMF becomes logic zero which inhibits NAND gate A8B. The 1T576 and 0T576 signals will remain at their present phase until NAND gate A8B turns on again. The logic one output from pin 6 of A2A causes the output of NAND gate A12D to change to logic one because the other input (pin 12) is already logic one (1LIM signal). This resets A13 so its output returns to a positive voltage (logic one) and through A15 and A12A 1LIM returns to logic zero. This inhibits NAND gate A5A and the D input. to A2A goes to logic zero. The next time OT1152 goes positive, the outputs of A2A switch and ODMF returns to logic one. NAND gate A8B is enabled again and 1T576 and 0T576 are generated again at A7B by 1T1152. During the period described above, the 576--kHz clock was stopped for a time equal to one cycle of T1152. Since the T288 signal is. generated by 0T576, 1T288 was also stopped for one cycle of T1152. One cycle of 1T1152 has a period of 868 nanoseconds; one cycle of 1T288 has a period of 3472 nanoseconds. Thus, 1T288 has been delayed one-quarter cycle, or 868 nanoseconds (equal to two baud at the 12-channel data rate or two bit times). This means that transitions from plus (logic one) to minus (logic zero) for 1T288 occur two bit times later. Since 1T576 was delayed, the data trigger (E16) signal at A10A and 1DS signal are also delayed, however, 1DS still occurs in coincidence with transitions of 1T288 and the signal at E16 still occurs two bit times later. The bit in 1CSPCM being sampled by A10B has now been shifted two places. As explained in *f* above, this may or may not create the required condition to assure that data

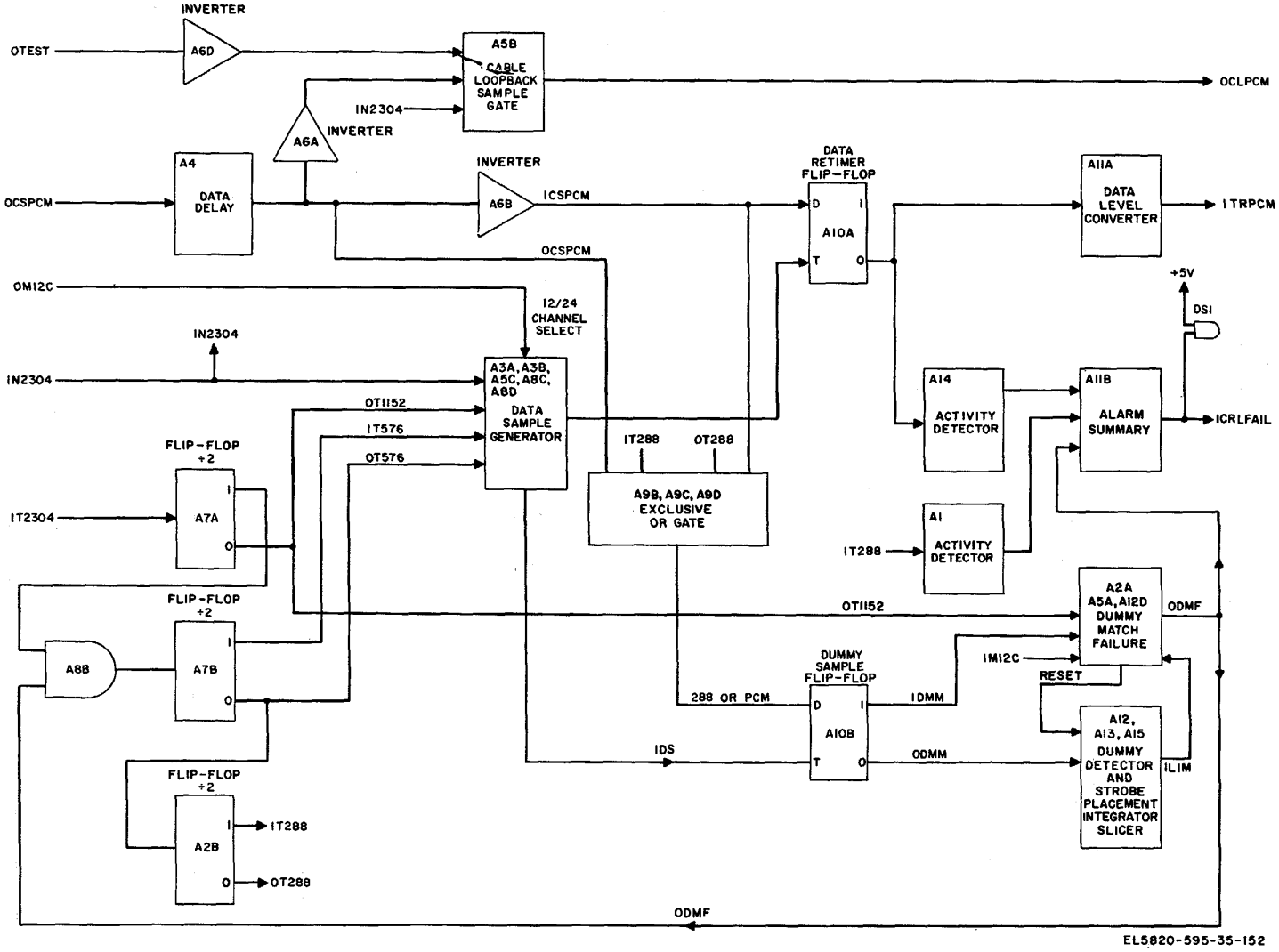


Figure 1-5. Cable digital processor 1A12A4, block diagram.

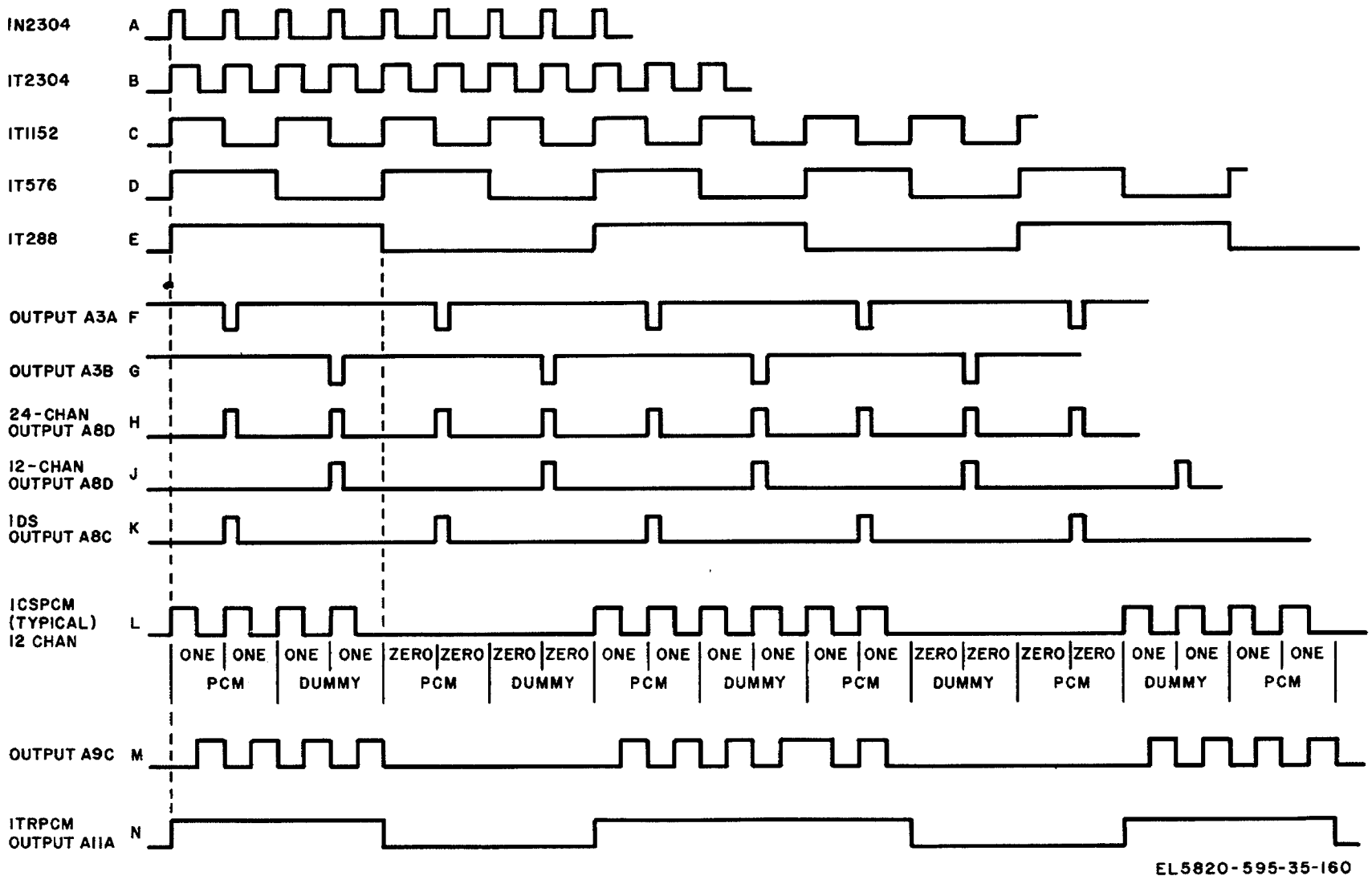


Figure 1-6. Cable digital processor 1A12A4, timing diagram.

bits are being retimed and transmitted through A10A. If it does not, dummy sample flip-flop A10B will continue to genertate 50 percent logic ones and 50 precent logic zeros. The action described above will be repeated and 1T576 and 1T288 will be shifted again. A maximum of three shifts of -Liming for these signals assures that the correct condition will be established.

h. Activity detectors A1 and A14 have identical circuits; A1 monitors the outputs of A2B (1T288) and A14 monitors the to radio pcm (1TRPCM) output of A11A. Both activity detectors (A1 and A14) are monostable multivibrators which provide a high (logic cne) output for 100 microseconds each time they receive a negative pulse (logic zero) at the trigger (S) input. Their outputs therefore will remain high (logic one) as long as they receive input pulses indicating activity of the signal being monitored.

i. The output of summary alarm or gate A11B is normally low and lamp DS1 is lighted. If either activity detector (A1 or A14) or the output (ODMF) of dummy match failure flip-flop A2A switches to logic zero output, the output of A11B changes to logic one (high) and lamp DS1 goes out. The output of A11B (1CRLFAIL) is sent to alarm monitor 1A12A6.

1-14. AF Amplifier 1A12A5 Block Diagram Description
(figs. 1-7 and 8-27)

a. AF amplifier 1A12A5 contains two 3-stage audio amplifiers. The first amplifier Q1, Q2 and Q3 is used to amplify the cable order wire signal and deliver a usable output (3 volts peak-to-peak) to order wire assembly 1A13. The second amplifier Q4, Q5, Q6, is used to transmit the order wire signal (4 volts peak-to-peak, minimum) down the cable. The amplifiers each have a common-emitter amplifier stage Q1 and Q4 with a voltage gain of approximately 16. Each voltage amplifier has a frequency response from 20 Hz to 2 kHz. The amplified outputs are direct coupled to their respective buffer amplifier, Q2, Q3 and Q5, Q6 via a low pass filter network.

b. The low pass filter in combination with the amplifier constitutes a unity voltage gain stage which provides current gain; high frequency cutoff point is approximately 2 kHz. The buffer output is coupled to the load by a capacitor and it is also connected to diode level detectors. The level

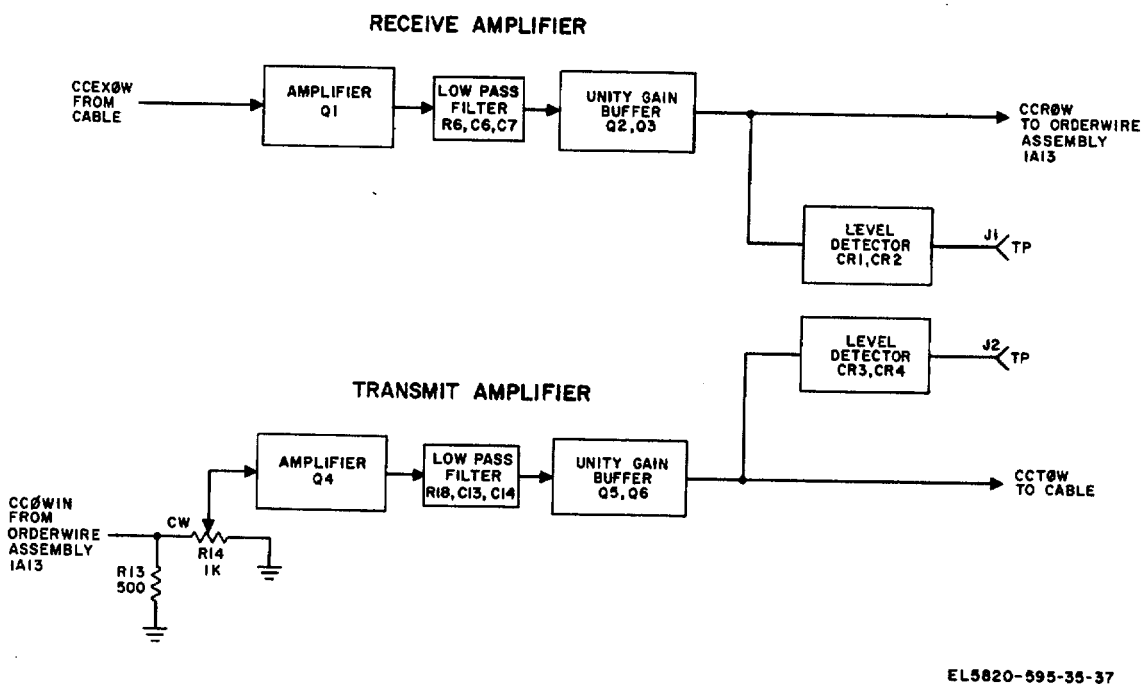


Figure 1-7. AF amplifier 1A12A5, block diagram.

detectors measure the output order wire signal level for monitoring purposes.

1-15. Alarm Monitor 1A12A6 Block Diagram Description
(figs. 8-6 and 8-28)

Alarm monitor 1A12A6 receives alarm signals from other digital data modem circuits and uses logic combinations of the alarm signals to generate traffic and functional alarm indications for the radio-to-cable and cable-to-radio circuits. The summarized alarm signals activate green and red status indicators, a major alarm relay, and control a bypass order wire relay. Input signal 1RRIFAIL is inverted by inverter A8A and sent to radio digital processor 1A12A13. Refer to paragraph 1-21 for discussion of this signal.

a. Cable-to-Radio Circuits. The cable-to-radio circuits of alarm monitor 1A12A6 control the CABLE-TO-RADIO MODEM indicator on meter panel assembly 1A16A4 and the Shelter mounted "traffic in" indicator. Two kinds of signals are monitored by the cable-to-radio circuits-functional alarm signals from 1A12A2 (1CRFAIL), 1A12A3 (1CCFAIL) and 1A12A4 (1CRLFAIL); and the cable traffic signal (XCPCM) from 1A12A2. When a functional failure occurs in 1A12A4, alarm signal 1CRLFAIL is activated (logic one). Since the pcm signal is processed in sequence in 1A12A2, 1A12A3 and 1A12A4, a functional failure in 1A12A3 causes both 1CCFAIL and 1CRLFAIL signals to switch to logic one; and a functional failure in 1A12A2 causes all three signals to switch to logic one. Also, if there is a failure of the cable traffic signal, all three functional failure signals switch to one because each circuit (1A12A2, 1A12A3 and 1A12A4) then loses the pcm signal. Alarm monitor 1A12A6 uses these four inputs to the cable-to-radio circuits to distinguish which kind of failure has occurred-functional failure or cable traffic failure.

(1) *Cable traffic normal*. When cable traffic (XCPCM) is being detected, the output of inverter A3E is logic zero (high) and lamp driver Q10 is turned on. The logic zero from A3E is inverted by A3F and lamp driver Q11 is turned off. Output OCTFL is logic one, 1CTFL is logic zero and the traffic in indicator is lighted green.

(2) *Cable traffic failure*. When loss of the cable traffic signal (XCPCM) occurs, the output of inverter A3E is low and lamp driver Q10 is turned off. The low from A3E is inverted by A3F and lamp driver Q11 is turned on. Output OCTFL is logic zero, 1CTFL is logic one, and the traffic in indicator is lighted red.

(3) *No functional failure*. The 1CRFAIL, 1CCFAIL and 1CRLFAIL signals are inverted by inverters A7B, A7C and A7F, and the resulting output signals are applied to negative OR gate A1B. When there is no functional failure, these signals are all low (logic zero) and all inputs to A1B are high. A1B then applies a low (logic zero) to NAND gate A4C.

(4) *Functional failure*. If any functional failure exists, A1B has at least one input which is low. If a cable traffic failure occurs, all inputs to A1B are low. In either case, A1B applies a high (logic one) to A4C.

(5) *Cable traffic normal-no functional.* failure. When cable traffic is normal and there is no functional failure, the conditions of (1) and (3) above exist and operation is as follows:

(a) The inputs to A4C are low from A1B and high from A3E. The output of A4C is then high, and as a result, lamp driver Q9 is turned on and output signal 1CFFL is logic zero. The output of A4C, inverted to a low by A3C, turns off lamp driver Q8 and output signal OCFFL is logic one. The CABLE-TO-RADIO MODEM indicator is lighted green.

(b) Negative OR gate A2A has high inputs from A4C and A3E and its output is low. NAND gate A2B has a permanent logic one at pin 5, and as a result, functions as an inverter for the signal at pin 6. The low from A2A is inverted by A2B and is applied as a high to negative OR gate A1A. This is the summary alarm output signal for cable-to-radio circuits (b(5) (c), (6) (c), and (7) (c) below).

(c) The output of A3E is high, lamp driver Q10 is turned on and output signal 1CTFL is logic zero. The high from A3E is inverted to low by A3F, lamp driver Q11 is turned off and output signal OCTFL is logic one. The traffic in indicator is lighted green.

(6) *Cable traffic normal-functional failure.* When cable traffic is normal and there is a functional failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) The inputs to A4C, from both A1B and A3E, are high and the output is low. Lamp driver Q9 is turned off and output signal 1CFFL is logic one. The output of A4C, inverted to high by A3C, turns on lamp driver Q8 and output signal OCFFL is logic zero. The CABLE-TO-RADIO MODEM indicator is lighted red.

(b) Negative OR gate A2A receives a low from A4C and its output is high. The high from A2A is inverted to low by A2B and applied to A1A*(b)* (5) *(c),* (6) *(c),* and (7) *(c)* below).

(c) The output of A3E is still high and Q10, Q11, 1CTFL and OCTFL are as explained in (5)(c) above. The traffic in indicator is still lighted green.

(7) *Cable traffic failure.* When a cable traffic failure occurs (loss. of the XCPCM signal), all functional failure signals are also affected and change to logic one (high). The conditions of (2) and (4) above then exist and operation is as follows:

(a) The inputs to A4C are high from A1B and low from A3E. The output of A4C is high and operation is as explained on (5) (a) above.

(b) Negative OR gate A2A receives a low from A3E and its output is high. The high output from A2A is inverted to low by A2B and applied to A1A (b (5)(c), (6)(c), and (7)(c) below.

(c) The output of A3E is low, lamp driver Q10 is turned off and output signal 1CTFL is logic one. The low from A3E is inverted to high by A3F; lamp driver Q11 is turned on and output signal OCTFL is logic zero. The traffic in indicator is lighted green.

b. *Radio-to-cable circuits*. The radio-to-cable circuits of alarm monitor 1A12A6 control the RADIO-TO-CABLE MODEM indicator on meter panel assembly 1A16A4 and the shelter mounted "traffic out" indicator. Two kinds of signal are monitored by the radio-to-cable circuits-functional signals from 1A12A8(1RRIFAIL), 1A12A9 (1RCFAIL), 1A12A10 (IF(1)FAIL), 1A12A12 (IF(2)FAIL) and 1A12A13 (1RPFAIL); and the radio traffic failure signal from 1A12A8. The functioning of these signals is similar to that described for cable-to-radio circuits. That is, since the radio pcm signal is processed in sequence through the indicated circuits, a functional failure in any plug-in module causes that module and any modules following it in the processing sequence to activate the functional failure signal. Likewise, when the radio pcm signal (FRPCM) fails, all functional failure signals are activated. The radio-to-cable circuits use these signals to distinguish which kind of failure has occurred-functional or radio traffic failure.

(1) *Radio traffic normal*. When radio traffic is normal, signal 1FRFAIL (from 1A12A8) is logic zero and the output of inverter A8D is high. Relay driver transistor Q7 is turned on and output signal 1BPOW is at logic zero. The output signal (high) from A8D is inverted by negative OR gate A4D (input pin 12 of A4D is always high from switch S1A) and inverted again by A7D. Negative OR gate A1A, therefore, has a high input at pin 1, negative OR gate A4B has a high input at pin 6 and NAND gate A4A has a high input at pin 2.

(2) *Radio traffic failure*. When loss of the radio traffic signal occurs, signal 1FRFAIL is logic one and the output of inverter A8D is low. Relay driver transistor Q7 is turned off and output signal 1BPOW is at logic one. Signal 1BPOW is connected to order wire assembly 1A13 and, when it is a logic one, activates a relay which causes the from radio (FRPCM) signal to be applied directly to order wire assembly 1A13 instead of through digital data modem 1A12. This connection allows order wire communications to be maintained when the radio pcm signal is lost. The output signal (low) from A8D is inverted first by A4D, and inverted again by A7D. Negative OR gate A1A, therefore, has a low input at pin 1; negative OR gate A4B has a low input at pin 6, and NAND gate A4A has a low input at pin 2.

(3) *No functional failure*. When there is no functional failure, the output signals of inverters A8A, A8B. A8C, A8F and A8E are all high and the corresponding inputs at negative OR gate A9 are high. The signal at pin 3 of A9 is always high except when the CABLE LOOP TEST switch is in TEST position. Since module input pins J and 11 are not connected externally and are connected to +5v internally, .A2C always applies a high to A9 at pin 9. With all input signals high, the output of A9 is low and A4A has a low at pin 1. The low output of A9 is inverted to a high by inverter A7E, so A4B has a high at pin 5 and A1A has a high at pin 13.

(4) *Functional failure.* When a functional failure occurs, the output of at least one inverter (A8A, A8B, A8C, A8F, or A8E) switches to low and the output of A9 is then high. The output of A9 is also high without a functional failure if the CABLE LOOP TEST switch is placed in TEST position. In either case, A4A has a high at pin 1. The high from A9 is inverted by A7E, so A4B has a low at pin 5 and A1A has a low at pin 13.

(5) *Radio traffic normal-no functional failure.* When radio traffic is normal and there is no functional failure, the. conditions of (1) and (2) above exist and operation is as follows:

(*a*) A4A has a high at pin 2 and a low at

pin 1 and its output is high. Lamp driver Q1 is turned on and signal 1RFFL is logic zero. The high output of A4A is inverted to low by A3A, and lamp driver Q2 is turned off. Signal ORFFL is logic one and the RADIO TO CABLE MODEM indicator is lighted green.

(*b*) A4B has a high at both inputs and its output is low. Lamp driver Q3 is turned off and signal 0RTFL is logic one. The low output from A4B is inverted by A3B and lamp driver Q4 is turned off. Signal 1RTFL is logic zero and the traffic out indicator is lighted green.

(*c*) A1A has high inputs at pins 13 and 1. If there is no failure in the cable-to-radio circuits, the output of negative OR gate A2A is low (a(5) (b) above). NAND gate A2B inverts the signal from A2A because its other input (pin 5) is always high, so A1A has a high at pins 2 and 3. With all inputs high, the output of A1A is low and this is inverted to high by A3D. Transistor Q5 is turned on, Q6 is turned off and signal OMARY is high (no alarm).

(6) *Radio traffic normal functional failure*. When radio traffic is normal and there is a functional failure, the conditions of (1) and (4) above exist and operation is as follows:

(a) Both inputs to A4A are high and its output is low. Lamp driver Q1 is turned off and signal 1RFFL is logic one. The low output of A4A is inverted to low by A3A and lamp driver A2 is turned on. Signal ORFFL is logic zero. The RADIO-TO-CABLE MODEM indicator is lighted red.

(b) The inputs to A4B are high at pin 6 and low at pin 5. The output, therefore, is high. Lamp driver Q3 is turned on and signal ORTFL is logic zero. The high output from A4B is inverted by A3B and lamp driver Q4 is turned off. Signal 1RTFL is logic one. The traffic out indicator is lighted red.

(c) The inputs to A1A are low at pin 13, from A7E, when a radio-to-cable functional failure exists; or low at pins 2 and 3, from A2B, when a cable-to-radio functional failure exists (a(6) (b) above). The output of A1A is high and this is inverted to low by A3D. Transistor Q5 is turned off, transistor Q6 is turned on, and signal OMARY is low (alarm condition).

(7) *Radio traffic failure*. When a radio traffic failure occurs (loss of the FRPCM signal), all functional failure signals are also affected and switch to logic one (high). The conditions of (2) and (4) above, then exist and the relay driver circuit is activated as explained in (2) above. Other operation is as follows: -

(*a*) The input signals to A4A are low at pin 2 and high at pin 1 and its output is high. Otherwise, operating conditions are as explained in (5) (a) above.

(*b*) Both inputs to A4B are low and its output is high. Otherwise, operating conditions are as explained in (6) (b) above.

(*c*) A1A has a low input at pin 1 and its output is high. Otherwise, operation is as explained in (6) (c) above.

c. *Switch S1*. Alarm monitor 1A12A6 also contains switch S1 which has three sections: section SIB is used to disconnect the automatic gain control from the receiver (for testing purposes) and supply a fixed agc signal (RAGC-SW) to radio digital regenerator 1A12A8; section S1A is used to cut off the alarm input from the receiver (ORCVR FAIL) for testing; and section S1C lights lamp DS1 when the switch is placed in the TEST position.

1-16. Amplifier-Detector 1A12A7 Block Diagram Description
(figs. 1-8 and 8-29)

a. Amplifier-detector 1A12A7 receives the pcm plus order wire (FRPCM) signal from the receiver and the reshaped pcm signal (1RSPCM-2) from 1A12A8. The function of 1A12A7 is to recover the order wire signal from the FRPCM signal (that is, eliminate the pcm component) and provide an amplified order wire signal as output. The basic method used to accomplish this purpose is to apply the two input signals (FRPCM and 1RSPCM-2) to a subtractor. The output signal of the subtractor is the difference between the input signals. This will be the order wire signal if the pcm components of the input signals are equal. The circuits of 1A12A7 (other than the subtractor and the audio output amplifier) are used to create this equality of pcm components at the subtractor inputs. The FRPCM (pcm plus order wire) signal is passed through a low pass filter which eliminates the high frequency components of the pcm signal but passes some low frequency components. This signal is applied to one input of the subtractor. The pcm signal (1RSPCM-2) was separated from the FRPCM signal and reshaped in 1A12A8, so it is not the same as the pcm component of the FRPCM signal. To equalize for this, the amplitude,

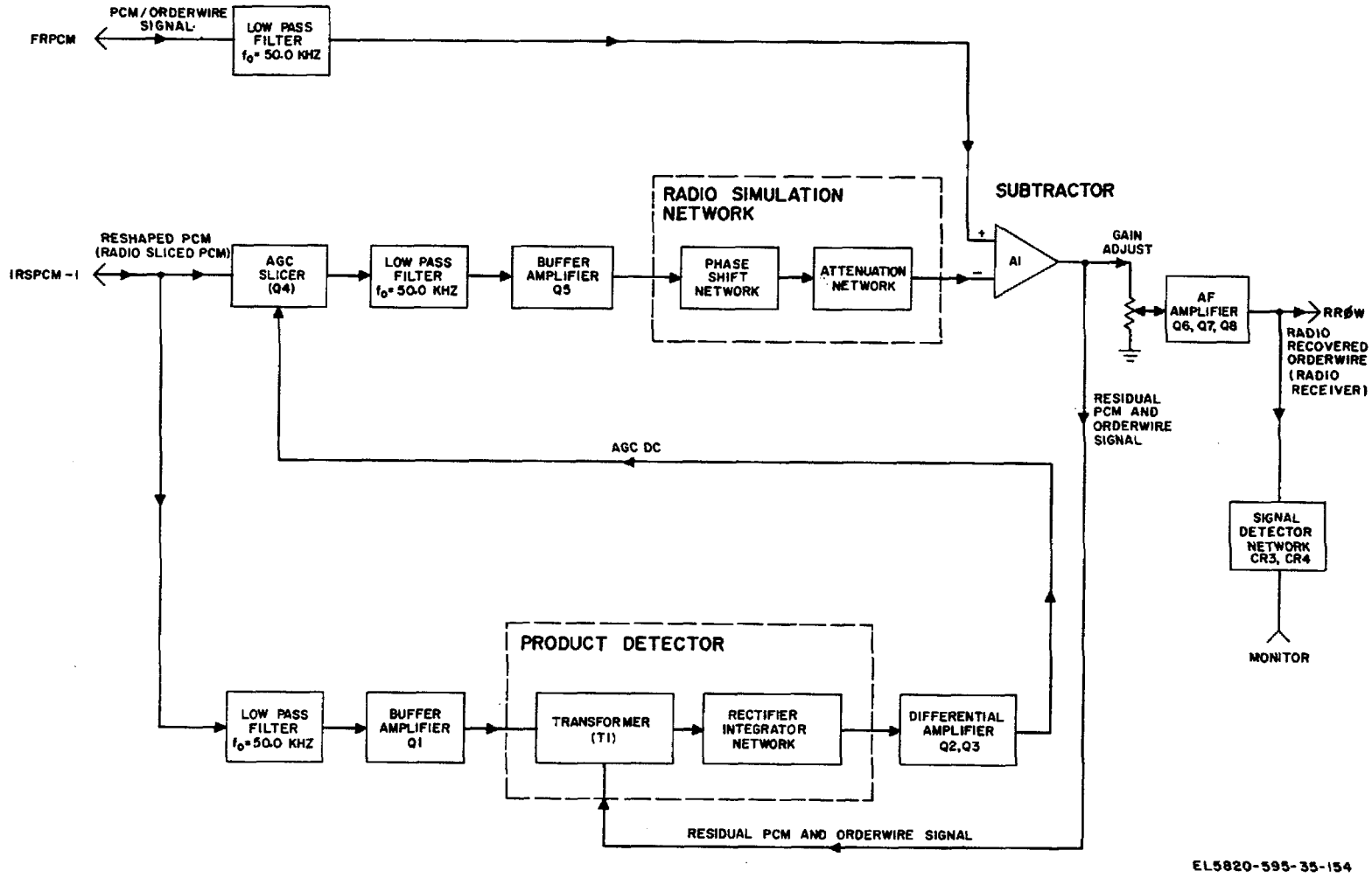


Figure 1-8. Amplifier-detector 1A12A7, block diagram.

phase shift and attenuation characteristics of the pcm (1SPCM-2) signal are, modified so that they approximate the similar characteristics of the pcm component of the FRPCM signal. The 1RSPCM-2 signal is also passed through a low pass filter. The characteristics of the pcm components of the input signals are then approximately equal. The output signal of the subtractor is applied to the audio amplifier and to a feedback circuit. The feedback circuit applies the output signal to the product detector circuit. If there is a residual pcm component in the output signal, it is combined with the 1RSPCM-2 signal in the product detector. The output of the product detector, through the differential amplifier, controls the amplitude of the pcm (1RSPCM-2) signal input to the subtractor and so reduces the residual pcm component at the output of the subtractor to a minimum.

b. The FRPCM signal from the radio is passed through a 50-kHz low pass filter to remove high frequency components before processing. At the output side of the filter, the signal consists of order wire plus residual pcm and noise components below 50 kHz. The filtered signal is applied to the noninverting input of the subtractor stage (differential amplifier A1).

c. The 1RSPCM-1 signal is sliced by the age slicer (Q4). The amplitude of the age slicer output signal is controlled so that it is the same amplitude as FRPCM signal (approximately 1 volt peak-to-peak). Age slicer amplitude is controlled by a dc signal from differential amplifier Q2 and Q3. The dc signal is developed by the 1RSPCM-1 signal through the product detector and the residual pcm from the subtracting network. The product of these signals produces a dc output from the rectifier and integration network which is applied to differential amplifier Q2 and Q3, which, in turn, provides age slicer gain. The signal is then passed through a 50-kHz low pass filter, to remove the very high frequency components, and applied to emitter follower buffer amplifier Q5.

d. The pcm signal is then applied to the radio simulation network where the low frequency components of the signal are phase shifted and attenuated in the same manner as were the low frequency components of the FRPCM signal during radio transmission. The radio simulation network consists of two sections: The first section provides for simulation of the low frequency phase shift and a portion of the attenuation characteristics of the radio; the second section provides the additional phase shift and attenuation required to properly simulate the radio characteristics. The output of the radio simulation network is applied to the second input of the subtractor (inverting input).

e. The only difference between the two input signals applied to the subtractor is the order wire signal which has been added to the FRPCM signal prior to radio transmission. The output of the subtractor stage therefore, is the order wire signal plus a residual pcm signal. The order wire signal is amplified by the AF amplifier stage (Q6, Q7, QS8). The audio amplifier has an adjustment for gain and a low pass network to attenuate the residual pcm. The output of the amplifier (RR0W) is applied to order wire assembly 1A13 for further processing. A signal detection network (CR3, CR4) generates a dc output level monitor when an order wire is present.

1-17. Radio Digital Regenerator 1A12A8 Block Diagram Description

(fig. 1-9)

a. The radio digital regenerator receives the pcm plus order wire signal (FRPCM) from the radio; separates the pcm signal from the order wire signal; amplifies this signal and regenerates a full-baud digital data signal (1RSPCM-1 and 1RSPCM-2). Additional functions are-

(1) Detects the presence of data transitions of the FRPCM signal and when data transitions are not detected, generates a traffic alarm (1FRFAIL).

(2) Monitors the level of radio receiver age signal (RAGC) and generates a squelch audio (0SA) and inhibit phase-locked loop clock signal (01NHP) when the age signal indicates loss of adequate radio reception.

(3) Detects presence of data transitions on 1RSPCM-2 signal and produces a logic 0 level if the data is missing. This is compared with the 0SA and 01NHP signals to produce a radio receiver interface failure signal (1RRIFAIL) if any of these three signals are logic 0.

b. The incoming signal FRPCM is applied to differential amplifier Q1A, B which generates a signal proportional to the difference between the input signal and a fixed reference. The linear buffer Q2, Q3 provides a signal with a low impedance source to drive the following peak detectors. The peak detectors consist of two half-wave diode rectifiers and filter circuits. The time constants of

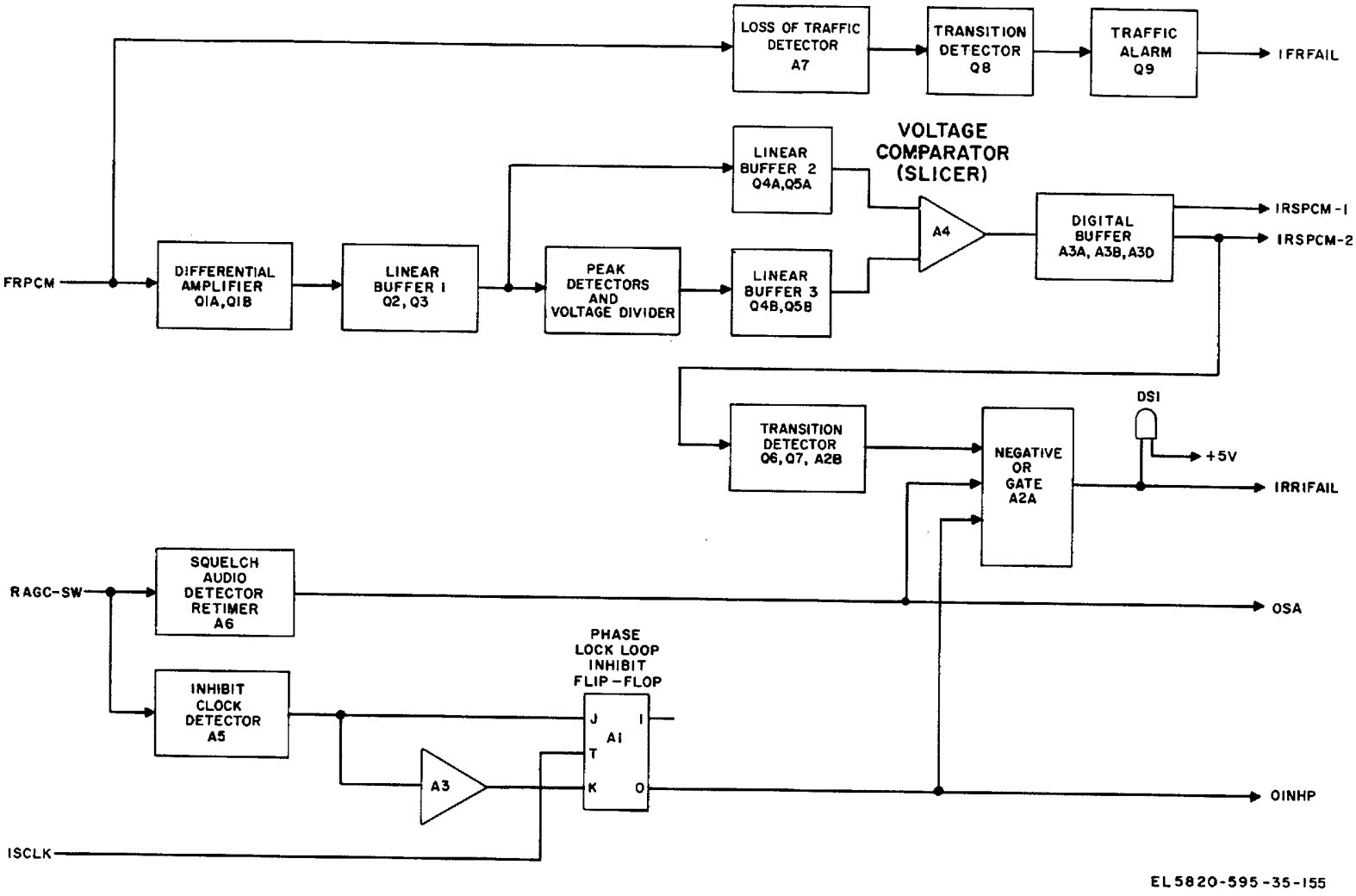


Figure 1-9. Radio digital regenerator 1A12A8, block diagram.

the filter circuits allow the capacitors to charge to the positive and negative peak excursions of the input signal.

c. The detected signals are applied to a voltage divider which derives the algebraic average of the peak-detected voltages. The linear buffers, Q4 and Q5, provide a high impedance buffer between the peak detector circuits and the input of voltage comparator A4. Voltage comparator A4 compares the inputs from linear buffers Q4 and Q5. The output of linear buffer 3 (Q4B and Q5B) is the reference signal for the voltage comparator. When the amplified FRPCM output of linear buffer 2 (Q4A and Q5A) is more positive than the reference, the voltage comparator output is high; when the amplified FRPCM signal is more negative than the reference, the voltage comparator output is low.

d. Digital buffer A3A inverts the output (pcm signal) of the voltage comparator for application to digital buffers A3B and A3D. These reinvert the signal and provide parallel outputs (1RSPCM-1 and 1RSPCM-2).

e. In the loss-of-traffic detector the FRPCM input signal is compared to a dc reference level. A7 produces a switching signal at the output which is detected by transition detector Q8. Q8 generates a high logic level while there are transitions out of A7, and a low logic level output if there are no (or very few) transitions. A low level output from A7 causes traffic alarm Q9 to provide a traffic alarm signal.

f. The output of digital buffer A3B (1 RSPCM-2) is also monitored by a transition detector consisting of integrator Q6 and inverter Q7. This circuit functions the same as the loss of traffic detector configuration. The output is applied to digital buffer A2B which provides the proper logic level to one input of negative OR gate A2A.

g. The squelch audio detector monitors the RAGC-SW signal from the radio receiver and compares it to dc reference level. If the input signal is more positive than the reference, output OSA is at a high logic level; if the input signal is more negative than the reference, output OSA is logic 0. OSA goes to negative OR gate A2A, which detects a functional error.

h. The inhibit clock detector A5 monitors the receiver RAGC-SW signal level and generates control levels for the phase-lock loop inhibit flipflop Al which inhibits the phase-locked loop when there is loss of adequate radio reception. When the input signal is more positive than the reference voltage, A5 produces a logic zero output level. This is applied as a "one" to the J input of phase-lock loop flip-flop Al. A3C inverts the logic level and applies it to the K input. The square wave clock signal (1SCLK) gates the logic one into the flip-flop which produces a logic one level at the reset output 01NHP. When the input to A5 is less than the required level (low agc) A5 produces a logic-one output level which sets the phase-lock loop flip-flop and produces a logic zero inhibit level at the output 01NHP.

i. The three alarm signals, 0SA, 01NHP, and the output of digital buffer A2B are applied to the input of negative OR gate A2A. If any signal is low, the output of negative OR gate A2A (1RRIFAIL), is high, holding lamp DS1 off. This indicates detection of a circuit functional failure on the board or low agc signal from the radio receiver. When there is no failure, 1RRIFAIL is a logic zero and lamp DS1 is on.

1-18. Radio Control Comparator 1A12A9 Block Diagram Description

(figs. 1-10 and 8-31)

a. The function of radio control comparator 1A12A9 is to determine the phase difference between the clock and data signals and to use this information to generate a control signal. The control signal is then used to shift the phase of the clock signal until data and clock are in phase. Radio control comparator 1A12A9 receives the 4608kHz radio-to-cable clock (0R4608) signal from 4608 kHz vco 1A12A14 and the reshaped pcm (1RSPCM-2) signal from radio digital regenerator 1A12A8. The 0R4608 signal is divided by two successively to generate 2304-kHz, 1152-kHz, and 576-kHz radio-to-cable clock signals. These signals are sent to radio digital processor 1A12A13. In radio control comparator 1A12A9, the 12-channel baud generator is turned on and the 576-kHz clock is used for phase comparison with data when the radio set is in the 12-channel mode of operation. In the 24-channel mode, the 24-channel baud generator is turned on and the 1152-kHz clock is used.

b. The operation of the data and clock pulse generators and the phase comparator is the same as that of similar circuits in cable control comparator 1A12A3. Only the differences are described in *c* below. The remainder of the circuits of 1A12A9 are the same as corresponding circuits in

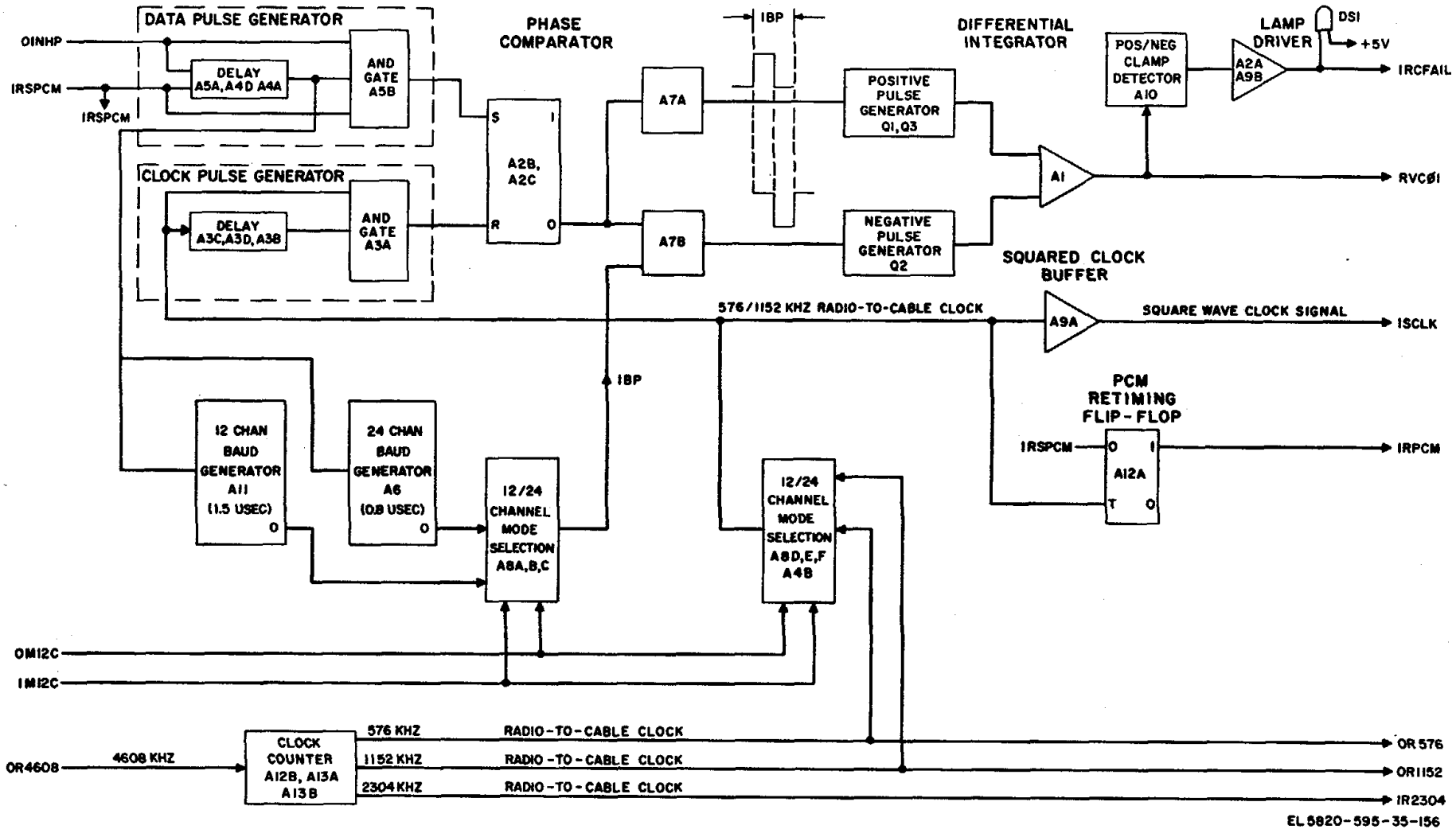


Figure 1-10. Radio control comparator 1A12A9, block diagram.

1A12A3 and their functional operation is the same (para 1-12).

c. There are Two inputs to the data pulse generator stage, reshaped pcm, 1RSPCM-2 and inhibit phase-lock loop clock 0INHP from radio digital regenerator 1A12A8. When the amplitude of the signal from the radio receiver falls below a predetermined level, OINHP is logic zero (low) and phase comparison of clock and data is prevented. This is true for both 12 and 24-channel modes of operation. Normally OINHP is logic one and operation of the data pulse generator is not inhibited. In 12-channel mode of operation, signal 1M12C is logic one and 0R576-kHz radio-to-cable clock from A12B is gated through AND gate A8D, OR gate A8F, and inverter A4B to provide the signal for operation of the clock pulse generator. In 24 channel mode, 0M12C is logic one and 0R1152kHz radio-to-cable clock is gated through AND gate A8E and OR gate A8F. The data and clock pulse generators then generate signals 0DP, 0CP and 0FP. The output signal from the data pulse generator at E7 drives both baud generators at all times but the output used is determined by the mode of operation. In 12-channel mode, the 12 channel baud generator signal from All is gated through AND gate A8B and OR gate A8C to provide signal 1BP. The duration of 1BP is adjusted (for 12-channel mode) so that time from the start of ODP pulse until the end of 1BP pulse is 1736 microseconds. In 24-channel mode, the 24 channel band generator signal from A6 is gated through AND gate A8A and OR gate A8C. The duration of 1BP is adjusted (for 24-channel mode) so that time from the start of 0DP until the end of 1BP is 868 microseconds. In either mode of operation, the selected clock output from A4B is again inverted by squared clock buffer A9A and sent to other digital data modem circuits used in the radio-to-cable function.

1-19. Control Processor 1A12A10 and 1A12A12 Block Diagram Description
(figs. 1-11 and 8-32)

a. General. The control processors receive the full-baud retimed pcm signal and the square wave clock signal from radio control comparator 1A12A9, The square wave clock is signal phaselocked with the retimed pcm signal. The function and operation of the control processors is based on the characteristics of the pcm signal under both 12-channel and 24-channel modes of operation.

b. *Signal Characteristics (12-Channel).* When the radio set is operating in the 12-channel mode, the pcm signal carries 12 channels of information. In the 12-channel mode of operation, sync bits alternate logic ones and logic zeros in successive frames. The data rate in 12-channel mode is 576 kilobits per second, so one bit time (baud) is 1.736 microsecond and the time of one frame is 125 microseconds. The pcm signal is sent out on the cable, to a demultiplexing station. The demultiplexer identifies each of the 12 information channels by counting from the sync bit. To assure reliability, a new sync bit is inserted into the outgoing pcm signal. Thus, errors occurring at the sync bit time, usually due to a "noisy" RF link (making a logic one look like a logic zero or the reverse) are corrected. Bits 1 through 71 of a frame are data, bits and are random and individually unpredictable, however, any bit (1 through 71) will average 50 percent logic ones and 50 percent logic zeros. If a bit selected at random from the pcm signal is compared with a clock pulse that changes polarity every 125 microseconds, matching (both signals logic one or both logic zero at the same time) could be expected only 50 percent of the time. However, if the randomly selected bit is the sync bit (which alternates logic ones and logic zeros every 125 microseconds), the result is that it matches 100 percent of the time, if the phase of the 4-kHz square wave (125 microseconds logic one, and 125 microseconds logic zero) is correct, If the phase is not correct it is shifted until it is correct. The correction is performed by the control processors. The output signal generated, 1ST (sync time), is sent to radio digital processor 1A12A13, where insertion of the new sync pulse is performed.

c. Signal Characteristics (24-Channel). In the 24-channel mode, the pcm signal is comprised of two separate 12-channel signals similar to the one described in b above, but with the following differences. One 12-channel signal, designated PCM-1, has a sync pattern of alternating logic ones and logic zeros in successive frames. The second 12-channel signal, designated PCM-2, has a sync -pattern of logic ones in two successive frames, followed by logic zeroes in the next two successive frames. Thus, the PCM-1 sync pattern for four successive fames (starting with logic one) is 1010; the PCM-2 pattern for four successive frames (staring with the first of a pair of logic ones) is 1100. PCM-1 and PCM-2 each operate at the 12-channel bit rate, 576 kilobits per

second and a baud time of 1.736 microsecond. These two signals are combined into one signal by interleaving alternate bits from PCM-1 and PCM-2. The combined signal has a data bit rate of 1152 kilobits per second and one baud is 868 nanoseconds. After PCM-1 and PCM-2 are combined to form one 24-channel pcm signal, all bits are full-baud at the data rate of the combined signal. When PCM-1 and PCM-2 are combined, if the starting times for frames of PCM-1 and PCM-2 coincided, then in the combined signal, bit 1 of PCM-1 would be followed by bit 1 of PCM-2, and so on, with bit 72 of PCM-1 followed by bit 72 of PCM-2. But the time relationship of frames of PCM-1 and PCM-2 is unknown and indeterminate because they are generated separately and independently. The frame starting time of PCM-1 occurs anywhere from 0 to 71 baud times ahead of the frame start time of PCM-2. The sync bits of PCM-1 and PCM-2 are therefore separated by some indeterminate time interval in the combined (24-channel) signal. Control processor 1A12A10 searches for and locates the sync bit of PCM-1; control processor 1A12A12 searches for and locates the sync bit of PCM-2.

d. Counter and Logic Signals (12-Channel). In the 12-channel mode, square wave clock (1SCLK) signal is 576 kHz. This signal is divided by a series of counters to provide the timing signals required.

(1) Counter A18 divides 1SCLK by two and provides output signals 1TA and 0TA. 0TA is one input to AND gate A4B. 1TA drives the first divide-by six counter. When 1 SCLK (at the trigger input of A18) has a negative transition, the state of the outputs changes. Thus 1TA is logic one for one cycle of 1SCLK and logic zero for the next cycle and its frequency is 288 kHz. The J and K inputs to A18 are through the gates. The OHALT signal input to these AND gates is normally logic one; for explanation of the logic zero state of OHALT refer to (6) below. The other input to the AND gates is always logic one in 12-channel mode.

(2) The flip-flops for the divide-by-six counters are connected as a Johnson counter; that is, the logic one output of the third (TD) stage is fed back to the K input of the first stage (TB) and the logic zero output of the third stage is fed back to the J input of the first stage. The counter sequence is as follows:

Divide-by-Six Counter Sequence Chart

State	TB	TC	TD
0	1	0	0
1	1	1	0
2	1	1	1
3	0	1	1
4	0	0	1
5	0	0	0

There are two other states not shown in the sequence chart, these are 101 and 010. By following the shifting rule, state 101 is followed by state 010, and state 010 is followed by state 101. Thus, if the counter started this way it would cycle between these two states and be divided by two instead of six. AND gates A10C and A10D are incorporated to prevent this from occurring. When the unwanted state 010 occurs, a low clearnot signal resets flip-flop TC (or TF for the other counter) forcing a change to state 000. When state 101 occurs first, it will be followed by state 010 and the reset function will force the counter to change to state 000. Output 0TB, at 48 kHz is used to drive the second divide-by-six counter. Output 1TD is combined with OTA in AND gate A1A to derive 0X5. 0TB and 0TC are combined with 0X5 in AND gate A4A to derive 1X6. 1TB and 0TC are combined in AND gate A1C to derive 0X1. 0X1 is inverted to 1X1 by inverter A1D. 1X1 and 1X3 are combined with 0TA in AND gate A4B to derive 0ST. The first divide-by-six counter is driven by 1TA (288 kHz) and its output is 48 kHz. The second divide-by-six counter is, driven by 0TB and its output is 8 kHz. Counter TH (A8B) divides by two, however, its output is not used in 12-channel mode as AND gate A10B has logic zero at pin 6. In the 12-channel mode, AND gate A9B has logic one at all inputs except OTE (pin 7) so AND gate A9B and inverter A10A both invert 0TE. Therefore, 1R8 is the same as 0TE. Decode gate A9A ANDS 1TE and 0TF since, in the 12-channel mode the other two inputs (pins 3 and 13) are always logic one. The output of A9A is inverted by A1B to derive 1X3. Sync time clock generator A4B ANDS 1X3, 1X1 and 0TA to derive 0ST. The time relationships of all signals described above are illustrated in figure 1-12.

(3) Counter T1 supplies timing for an option not used in AN/GRC-143. Sync pattern reference generator All is a Johnson type counter. In control processor 1A12A10, output pin 7 is connected to pin 8 in the connector wiring, so the J and K inputs of A11B are both fixed at logic one and A11B is then a divide-by-two counter. Since

the input (1R8) is 8 kHz, the output is 4 kHz. The 1REF (frame reference signal) is sent to radio digital processor 1A12A13. The 0REF signal goes to OR gate A6B.

(4) The mismatch shift register consists of gates A5D, A5E, flip-flop A3A and 8-bit shift register A2. Shift register A2 contains 8 flip-flops with an AND gate at the D input. Shift pulses are applied to the T input (pin 9) which triggers all internal flip-flops. These flip-flops are referred to as stages M0 through M7 where M7 is the input flip-flop and M0 is the output flip-flop. The output of the shift register 1M0 is fed back through AND gate A5D and OR gate A5E to the D input of flip-flop A3A which is designated stage M8. The output of flip-flop M8 connects to the data input of the 8-bit shift register; thus, these circuits together comprise a 9-bit recirculating shift register. The circulating data may be modified by the gates in the circular path.

(5) A group of nine clock pulses is generated in each frame by shift register clock generator gate A4C. These pulses (0SHC) are generated during gate time 1X6 by 1SCLK (fig. 1-12). These nine shift pulses circulate the data in the shift register once during each frame.

(6) Halt gate A12 produces a logic zero output level to inhibit the timing counter advance when all the input levels are at logic one. The following are the required conditions for the start of a-halt:

(a) Signals 1TA, 1X1 and 1X3 must be logic one. This occurs, once per frame, at the end of frame sync time (signal 1ST).

(b) Signals 1SM and 1SL (from 1A12A13) must be logic one.

(c) The output signal (pin 6) of register stage M8 must be a logic one.

e. Synchronous Operation (12-Channel). When the radio set is operating in the 12-channel mode, TRAFFIC SELECT switch 1A12A15A1S2 is in the 12 CHAN position. Signal 0M12C input (pin 12) to control processor 1A12A10 is then logic zero; signal 0M12C input (pin 18) to control processor 1A12A12 is also logic zero. At control processor 1A12A12, signal OM12C is connected to the J and K inputs of counter flip-flop A18, holding them at logic zero. When the J and K inputs of a J-K flip-flop are both logic zero, the output does not change with trigger signals. Thus control processor 1A12A12 does not generate timing signals and is not used when the radio set is in 12-channel mode. In 12-channel mode, the bit rate of the input signal (1RPCM) to the inverse exclusive OR gate (A6B, A5) is 576 kilobits per second. The frequency of the 0REF (1) input to A6B is 4 kHz, therefore, 0REF (1) changes polarity every 125 microseconds. The operation of the inverse exclusive OR gate is as follows: When the inputs at A6B match (are both logic one or are both logic zero), the output at A5C (1MMF) is logic one (mismatch); when the inputs do not match (one signal at logic one while the other is logic zero), 1MMF is logic zero (match). Signal 1MMF is connected to the D input of mismatch flip-flop A3B and to inverter A1CC. When the sync bit has been located and normal synchronous operation is proceeding, signal 1MMF is always logic zero at frame sync time. (How synchronous operation is established is explained in f below.) Signal OST at the output of sync time clock generator A4B goes to logic zero for one baud time in coincidence with transitions of the 0REF signal (fig. 1-12). 0ST is inverted to 1ST (frame sync time) by A6A and is sent to radio digital processor 1A12A13. It is also A: NDed with 1SCLK in AND gate A6C and inverted again by A6D to provide 1MT (match time-PCM) which is sent to 1A12A11. Note the timing of these signals (fig. 1-10). 1ST is derived at sync time clock generator A4B. Since the shortest logic one input to A4B is 0TA (288 kHz), 1ST is logic one for one baud time (at the 12 channel data rate). Also, since it is generated in coincidence with transitions of 1TE, it occurs at 125 microsecond intervals which is the frame rate. 1MT, derived from 1ST and 1SCLK, is a half-baud pulse corresponding to the last half of 1ST and triggers mismatch flip-flop A3B. At this time, comparisons of 1RPCM and 0REF (1) are occurring in the inverse exclusive OR gate at the 12-channel bit rate. Signal 1MMF is random logic ones and logic zeros until the sync bit of 1RPCM arrives; at that time 1MMF is always logic zero. 0REF polarity transitions (at frame rate) always occur in coincidence with the sync bit of 1RPCM and the logic one for 1ST is generated at the same time. One half-baud time later, 1MT (frame match time) triggers A3B. Under synchronous operation, the output (0MM) of A3B is always logic one because A3B is always in the reset state. Signal 1MMF is also present at the output of A16D since it is inverted by A16C and again by A16D. At frame sync time of each frame, nine pulses of 1SCLK are gated through shift register clock generator A4C. Positive transitions of this signal (0SHC) trigger shift registers A3A and A2, and cause the data in them to be shifted one position forward for each pulse. The OR function

of 1M0 (through A5D) and 1MMF (through A16D) is generated by A5E each bit time. This K signal is shifted into A3A by the positive transitions of 0SHC. At the same time, data bits in the input flip-flop (M7) of A2 through the output flipflop (M0) are shifted one position, so the logic / state of M1 is shifted into M0. The first shift occurs immediately after the 1MMF signal for frame sync time is generated. At this time 0ST is logic zero, the output of A5D is logic zero and the logic state of 1MMF alone is entered into the register. Succeeding 1MMF signals represent matches or mismatches for the eight data bits of 1RPCM immediately following frame sync time. After one complete shift cycle, the logic state of flip-flop M0 always represents the-logic result of the current frame sync time comparison with 0REF, since the previous state was blocked by 0ST at A5D. If either 1MMF or 1M0 is logic one (mismatch), 1M8 is logic one after the shift pulse; but if both 1MMF and 1M0 are logic zero (match), 1M8 is logic zero after the shift pulse. Since the halt gage output signal (OHALT) is logic one (f below) the AND gate input of A2 permits inward shift of data at 0SHC pulse time when 1M8 is logic one (mismatch). Thus, logic ones in the register (representing mismatches) are cumulative because the OR function in the recirculating path assures that a logic one will be reentered. When the next frame sync time occurs, signal 0SHC again shifts match or mismatch data into A3A and A2. This procedure repeats each frame with the probability that all flip-flops M1 through M7, will have logic ones stored.

f. Nonsynchronous Operation (12-Channel). It must be remembered throughout the following discussion that two sync times are under consideration. The time when sync bits occur in signal 1RPCM is always referred to as sync time. Frame sync time signal (1ST) of 1A12A10 and 1A12A12 occurs at the same time as sync bits of 1RPCM (sync time) under synchronous operation, but under asynchronous operation, it does not. Frame sync time always refers to the signal of control processor 1A12A10 and 1A12A12 and is used as an assumed sync time which may or may not be synchronous with true sync time. If loss or interruption of the 1RPCM signal occurs, the location of the sync bit is unknown when the 1RPCM signal is restored. True sync time of the 1RPCM signal will probably not occur in coincidence with OREF and 1ST (frame sync time) signals of 1A12A10. The inverse exclusive-OR gate detects mismatches at sync time about 50 percent of the time when it is sampling data bits instead of the sync bit. The output of mismatch flip-flop A3B, therefore, is random logic ones and zeros, varying according to the pcm data. This output signal causes pulse decoder 1A12A11 to supply logic ones for input signals 1SL and 1SM at 1A12A100. This provides two logic one inputs to halt gate A12. On the next transition of OREF, signals 1X1 and 1X3 become logic one and halt gate A12 has a logic one at all inputs except 1TA (pin 5) and 1M8 (pin 9).

The logic zero (match) or logic one (mismatch) at the output of A5E, resulting from comparison of the first bit of 1RPCM following the transition of 0REF, is shifted into A3A by the first pulse of 0SHC. Remember that 1M0 is blocked at A5D at this time because 0ST is logic zero during the first pulse of 0SHC, therefore, the signal shifted into A3A is derived from 1MMF alone. If 1M8 is logic zero at this time, the following eight pulses of 0SHC shift data out of A2. These are all logic ones (e above), and 1M8 remains at logic zero and a half cannot start. At the termination of 0SHC pulses, flip-flop MO (which stores the sync time data) has a logic zero (match) stored. At frame sync time of following frames the process just described repeats, that is, the logic state of A5E for frame, sync time is shifted into A3A (while 1M0 is blocked). The next time that a mismatch is detected at frame sync time (1MMF is a logic one), 1M8 goes to logic one. But at the same time that the new logic state of 1M8 is generated 1TA goes to logic one. Now all inputs to halt gate A12 are logic one and the output (OHALT) goes to logic zero. The 0HALT signal applies a logic zero at the AND gate inputs of counter A18. When the J and K inputs of a J-K flip-flop are both logic zero, the output does not change with trigger signals. So the output of A18 and all signals derived from 1SCLK (except 0SHC) remain in the same logic state until the halt condition ends. The logic states of all clock derived signals are known when the halt occurs since a halt can start only at the end (trailing edge) of 1ST (frame sync time) ((6) above). See figure 1-12 and note the logic state of the following signals at the end of 1ST. The 0ST signal is logic one and remains in that state since the 0TA, 1X1 and 1X3 signals are fixed at logic one. 1ST and 1MT are fixed at logic zero. With 1X3 and 1X6 fixed at logic one, 1SCLK signals (which are not affected by the halt) are gated through shift register clock generator A4C to generate 0SHC. Since 1X3 and 1X6 are fixed at logic one, 0SHC pulses continue as long as the halt condition exists, instead of being cut off after nine

pulses. As explained above, the halt starts at the end of frame sync time when 1M8 becomes logic one (mismatch). The following eight pulses of 0SHC shift data out of A2. 0ST is at logic one, so data logic ones can go through A5D. Since all data in A2 will be logic one (because it was assumed that this halt started after a long run of synchronous operation), the output of A5E will be logic zero for these eight pulses of 0SHC. During halt time, 0HALT is logic zero, so the AND gate input of A2 is inhibited and no new data is shifted into registers M7 through M0. After the ninth pulse of 0SHC, 1M0 remains logic zero. From the tenth pulse of 0SHC onward, 1MMF is the only active input to A5E. The first time 1MMF goes to logic zero, 1M8 goes to logic zero (match), and 0HALT returns to logic one. This ends the halt, and clock derived signals return to normal operation. The probability that a match will occur at any frame sync time is 50 percent; the probability of at least one match in two successive frames is 75 percent; and for three successive frames, it is 88 percent. Thus, the probability that the halt will end after very few frames is high. Assuming it ends after three frames, the bit time of 1RPCM which provided a match and ended the halt is the new frame sync time. The AND gate input of A2 is no longer inhibited, therefore, the match/mismatch data for the next eight bits of 1RPCM is shifted into A2 and A3A by 0SHC. The control processor is now operating as if synchronous operation had been reestablished. If the new frame sync time does not occur in coincidence with the true sync time of 1RPCM, signal 0MM will be logic zero about 50 percent of the time instead of logic one all the time. Signal 0MM then causes pulse decoder 1A12A11 to maintain signals 1SM and 1SL is at logic one. The next time 1MMF is logic one at frame sync time, a new halt is started. Assume this halt starts two frames after the end of the previous halt. Then match/mismatch data for the eight bits of 1RPCM following frame sync time is stored in the shift registers, as accumulated for two frames. During the halt, data from the shift registers is recirculated and the OR function of the recirculated data. with 1MMF (each bit time) is again entered at A3A (M8). The first time the OR function provides a match, signal 1M8 goes to logic zero and the halt ends. Assuming that this occurred for the data originally stored in M4 (when it is recirculated to M8) the new frame sync time is then advanced four bit times. If this new frame sync time does not coincide with true sync time, another halt is started, resulting in another forward shift of frame sync time. This process of selecting a bit time of 1RPCM as frame sync time; testing whether it is true sync time; rejecting it if it is not; and selecting a new frame sync time is repeated until frame' sync time coincides with true sync time.

g. Synchronous and Nonsynchronous Operation (24-Channel). When the radio set is in the 24 channel mode of operation, the bit rate of 1RPCM is 1152 kilobits per second and baud time is 868 nanoseconds and the square wave clock signal (1SCLK'), received from radio control comparator 1A12A9, is 1152 kHz. Since both data and clock rates are double (compared to the 12-channel rate) operation is the same except as noted below. The same waveforms (fig. 1-12) apply since the timing relationships are unchanged. Control processor. 1A12A10 searches for and synchronizes with the sync time of the PCM-1 signal; 1A12A12 searches for and synchronizes with sync time of PCM-2 signal. TRAFFIC SELECT switch 1A12A15A1S2 is in the 24 CHAN position and provides the required change in logic input signals to enable 24-channel operation. The changes in logic signal inputs and operating changes produced are listed in the following chart for both 12-channel and 24-channel modes of operation.

Input signal	12 channel		24 channel-	
	A12A10	1A12A12	1A12A10	1A12A12
1SCLK----------	576 kHz----------	576 kHz----------	1152 kHz----------	1152 kHz.
Pin 12----------	Logic zero----------	Logic one ----------	Logic one ----------	Logic one.
Pin 18 ----------	Logic one ----------	Logic zero ----------	Logic one ----------	Logic one.
AND gate A10B-----	Inhibited----------	Enabled ----------	Enabled ----------	Enabled.
Counter A11---------	Divide-by-two ----------	Not used ----------	Divide-by-two ---------	Divide-by-four.
Frequency 1R8 -----	8 kHz----------	Not used ----------	8 kHz ----------	8 kHz.
Frequency OREF---	4 kHz----------	Not used ----------	4 kHz ----------	2 kHz.

In 24-channel operation, signal OTE has a frequency of 16 kHz (it was 8 kHz for 12-channel ' mode), and the output of divide-by-two counter TH (A8B) at 8 kHz is now able to pass through AND gate A10B. The output of A9B (OR8) is the AND function of OTE and OTH-G, therefore, OTE / is effectively divided by two and OR8 and 1R8 are always 8 kHz. Counter A11 (TK, TL) of control processor 1A12A12 has strapping on the connector which converts it to a divide-by-four counter. The strapping connects output pin 8 to pin 11 and pin 7 to pin 14. This connects the outputs of A11A to the J and K inputs of A11B. In 24-channel mode, signal OREF (2) for control processor 1A12A10 is the same as it was for 12-channel operation. Since the sync bit pattern for PCM-1 is the same as the sync pattern for 12-channel pcm, the operation of 1A12A10 is unchanged. Signal OREF (2) in control processor 1A12A12 has a frequency of 2 kHz and a period of 500 microseconds, therefore, transitions occur every 250 microseconds. Frame time for PCM-2 is 125 microseconds and the sync pattern is 11001100, etc., for successive frames. Thus, signal OREF is logic one for 250 microseconds to match 'two successive logic ones and logic zero to match two successive logic zeros of 1RPCM.

h. Alarm Circuits. The activity detector monitors the output of the sync pattern reference generator. The output signal of the activity detector remains logic one as long as the sync pattern output signal is active. Normally all inputs to the summary alarm are logic one and the output is logic zero. Lamp DS1 is lighted. When any input changes to logic zero, the output goes to logic one (alarm condition) and lamp DS1 goes out. The output signal 1F(A)FAIL is sent to alarm monitor 1A12A6.

1-20. Pulse Decoder 1A12A1 1 Block, Diagram Description (figs. 1-13 and 8-33)

a. Pulse decoder 1A12A11 and control processors 1A12A10 and 1A12A12 operate together as a functional unit., The pulse decoder contains two framing control units: one for 1A12A10 which processes the pcm signal in the 12-channel mode or the PCM-1 signal in 24-channel mode; the other for 1A12A12 (which is not used in 12 channel mode) and processes the PCM-2 signal in 24-channel mode. b through e below describe the operation of the framing control circuit for 12 channel (or PCM-1) mode; the description is also applicable to the framing control circuit for PCM-2 since the circuits are identical.

b. The match/mismatch PCM-1 signal, OMM(1), comes from control processor 1A12A10, and is sent to sense integrator Al and search integrator A3. The voltage level of the logic signal inputs to these integrators is critical. To assure proper operation, the logic one and logic zero input signals are clamped at constant voltage levels by clamp circuit R1, CR1, CR2.

c. Input signal OMM (1) is logic one when 1A12A10 detects a match at frame sync time and remains at logic one for one frame time (125 microseconds). When a mismatch is detected at frame sync time, OMM(1) is logic zero and remains at that level for one frame time (125 microseconds). The logic state of signal OMM(1) over a period of time depends on the radio signal and on the mode of operation of 1A12A10.

(1) When the sync bit has been located and 1A12A10 is operating synchronously, signal OREF changes phase in step with the sync bit of the pcm signal; it is always logic zero when the sync bit is logic one and logic one when the sync bit is logic zero.

(2) When the sync bit of the pcm signal has not been located, 1A12A10 operates nonsynchronously and searches for the sync bit. During this time, the percentage of logic zeros in the OMM signal will be approximately 50 percent. When the sync bit is located, the search mode is continued for some time to confirm that frame sync time is in phase with true sync time.

d. The input voltage (pin 2) of sense integrator Al is 2.2 volts for logic one and 0 volt for logic zero. The basic operation of Al is that the output voltage changes at a rate proportional to the difference between the voltages at pin 1 (bias) and pin 2 (signal), and the direction of change is inversely related to the polarity of the difference. For a logic one input, the signal voltage is more positive than the bias voltage and the output voltage decreases at a rate proportional to the difference. If this condition holds long enough, the output voltage reaches maximum negative (-5v) and remains at that level. For logic zero input, the signal voltage is more negative than the bias voltage and the output voltage increases at a rate proportional to the difference. If this condition holds long enough, the output voltage reaches maximum positive (+5v) and remains at that level. The level of the bias voltage controls the operation of Al in the following way. If the bias

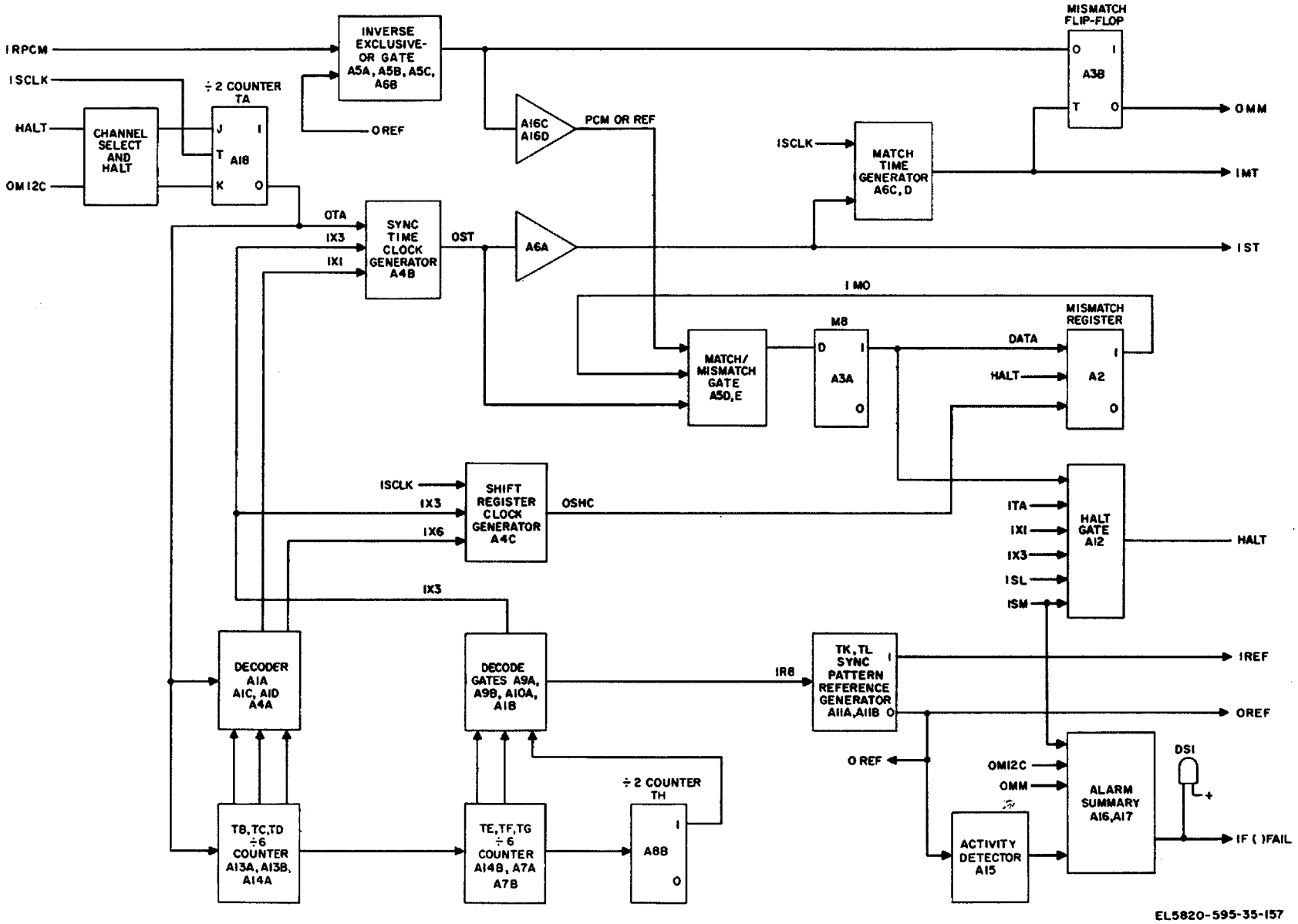


Figure 1-11. Control processor 1A12A10 and 1A12A12, block diagram.

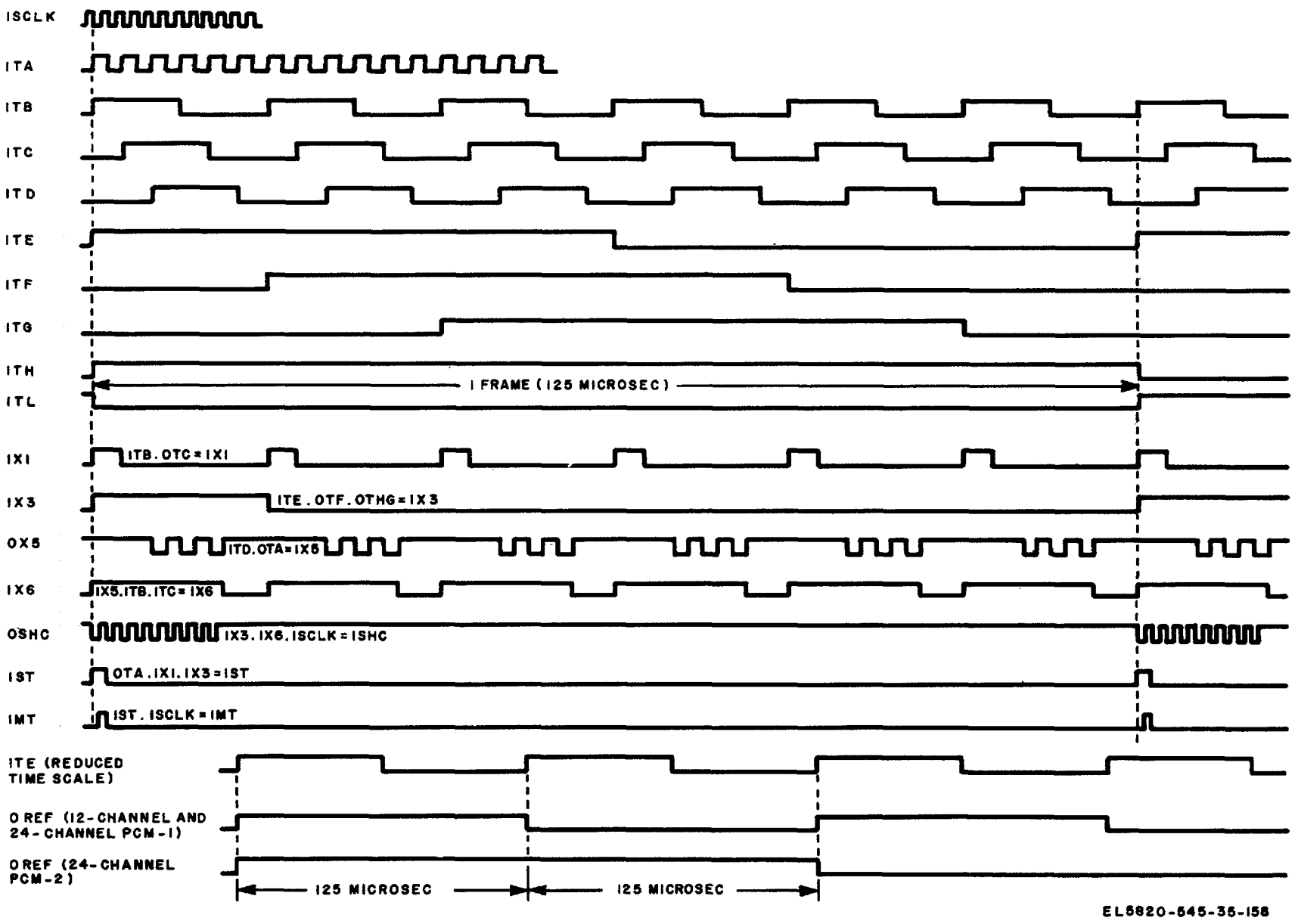


Figure 1-12. Control processor 1A12A10 and 1A12A12, timing diagram.

voltage (pin 1) is set at +1.1 volt, then for logic one (+2.2v at pin 2) input, the difference voltage is +1.1 and the output voltage decreases at a fixed rate of change. For logic zero (Ov at pin 2), the difference voltage is -1.1 volt and the output voltage increases at the same rate of change because the voltage difference is the same magnitude. In this case, the bias voltage (+-1.1v) is 50 percent of the signal voltage for logic one (+2.2v). Therefore, if the input signal, for this setting of the bias voltage, averages 50 percent logic ones and 50 percent logic zeros for a given time period, the output voltage will be at the same level at the end of the period as it was at the beginning. If the input signal is 60 percent logic ones and 40 percent logic zeros over any time period, then the output voltage is decreasing 60 percent of the time and increasing 40 percent of the time (at the same rate of change for both). If this condition holds long enough, the output voltage reaches maximum negative (-5v). In the same manner, if the input signal is 40 percent logic ones and 60 percent logic zeroes over any time period, then on the average the output voltage is decreasing 40 percent of the time and increasing 60 percent of the time (at the same rate of change for both). If this condition holds long enough, the output voltage reaches maximum positive (+5v). The turning point for the positive or negative output voltage is therefore determined by the setting of the bias voltage. This percentage is called the threshold.

e. If the bias voltage is set at two-thirds of logic one voltage, the threshold is C62/3 percent. The operation of sense integrator Al for a typical OMM(1) input signal over a period of 25 frames under this condition (662/3 percent threshold) is shown in figure 1-14. Signal OMM(1) is alternate logic one and logic zero for the first four frames. This is 50 percent logic ones and is below the threshold, so the output voltage goes positive. This is shown in the figure at the segment marked 50 percent matches. The output voltage goes positive (for mismatch) during frames 1 and 3 and it goes negative (for matches) during frames 2 and 4. The time interval (one frame time), during which the changes (increase or decrease) take place, are equal but the rate of change of voltage for matches is only 1/2 the rate of change for mismatches. As a result, the output voltage is higher at the end of frame 4 than it was at the beginning of frame 1. During the 16 frames from 9 to 25, there are 12 matches and four mismatches. This is 75 percent matches and is above the threshold, and the output voltage goes negative. This is shown in the figure at the segment marked 75 percent matches. During the 12 frames from 8 to 20, there are 9 matches and 3 mismatches, which is 662/3 percent matches and equals the threshold, therefore, the output voltage does not change. This is shown in the figure at the segment marked 662/3 percent matches, where the output voltage; at the start of frame 20 is at the same level as at the start of frame 8. The operation of sense integrator Al, as shown in figure 1-14, shows the output waveform at a time when it is close to the upper limit. At the start of frame 4, the output goes positive (for a mismatch) and reaches the upper limit at the end of frame 4. At the start of frame 5, the output voltage would go positive for the mismatch at frame 5, however, it cannot because it is at the upper limit voltage already.

f. The operation of search integrator A3 is basically the same as that for sense integrator A1. It receives the same input signal and the bias setting is the same. It is different in that its reaction time is faster as the rate of change of voltage in A3 is ten times faster than the rate of A1. When the output of A3 starts to go positive (from -5v), it switches A4 after a 1-volt rise. A1 must rise 9 volts to switch A2; this is a 9 to 1 difference. Therefore, the reaction time for A3 to switch A4 is 90 times faster than the time for A1 to switch A2.

g. When the percentage of logic ones in signal OMM is above the threshold and remains there, as it does for synchronous operation ((1) above), the output voltages of Al and A3 are at low (5v). The output signal of search mode decision circuit A2 is then logic zero and this is applied to the J input of PCM-1 sense/search mode flip-flop A6A. The output of sense mode decision circuit A4 is then logic one and this is applied to the K input of A6A. A6A receives trigger pulses (signal 1MT(l) from 1A12A10) each frame sync time. With the J input at logic zero and the K input at logic one, A6A is reset and remains reset as long as the input conditions from A2 and A4 hold. Output signal 1SM(1) is then logic zero which is sent to 1A12A10. Output signal OSM(1) is logic one and is -sent to radio digital processor 1A12A13. The output of A3 also goes to sync loss decision circuit A5. The output of A5 (1SL(1)) is then logic zero and goes to 1A12A10. (For reference, refer the time during which these conditions exist TIME A.)

h. If the percentage of logic ones in signal

OMM(1) falls below the threshold, after a period of synchronous operation as described in g above, the outputs of Al and A3 both start to go positive. The outputs of. A4 and A5 change immediately; the output of A4 goes to logic zero and the output of A5 gces to logic one. (For reference, refer to this as TIME B.) A6A now has logic zero at both J and K inputs, so it remains reset. Output signal 1SL is now logic one. The change in output at A2 is delayed with respect to the change in output at A3 because Al has a slower reaction time. If the number of logic ones' in the input signal (OMM(1)) remains below threshold, the output of Al rises to +4 volts and causes the output of A2 to go to logic one (approximately 200 frames minimum). (For reference, call this TIME C.) At TIME C, the J input of A6A becomes logic one (the K input is still logic zero). At the next frame sync time, signal 1MT(1) sets ACA and signal 1SM(l) becomes logic one, signal OSM (1) becomes logic zero.

i. During TIME B, the pulse decoder is in sense mode. TIME A ended and TIME B started when the percentage of logic ones in signal OMM(1) fell below the threshold.

(1) If the drop in the percentage of logic ones is caused by temporary fade in the radio signal, it will go above the threshold again when the radio signal returns to normal. When this occurs, the output signals of Al and A3 both start to go negative. If the input signal remains above the threshold long enough, all circuits (A1 through A5) return to the conditions of TIME A.

(2) If the drop in the percentage of logic ones is not temporary but continues, then the output of Al switches the output of A2 and the conditions of TIME C exist. This is search time. During search time, output signals 1SM(1) and 1SL(1) are at logic one. These signals are sent to control processor 1A12A10; when they are both logic one, they permit 1A12A10 to start a halt and search for sync time.

(3) The purpose of sense mode (TIME B) is to prepare to go into search mode when the signal falls below threshold but to provide a time-delay interval before going into search mode. Then, if the below threshold condition is only temporary, operating conditions return to normal (TIME A). Output signal conditions during the conditions defined above for TIME A, TIME B, and TIME C are listed in the following chart.

	Time A	Time B	Time C
A6A state	Reset	Set	Reset
A6A J input	Logic zero	Logic zero	Logic one
A6A K input	Logic one	Logic zero	Logic zero
Signal 1SM(1)	Logic zero	Logic zero	Logic one
Signal OSM(1)	Logic one	Logic one	Logic zero
Signal 1SL(1)	Logic zero	Logic one	Logic one

1-21. Radio Digital Processor 1A12A13 Block Diagram Description (figs. 8-7 and 8-34)

a. The radio digital processor logic circuits correct the frame sync code(s) and change the timing of the pcm signal to the bit rate (2304 kHz) required by the cable system. The incoming pcm signal (1RPCM) passes through four similar logic switch circuits and is applied to the retiming flip-flop A1B.

b. The first switch logic circuit (A5A, A5B, A5C, and A6A) is controlled by signal ORRFAIL received from alarm monitor 1A12A6.

(1) ORRIFAIL is normally logic one enabling AND gate A5A and inhibiting AND gate A5B by the logic zero from A6A. Signal 1RPCM is then gated through A5A and A5C.

(2) When ORRIFAIL is logic zero, AND gate A5A is inhibited and gate A5B is enabled. Signal 0R288 from flip-flop A1A is then gated through A5B and A5C. Signal OR288 is equivalent to 1010 at the 12-channel bit rate and to 1100 at the 24-channel rate. One baud time at 12 channel rate is one-half cycle of 0R288; two cycles of OR288 give 1010.... Two baud times at 24-channel rate is one-half cycle of OR288; one cycle of 0R288 gives 1100.... Refer to e(4) and f below.

c. The second logic switch circuit (A5D, A5E, A5F, A6B and A7A) substitutes the frame reference sync for the sync bit of PCM-2 when signals 1ST (2), OSM (2) and OM12C are logic one. A logic one on the OSM (2) input indicates that signal OREF (2) represents the correct sync code regardless of bit errors on the received signal. Signal OREF (2) is substituted for the pcm sync bit. In this way, the frame sync code is made error-free, even when the bit error rate of the PCM signal is high. When the specified conditions exist, all inputs to A6A are logic one at sync time, and the output is logic zero. Thus, at sync time, A5D is inhibited; A5E is enabled, blocking the pcm sync bit at A5D and substituting OREF (2) through A5E. When control processor 1A12A12 is in search mode, signal OSM (2) is logic zero, the

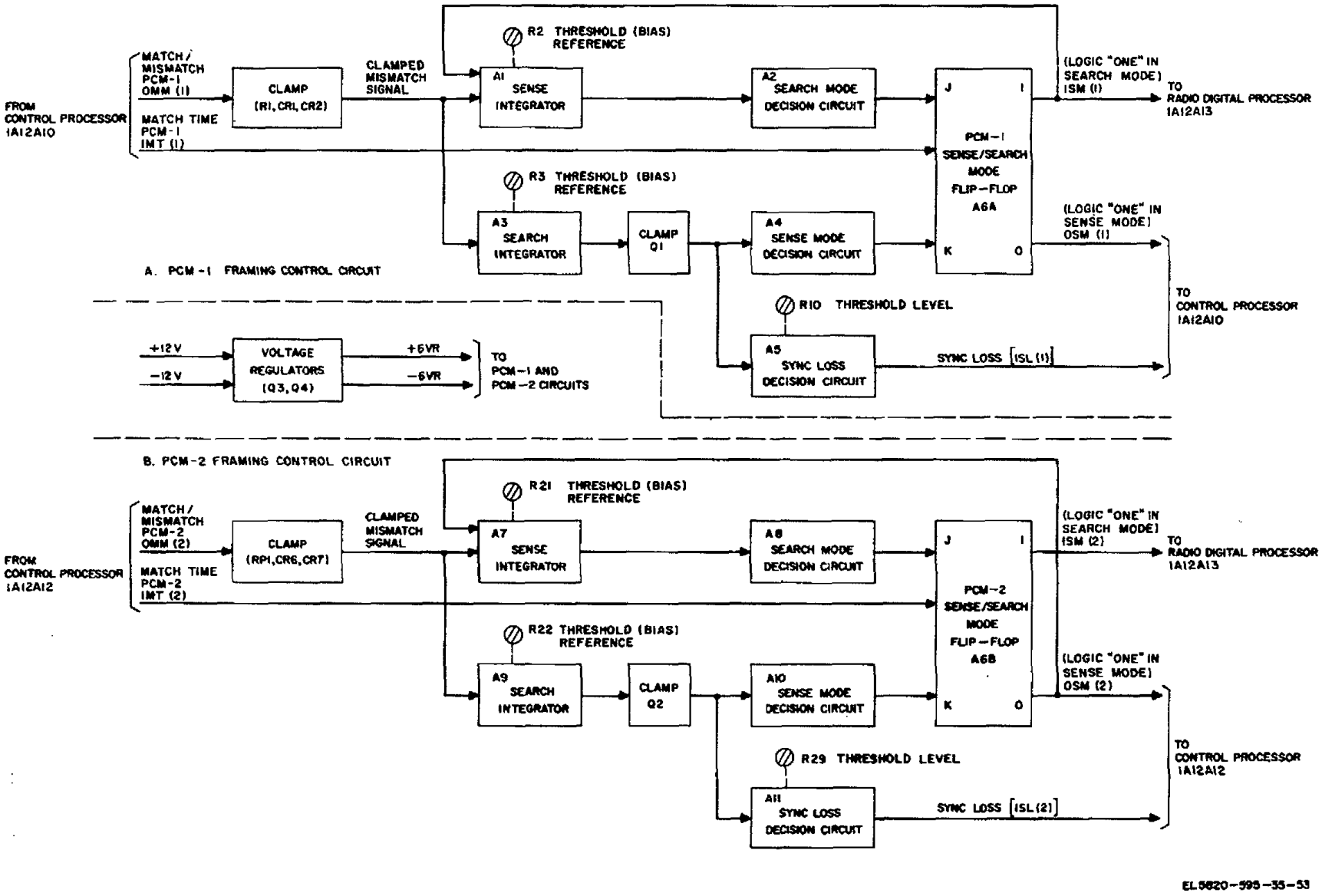


Figure 1-13. Pulse decoder 1A12A11, block diagram.

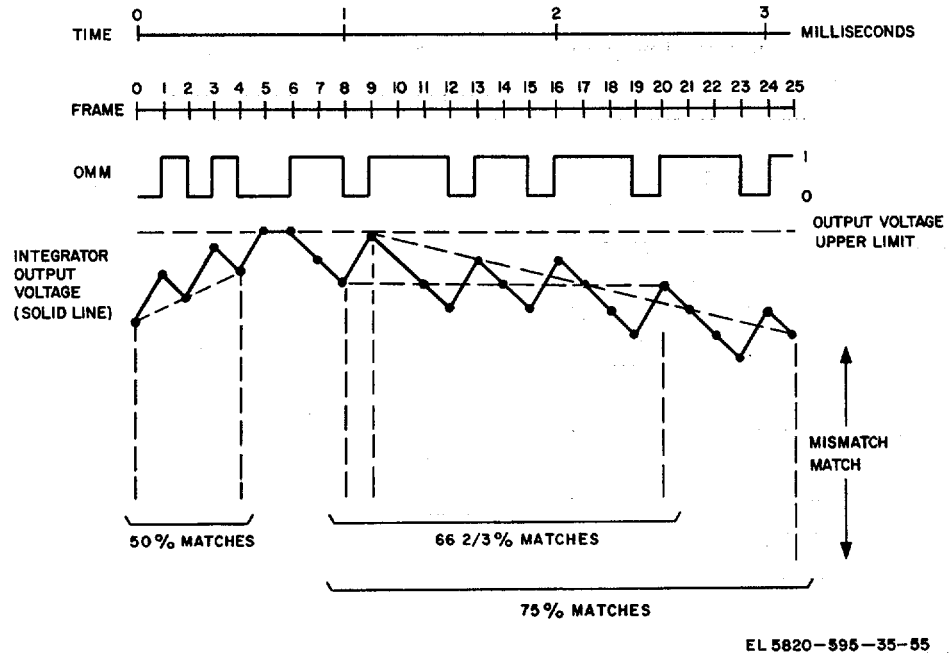


Figure 1-14. Pulse decoder 1A12A11, graph of integrator operation.

output of A7A then remains at logic one. The pcm sync bit is then gated through A5D since the relationship of sync and OREF is unknown during search mode.

d. The third logic switch circuit (A3A, A3B, A3C, A6C, and A6D) corrects the frame sync code of the PCM-1 group in a similar manner as frame sync code correction is provided for PCM-2 by the second logic switch. The third logic switch circuit is activated for both 12- and 24-channel operation.

e. The fourth logic switch circuit (A3D, A3E, A3F, A4A, and A4B) changes the 12-channel signal to half-baud and inserts alternate logic ones and zeros (dummy pulses) in the other half-baud.

(1) In 12-channel mode, signal 1M12C is logic one which gates 0R576 through A4A. OR 576 is logic one for 868 nanoseconds and logic zero for 868 nanoseconds. These two total 1736 nanoseconds which is the baud time of the pcm signal in 12-channel mode (waveforms A, B, and C, fig. 1-15). Therefore, the input signals to A3E are both logic one for only half-baud, and the output signal is a half-baud logic one whenever the input pcm bit is logic one. This is half-baud at the 12 channel rate, but it is full-baud at the 24-channel rate. Signals 0R576 and 0R288 are combined in AND gate A3D, and the output signal is a logic one every fourth baud time (at the 24-channel rate) (waveforms D, E and F, fig. 1-15). The outputs of A3E and A3D are combined in A3F (waveform G, fig. 1-15). The output of A3F is the pcm signal with alternate logic ones and zeros inserted between data pulses. This output signal is retimed by flip-flop A1B. Waveform J (which is the same as G) is marked to identify pcm and dummy bits at the 24-channel rate.

(2) When in 24-channel mode, signal 1M12C is logic zero, A3D is inhibited and supplies a constant logic zero to A3F. At the same time, A3E has a constant logic one input at pin 11 so its output is the 24-channel pcm signal.

(3) Thus, for either 12 or 24-channel mode of operation, the output of A1B is at 24-channel rate. In 24-channel mode, the pcm bits are alternate PCM-1 and PCM-2; in 12-channel mode, the pcm bits correspond to PCM-1 and the alternate logic one and logic zero dummy bits correspond to PCM-2.

(4) When signal 0R288 has been substituted for the pcm signal (b(2) above) in 12-channel mode, the action of the 4th switch changes the bit sequence 1010 . .. to 11001100.... This is the same sequence as the 24-channel pattern produced by 0R288.

f. When CABLE LOOP TEST switch (1A12A15A1S1) is in the NORMAL position, both OTEST and OCLPCM are logic one. The pcm signal (1152 kilobit/second) and 1R2304 (2304 kHz) are combined in AND gate A7B which in effect doubles the data bit rate and cuts baud time in half (waveforms J, K and L, fig. 1-15). The output at A7B is inverted by A4D (waveform M). There are two consecutive' logic one bits in the output signal of A4D for each one bit in the pcm input to A7B (waveform J). For comparison, the original pcm signal, waveform N, is shown next to waveform M. When the CABLE LOOP TEST switch is in the TEST position, AND gate A7B has a logic zero at pin 6 and the pcm signal from the radio is cut off. Instead, the incoming cable pcm signal, OCLPCM, is transmitted through pin 13 at OR gate A4D. Generator A2 precisely times the pcm signal and A4C inverts the output.

g. When signal OR288 has been substituted for the pcm signal (b(2) above), the bit sequence 11001100. .... (b(4) above) is doubled by the action of A7B and changes to 1111000011110000. . . .This constant pattern at the cable receiving station indicates a failure of the radio pcm signal.

h. In the cable-to-radio direction of transmission, the pcm signal is sent to the radio for transmission after being processed in the digital data modem. This signal, inverted (OCLPCM from cable digital processor 1A12A4), is applied to radio digital processor 1A12A13. When the CABLE LOOP TEST switch 1A12A15A1S1 is placed in the TEST position, this from cable signal is substituted for the from radio pcm. signal. Thus, under the test-condition, the signal from the cable is returned directly to the cable as a means of testing the cable system.

i. The pcm signal is amplified by cable output amplifier Q1 and transformer coupled to the cable circuit and the traffic detector.

(1) There are three cable simulation networks; each network provides attentuation equivalent to 1/4 mile of cable. They are added in the required increments to make the total length of actual and simulated cable equal 1 mile. A selector plug connects the required networks and also makes a connection to the applicable CABLE LG (MILES) indicators on the front panel. A similar arrangement is provided for cable digital regenerator 1A12A2 such that when both special connectors are plugged in to simulate the same length of cable, the associated CABLE LG (MILES) indicator is illuminated.

(2) At the secondary side of transformer T1, the pcm signal is combined with the order wire signal and the cable dc current. The overvoltage shunt circuit protects circuits of radio digital processor 1A12A13 against input voltage surges from the cable.

(3) The radio digital processor traffic detector circuit generates signals ONOR and 1RPFAIL.

When the radio-to-cable pcm signal output from flip-flop A1B is normal, the pcm signal is gated through A7B and following circuits into the secondary of T1. Signal ONOR output from the traffic detector is then logic one, signal 1RPFAIL is logic zero, and the radio-to-cable pcm signal is transmitted through the cable. If the CABLE LOOP TEST switch is then placed in TEST position, the pcm signal is inhibited at A7B (logic zero at pin 6) but signal OCLPCM is gated through A4D. Signals ONOR and 1RPFAIL are the same as above but now the cable loopback pcm signal is sent to the cable. When the radio-to-cable pcm signal fails, if the CABLE LOOP TEST switch is in NORMAL position, there is no pcm signal into T1. Signal ONOR switches to logic zero and signal 1RPFAIL switches to logic one (traffic failure). There is no pcm Signal in the cable. If the CABLE LOOP TEST switch is then placed in TEST position, signal OCLPCM is gated through A4D. Signal ONOR is logic one, signal 1RPFAIL is logic zero and the cable loopback pcm signal is sent to the cable. The logic state of signal ONOR affects operation of relay 1A12A12A2TB1K1 (para 1-54b).

1-22. Order Wire Assembly 1A13 Block Diagram Descriptions

Operational or maintenance activities between the distant radio station, the radio set, and terminal equipment (through order wire) are provided by a single order wire channel operated on a party line basis. Order wire assembly 1A13 provides duplex telephone communication between the order wire stations by interconnecting signals from four different sources. These four sources are the local handset, the remote telephone, the, radio equipment (transmitter order wire output and recovered order wire or order wire, pcm bypass inputs) and the through order wire (TO CABLE output and FROM CABLE input). Order wire assembly' 1A13 also provides alarm monitoring circuits, an input to a speaker monitor, inband signaling at 1.6 kHz, a 1.l-kHz test tone,

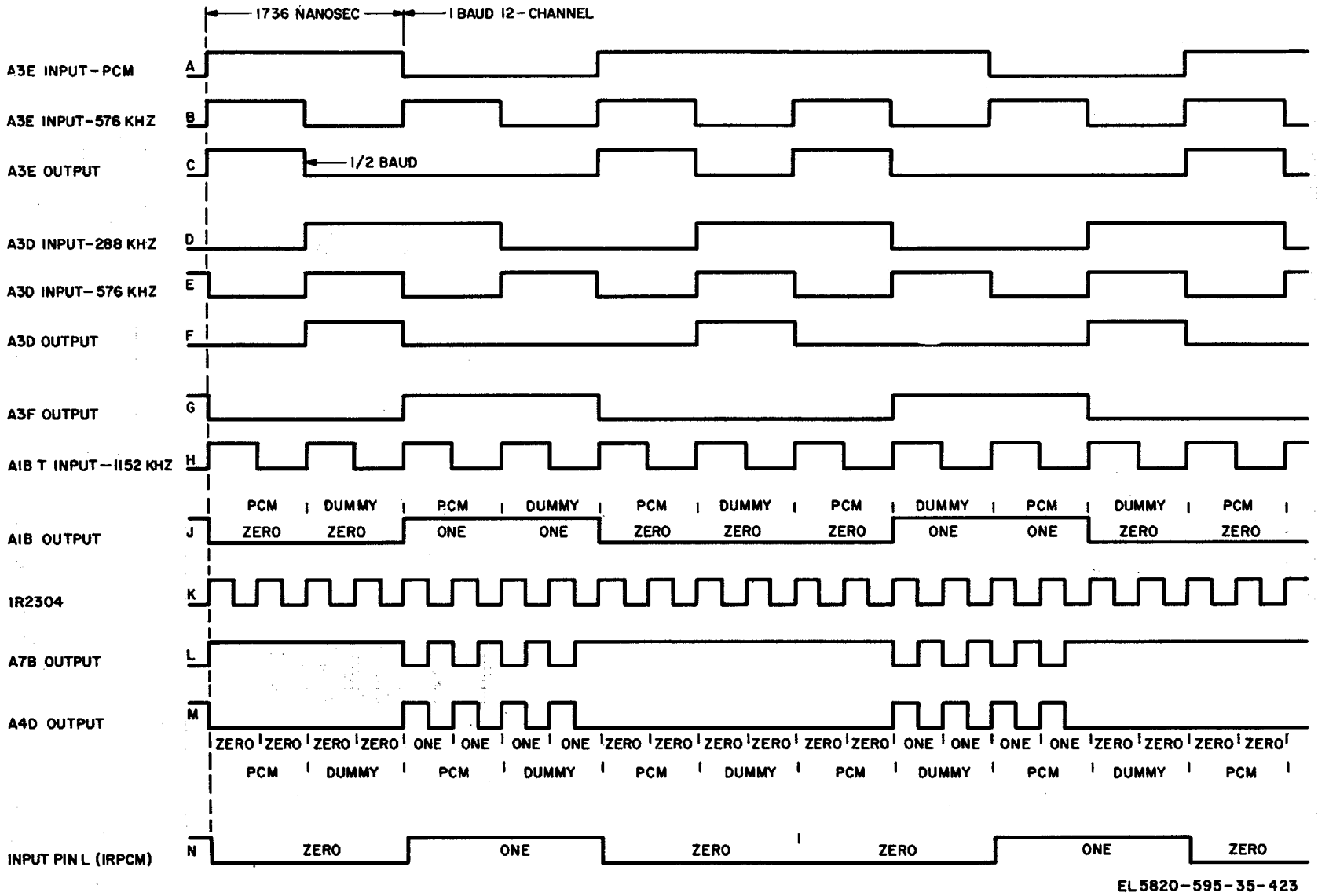


Figure 1-15. Radio digital processor 1A12A13, timing diagram.

and order wire module fault detection circuits. These circuits are described in paragraphs 1-23 and 1-24. The order wire assembly is comprised of five daughter boards and chassis mounted components. The daughter boards contain both discrete components (transistors, resistors, etc.) and integrated circuits (IC's).

1-23. Order Wire Signal Distribution B lock Diagram Description (fig. 8-8)

a. Signal distribution through order wire assembly 1A13 is illustrated in figure 8-8. Duplex (transmit and receive) order wire signal paths connecting the distant radio, radio set, and Ale terminal equipment are shown. Through order wire receive (FROM CABLE), recovered order wire, order wire (pcm bypass), local handset, and remote telephone input signals are shown entering the order wire assembly on the left-hand side of the diagram. Through order wire transmit (TO CABLE), transmitter order wire, handset receive, and remote telephone output signals are shown leaving the order wire assembly on the right-hand side of the diagram. The through order wire receive (FROM CABLE) input signal is received by cable from the terminal equipment and the through order wire transmit (TO CABLE) output signal is sent by cable to the terminal equipment. The recovered order wire or order wire (pcm bypass) input signal is received by the antennas and radio receiver from the distant radio station and the transmitter order wire output signal is sent by the transmitting circuits, power amplifier, and antenna to the distant radio station. The internal order wire connections are such that a signal originating at one of the four inputs is fed out to the other three outputs, but not to the associated output. For example, the through order wire receive (FROM CABLE) input signal is fed out to the transmitter order wire, local handset, and the remote telephone signal outputs but not to the through order wire transmit (TO CABLE) output.

b. To illustrate signal distribution through the order wire assembly, assume that a signal is applied from the remote telephone output. The signal passes through hybrid transformer 1A13A7TB1T1 and peak limiter B (integrated circuit A3) on board No. 5 1A13A5 and is distributed as follows:

(1) To the speaker through IC amplifier A2 on board No. 4 1A13A4, the speaker volume control on the meter panel and IC amplifier A2 on board No. 2 1A13A2.

(2) To the local handset receive through IC amplifier A2 and filter FL1 on board No. 4 1A13A4.

(3) To the transmitter through IC amplifiers A5 and A4, filter FL1 and transformer T1, on board No. 5 1A13A5.

(4) To the through order wire transmit '(TO CABLE) through IC amplifier A5 on board No. 5 1A13A5, and IC amplifier. A1, filter FL1, and transformer T1 on board No. 3 1A13A3.

c. Assume that a signal is applied from local handset output. The signal is applied to peak limiter A (integrated circuit A2) and to sidetone amplifier Q2 on board No. 5 1A13A5. The output of sidetone amplifier Q2 is applied to the local handset's receive element to provide sidetone. The signal output of peak limiter A is distributed-

(1) To the remote telephone through IC amplifier A2 and filter FL2 on board No. 3 1A13A3, and hybrid transformer 1A13A7TB1T1.

(2) To the through order wire transmit (TO CABLE) through IC amplifier A5 on board No. 5 1A13A5, and IC amplifier Al, filter FL1, and transformer T1 on board No. 3 1A13A3.

(3) To the transmitter via IC amplifier A5 and A4, filter FL1, and transformer T1 on board No. 5 A13A5.

d. Assume that the terminal equipment pcm and order wire signal with the pcm signal removed by the digital data modem is applied to the through order wire (FROM CABLE) input. The signal is distributed-

(1) To the speaker through transformer T1 and IC amplifiers Al and A2 on board No. 4 lA13A4, the speaker volume control on the transmitter meter panel, and IC amplifier A2 on board No. 1A13A2.

(2) To the local handset receive through transformer T1, IC amplifier Al and A2, and filter FL1 on board No. 4 1A13A4.

(3) To the transmitter through transformer 1A13A4Tl, and IC amplifier A4, filter FL1, and transformer T1 on board No. 5 1A13A5. (4) To the remote telephone through transformer T1 and IC amplifier Al on board No. 4 1A13A4, IC amplifier A2 and filter FL2 on board No. 3 1A13A3, and hybrid transformer 1A13A7TBlT1.

e. For normal operating conditions, relay K1 on board No. 3 1A13A3 is energized, allowing the

recovered order wire signal (the order wire signal from the distant radio station) to enter the order wire circuits. However, if the recovered order wire sensing signal is lost (pcm alarm condition), relay K1 becomes deenergized and the order wire (pcm bypass) signal will enter the circuits to maintain order wire communication. In either case, the recovered order wire signal or order wire (pcm bypass) signal passes through contacts of relay K1 on board No. 3 1A13A3 and is distributed-

(1) To the speaker through IC amplifiers A1 and A2 on board No. 4 1A13A4, the speaker volume control on the meter panel, and IC amplifier A2 on board No. 2 1A13A2.

(2) To the local handset receive through IC amplifier Al and A2, and filter FL1 on board No. 4 1A13A4.

(3) To the remote handset through IC amplifier Al on board No. 4 1A13A4, IC amplifier A2 and filter FL2 on board No. 3 1A13A3, and hybrid transformer 1A13A7TBlT1.

(4) To the through order wire transmit (TO CABLE) through IC amplifier Al, filter FL1, and transformer T1 on board No. 3 1A13A3.

f. The 1.6-kHz monitor (integrated circuits A3 and A4) on board No. 4 1A13A4 detects the inband signaling tone (1.6 kHz) when it is present on any of the inputs causing relay K1 on board No. 4 1A13A4 to become energized. With K1 energized, the signal is directed to the speaker passing through IC amplifiers (Al and/or A2) and contacts of relay K1 on board No. 4 1A13A4 and IC amplifier A2 on board No. 2 1A13A2. Note that with K1 energized the speaker volume control is bypassed. Energizing K1 also changes the RING indicator color from green to red.

g. Signaling tone is generated locally by pressing the RING pushbutton located on the transmitter meter panel. When the RING pushbutton is depressed, ground is applied to the 1.6-kHz oscillator (Q1) on board No. 5 1A13A5 causing oscillations and making 1.6: kHz tone available at the output of the oscillator. The 1.6-kHz oscillator tone is distributed through IC amplifier Al on board No. 5 1A13A5-

(1) To the speaker through closed contacts of the RING switch, peak limiter B (integrated circuit A3) on board No. 5 1A13A5, IC amplifier A2 and closed contacts of relay K1 on board No. 4 1A13A4, and IC amplifier A2 on board No. 2 1A13A2.

(2) To the speaker through emitter follower Q5 and IC amplifier A2 on board No. 2 1A13A2.

(3) To the local handset receive through closed contacts of the RING switch, peak limiter B (integrated circuit A3) on board No. 5 1A13A5, and IC amplifier A2 and filter FL1 on board No. 4 1A13A4.

(4) To the remote telephone through emitter follower Q4 on board No. 2 1A13A2 and hybrid transformer 1A13A7TBlT1.

(5) To the transmitter through closed contacts of the RING switch, and peak limiter B and IC amplifier A5, A4, and filter FL1, and transformer T1 on board No. 5 1A13A5.

(6) To the through order wire transmit (TO CABLE) through closed contacts of the RING switch, peak limiter B and IC .amplifier A5 on board No. 5 1A13A5, IC amplifier Al, filter FL1, and transformer T1 on board No. 3 1A13A3.

h. Test tone is generated by depressing the TEST TONE switch located on the order wire assembly front panel. When the TEST TONE pushbutton is depressed, ground is applied to the 1.1-kHz oscillator Q7 on board No. 2 1A13A2 causing oscillation and making 1.1-kHz test tone available at the output of the oscillator. The 1.1kHz test tone is amplified by IC amplifier A1 on board No. 2 1A13A2, passes through contacts of the depressed TEST TONE switch, and is distributed-

(1) To the local handset receive through the sidetone amplifier Q2 on board No. 5 1A13A5.

(2) To the remote telephone via peak limiter A (integrated circuit A2) on board No. 5 1A13A5, IC amplifier A2 and filter FL2 on board No. 3 1A13A3, and hybrid transformer 1A13A7TBlT1.

(3) To the transmitter via peak limiter A, IC amplifiers A5 and A4, filter FL1, and transformer T1 on board No. 5 1A13A5.

(4) To the through order wire transmit (TO CABLE) via peak limiter A and IC amplifier A5 on board No. 5 1A13A5, and IC amplifier A1, filter FL1, and transformer T1 on board No. 3 1A13A3.

i. OR gate circuits A and B on board No. 2 1A13A2 monitor alarm signal inputs from the receiver RCVR ALM; transmitter XMTR ALM; power amplifier P.A. ALM; and digital data modem PCM SUM ALM; A fault in the monitored equipment results in grounded alarm input to the OR gate circuits. OR gate A (CR6-CR9) controls a multivibrator circuit (Q1-Q3) and OR

gate B (CR2-CR5) controls a transistor switch (Q6). When one of the alarm input signal becomes grounded, the transistor switch is activated causing the CNTRL ALARM indication on the transmitter meter panel to change from a green to a red indication. The grounded alarm input signal also activates the multivibrator circuit (Q1-Q3). When activated, the multivibrator alternately triggers the 1.1-kHz oscillator Q7 on board No. 2 1A12A2 and the 1.6-kHz oscillator Q1 on board No. 5 1A12A5 into operation. The 1.1-kHz oscillator is connected to the 1.6-kHz tone output of the 1.6-kHz oscillator via contacts of the TEST TONE and RING switches. The alternating 1.1/1.6-kHz tone is distributed to the speaker on the meter panel and to the remote telephone to provide an audible indication that a fault has occurred. The 1.1/1.6-kHz tone is distributed to the speaker via emitter follower Q5 and IC amplifier A2 on board No. 2 1A13A2. The 1.1/1.6kHz tone is distributed to the remote telephone via emitter follower Q4 on board No. 2 1A13A2 and hybrid transformer 1A13A7BlT1. Momentarily depressing the RESET switch on the transmitter panel or an external AUDIBLE ALARM DISABLE switch (shelter mounted) silences the speaker alarm by disabling the multivibrator. The CTRL, ALARM indicator on the transmitter meter panel remains lighted red indicating a fault still exists. The CNTRL ALARM indicator will turn green only after the fault is removed.

1-24. Order Wire Module Fault Detection Block Diagram Description (fig. 8-9)

a. The module fault detection circuits are illustrated in figure 8-9. The module test circuits and the modules tested are shown. The test circuits consist of MODULE TEST selector switch 1A13A1S1, 4.02-kHz oscillator 1A13A1Q1 and IC amplifier 1A13A1A1, 4.02-kHz monitor 1A13A1Q2 and IC amplifier 1A13A1A2, transformer 1A13A1Tl, and light switch assembly 1A13A1S2 which contains the MODULE TEST monitor indicator. Figure 8- is arranged for left to right signal flow with the module test input circuits on the left and the output circuits on the right.

b. With the MODULE TEST selector switch set to position 1, the module fault detection circuits are tested. The output of the 4.02-kHz oscillator is connected to the 4.02-kHz monitor through contacts S1E-1 and S1E-5 of the selector switch and contacts of the MODULE TEST indicator press to-test switch. The 4.02-kHz monitor converts the 4.02-kHz signal into a dc output voltage which biases the lamp driver in light switch assembly 1A13A1S2 off. With the lamp driver biased off, the MODULE TEST indicator is extinguished indicating that the fault detection circuits are operating normally. Depressing the MODULE TEST indicator (press-to-test), grounds the 4.02kHz monitor input thus removing its output voltage. This cases the lamp driver to be biased on and the MODULE TEST indicator conducts and glows red.

c. To test IC amplifier 1 (1A13A5A5), the MODULE TEST selector switch is set to position 2, connecting the 4.02-kHz oscillator output signal through selector switch contact SIC-2 to one input of IC amplifier 1. This signal is designated +4.02 kHz. The 4.02-kHz oscillator output signal is also connected through transformer T1 and selector switch contact S1D-2 to the other input of of amplifier 1. Transformer T1 reverses the phase of the signal which is designated-4.02 kHz., The output signal level of amplifier 1 is applied through selector switch position SIB-2 and MONITOR TEST switch S2 to the 4.02 kHz monitor Q2. If the output signal level of amplifier I is normal, the lamp driver is biased off. Thus, the MODULE TEST indicator is extinguished indicating amplifier 1 is operating normally. However, if the output signal level of amplifier 1 is low, the 4.02-kHz monitor cannot develop a dc voltage sufficient to bias the lamp driver off. With the lamp driver biased on, the MONITOR TEST indicator lights indicating that amplifier 1 is defective.

d. Amplifiers 2 through 6, the peak limiters, and the speaker amplifier are tested in the same manner as described above for amplifier 1. The selector switch positions and input and output contacts associated with each test are listed below.

Module test selector switch-(S1) position	Input selector switch contacts		IC circuit	Output selector switch contacts
	+4.02 kHz	-4.02 kHz		
3	S1C-3----------	S1D-3 ----------	Amp 2 (1A13A3A2) ----------	S1B-3.
4	S1C-4 .----------	S1D-4----------	Amp 3 (1A13A3A1) ----------	S1B-4.
5	S1C-5 ----------	S1D-5----------	Amp 4 (1A13A4A1)----------	S1B-5.
6	S1C-6- ----------	S1D-6----------	Amp 5 (1A13A5A4) ----------	SB-6.
7	S1C-7 .----------	S1D-7----------	Amp 6 (1A13A4A2) ----------	S1B-7.
8	S1C-8 ----------	S1D-8----------	Peak Limiters (1A13A5A2 and A3) ----------	S1B-8.
9	S1C-9 ----------	None----------	Speaker Amp (1A13A2A2) ----------	S1B-9.

e. To test the 1.6-kHz oscillator (1A13A5Q1), the MODULE TEST selector switch is set to position 10 which connects ground to the oscillator input via S1E-2 and S1E-10. With its input grounded the oscillator starts to oscillate and provides 1.6-kHz tone output via IC amplifier 1A13A2A1. The tone signal is connected to the 1.1/1.6-kHz input of the 4.02-kHz monitor 1A13A1Q2 via emitter follower Q5 and IC amplifier A2 on board No. 2 1A13A2, and contact S1A-10 of the selector switch. If the 1.6-kHz oscillator and emitter follower Q5 are operating normally (IC amplifier 1A13A2A2 was tested for normal operation in position 9 of the selector switch), the MODULE TEST indicator should be extinguished. If the 1.e-kHz oscillator and/or emitter follower Q5 are not operating normally, the MODULE TEST indicator will light red.

f. The 1.1-kHz oscillator (1A13A2Q7) is tested in a manner similar to that described above for the 1.6-kHz oscillator except that the MODULE TEST selector switch is set to position 11. Ground is applied to the oscillator input via S1E-3 and S1E-11 causing the oscillator to provide a 1.1-kHz tone output via IC amplifier 1A13A2A1. The 1.1kHz tone signal is connected to the 1.1/1.6-kHz input of the 4.02-kHz monitor via the TEST TONE switch, emitter follower Q5 and IC amplifier A2 on board No. 2 1A13A2, and selector switch contact S1A-11.

g. To test the central alarm monitor circuit on the transmitter panel and the monitor circuit on board No. 2 1A13A2, the MODULE TEST selector switch S1 is set to position 12. Sections S1E-4 and S1E-12 applies ground to simulate power amplifier alarm input OR gates A and B on board No. 2. OR gate A triggers the multivibrator circuit Q1, Q2 and Q3 into operation. The multivibrator alternately connects ground to the 1.1-kHz oscillator inputs. The 1.6-kHz oscillator is located on board No. 5 1A13A5. The alternating output of each oscillator is coupled through the TEST TONE and RING switches and applied to the emitter followers Q4 and Q5 and speaker amplifier A2 on board No. 2. The output of A2 is applied to the monitor circuit amplifier A2 through switch section S1A-12. Monitor circuit amplifier A2 will provide an output to extinguish the MODULE TEST indicator. Alarm or gate B turns transistor switch Q6 off on board No. 2, thereby removing the operating voltage from CNTRL ALARM indicator on the transmitter meter panel. Removing the voltage changes the lamp indication from green to red for alarm condition. The emitter follower Q4 applies the 1.1/1.6-kHz tone to the meter panel speaker for an audible alarm.

1-25. Modulator Circuits Block Diagram Description (fig. 8-10)

The transmitter's modulator circuits are shown in figure 8-10. The modulator circuits consist of input circuits, modulator 1A8, and electronic frequency control module 1A7. The input circuits combined the pcm signal and order wire signals at the appropriate signal levels and apply the composite signal to modulator 1A8. The combined signal modulates a 150-MHz oscillator in the modulator (1A8). The frequency modulated 150-MHz output is applied to frequency mixer 1A9. A sample of the frequency modulated output is fed back from the modulator (1A8) to the electronic frequency control (1A7) which produces an automatic frequency control (afc) signal to stabilize the center frequency of the 150-MHz oscillator in the modulator (1A8).

a. Input Circuits. The input circuits consist of pcm attenuator assembly 1A3, AF-RF amplifier 1A4, and 1.3-MHz low pass filter 1A6.

(1) The pcm input from digital data modem 1A12 is applied to pcm attenuator and phase shift network (R1-R5, C1, C2) in attenuator assembly 1A3. The attenuator and phase shift network provides a pcm signal phase shift of 29 degrees at 300 Hz and attenuates the signal to the proper

level for application to AF-RF amplifier 1A4. To maintain separation between pcm signal and order wire, the 29 degree phase shift is required of the transmitter since the receiver phase shift is 16 degrees and the overall radio set phase shift requirement is 45 degrees at 300 Hz. The AF-RF amplifier (1A4) provides a maximum gain of 25 db. The amplifier is comprised of three stages (Q1, Q2, Q3) and is basically a shunt feedback amplifier. The TRAFFIC LEVEL ADJ control determines the input level of the pcm signal to the amplifier first stage Q1. The gain can be adjusted from maximum of 25 db to zero.

(2) The order wire input from order wire assembly 1A13 is applied to order wire attenuator network (.R6, R7, R10) and metering circuit (CR1, CR2, R8, R9, C3, C4) in pcm attenuator assembly 1A3. The attenuator network provides the proper order wire signal level for combining with the pcm signal before application to 1.3-MHz low pass filter 1A6. The order wire signal level is maintained within 15 to 20 percent of the pcm signal. The pcm output signal from AF-RF amplifier 1A4 and the order wire signal are connected together at the output of AF-RF amplifier 1A4 and form a combined signal (pcm and order wire) input to the 1.3-MHz low pass filter (1A6). The low pass filter passes the combined signal to modulator 1A8 and together with other filters in the radio set provides the required shaping.

b. Modulator 1A8. Modulator 1A8 receives the combined pcm and order wire signal and produces a frequency modulated 150-MHz output which is applied to frequency mixer lA9. A sample of the frequency modulated output is fed back from the modulator to electronic frequency control 1A7 which produces an afc signal to stabilize the center frequency of the 150-MT-Hz oscillator in modulator 1A8.

(1) The traffic input signal (combined pcm and orderwire signal) is applied to operational amplifier Al (integrated circuit). Front panel variable resistor R2 is used to adjust the traffic input level to the amplifier (A1). The amplifier traffic signal is then applied to the 150 MHz vco (Q1). The 150 MHz vco employs varactor diodes to control the output frequency. A positive-going traffic signal deviates the vco toward a lower frequency and a negative-going traffic signal deviates the vco toward a higher frequency. The vco's center frequency can be adjusted with front panel variable capacitor C15. The .150-MHz frequency modulated output of the vco is applied to amplifier stages Q3, Q4, and Q8 and Q9 via emitter follower Q2 which isolates the vco from the amplifier stages. The amplified frequency modulated 1560 MHz signal is applied through matching pad (R62-R65) to frequency mixer 1A9.

(2) The 150-MHz output signal is also applied to mixer circuit (T3, CR7, CRS) where it is mixed with a 220-MHz signal. The 220-MHz signal is developed by the 110-MHz crystal oscillator circuit (Q5) and frequency doubler circuit (T2, CR5, CR6). The output of the mixer is applied to low pass filter (L10, C38, C39). The 70-MHz difference signal produced by the mixing process is passed by the filter and amplified by stages (Q6, Q7) for application to electronic frequency control 1A7.

c. Electronic Frequency Control 1A7. Electronic frequency control 1A7 receives the modulated frequency controlled 70-MHz signal from the modulator,(1A8) and produces an afc signal to stabilize the center frequency of the 150 MHz vco in the modulator.

(1) The 70-MHz frequency controlled signal is applied to gate A (CR4-CR6) via emitter follower (Q3) inelectronic frequency control 1A7. A 70-MHz reference signal from reference oscillator circuit (Q1) is applied to gate B (CR1-CR3) via: emitter follower (Q2). The frequency of the reference oscillator can be adjusted using variable inductor L2. With switch S1 in the OPR position, free-running multivibrator (Q4, Q5) alternately switches between gate A and gate B. Thus, the 70-MHz frequency controlled signal from the modulator (1A8) and the 70-MHz signal from the reference oscillator are alternately applied to emitter follower(Q7). The emitter follower provides isolation between the gate inputs and limiter stages (QS8, Q9). The limiter stages prevent any amplitude variations from reaching the discriminator. The limiter stages are tuned by adjusting the 1ST L1M LEVEL and the 2ND L1M LEVEL controls. Emitter follower (Q10) isolates the second limiter stage from discriminator driver (Q11). Discriminator (T1, C51-C55, CR10, CR11) is a. conventional type, employing the phase shift principle. Both the primary and secondary of T1 are tuned for a linear S-curve-centered about 70 MHz. The output of the discriminator is a square wave whose amplitude is proportional to the frequency difference of the signals (70-MHz frequency controlled signal from, the modulator and 70-MHz reference signal). The difference (error) signal is applied to phase detector circuit (T2, CR12-CR15) via square wave

amplifier (Q12-Q15). The square wave amplifier is a highly stable feedback amplifier which is ac coupled both at the output and the input.

(2) The phase detector circuit receives the error signal and an input from the multivibrator to determine the polarity for plus or minus correction. When the frequency controlled input from the modulator is lower than 70 MHz, the phase detector provides a negative correction voltage output to drive the vco frequency higher. When the frequency controlled input from the modulator is higher than 70 MHz, the phase detector provides a positive correction voltage output to drive the vco frequency lower. The center frequency of the phase detector can be adjusted using variable resistor R78. Emitter follower Q6 isolates the multivibrator from the phase detector. The correction signal (afc) is applied to differential amplifier (A2-A and A2-B) in modulator 1A8. The differential amplifier increases the sensitivity of the afc output circuit. The afc signal applied to the 150 MHz vco provides ±20 kHz center frequency stability. The EFC DISABLE switch on modulator 1AS is used to disable the afc input signal. When depressed, the switch shorts out the afc input to the modulator (1A8). When aligning the vco, the EFC DISABLE switch is depressed and front panel variable capacitor C15 is adjusted.

d. Meter Circuits.

(1) The order wire metering circuit in pcm attenuator 1A3 provides an output to the meter selector switch on the transmitter meter panel. The order wire signal level may be monitored by setting the switch to the O.W. TEST position.

(2) Various signals from modulator 1A8 and electronic frequency control 1A7 are applied to the meter selector switch on the transmitter's meter panel. The traffic input to modulator 1A8 is applied through emitter follower A2-D (part of integrated circuit A2) to pcm attenuator 1A3 and then to the meter switch via alarm monitor 1A5. A variable resistor (R7) mounted on the back of the transmitter meter panel is used to calibrate the TRAFFIC meter indication. The 150-MHz output and 70-MHz frequency controlled output signals from modulator 1A8 are applied via meter circuits (CR10 and CR9, respectively), to the meter switch. The center frequency (afc signal) is applied from the output electronic frequency control 1A7 to the meter switch. Also, the afc level at the output of the limiter stages in electronic frequency control 1A7 is applied to the meter switch through meter circuit (1A7CR9). Any one of the above signals may be monitored by setting the meter switch to the desired position.

1-26. Transmitter Local Oscillator and Mixer Circuits Block Diagram Description

(fig. 1-16)

The transmitter's local oscillator and mixer circuits are shown in figure 1-14. The local oscillator circuits consist of frequency synthesizer 1A14, amplifier-frequency multiplier 1A11, 1137-1213 MHz bandpass filter 1FL5, 1137-1213 MHz circulator 1HYI, and frequency multiplier group 1A10. The local oscillator circuits produce a 4.55-to 4.85-GHz output which is applied to frequency mixer 1A9 along with the frequency modulated 150-MHz output from modulator 1A8. The mixer circuits consist of crystal mixer 1A9A1 and 4.4to 5.0-GHz circulator 1A9HY1 in frequency mixer 1A9. The frequency mixer (1A9) heterodynes the local oscillator frequency with the 150MHz signal to produce a 4.4-to 5.0-GHz output which is applied to the power amplifier via 4.4-to 5.0-GHz bandpass filter 1FL3, 5.0-GHz low pass filter 1FL4, directional coupler 1DC2, and an interconnecting cable.

a. Local Oscillator Circuits. The local oscillator circuits produce an output frequency of 4.5 to 4.85 GHz by multiplying the frequency synthesizer's output frequency by 16. Frequency synthesizer 1A14 generates a highly stable radio frequency in the range of 284.375 to 303.125 MHz, adjustable in 6.250-kHz steps. The frequency synthesizer (1A14) circuits are described in detail in paragraph 1-27. The 284.375 to 303.125 MHz, 20 milliwatt output of the frequency synthesizer is applied to amplifier-frequency multipler 1A11.

(1) Amplifier-frequency multipler 1A11 is comprised of low level amplifier stage (Q1, Q2) high level amplifier stage (Q3, Q4, Q5), and 1st frequency multiplier stage (CR4, CR5). The low level amplifier stage provides 18-20 db gain when driven with a 20-milliwatt input from the frequency synthesizer source. The low level amplifier stage has a 1 db instantaneous bandwidth of greater than 20 MHz and delivers 2-watt output power to the high level amplifier stage (Q3, Q4, Q5). The output of the low level amplifier stage is also applied through metering circuit (CR1) to the LOW PWR AMPL LEVEL ,test point on the module's front panel. The high level amplifier stage delivers about 18 watts of drive power to the 1st

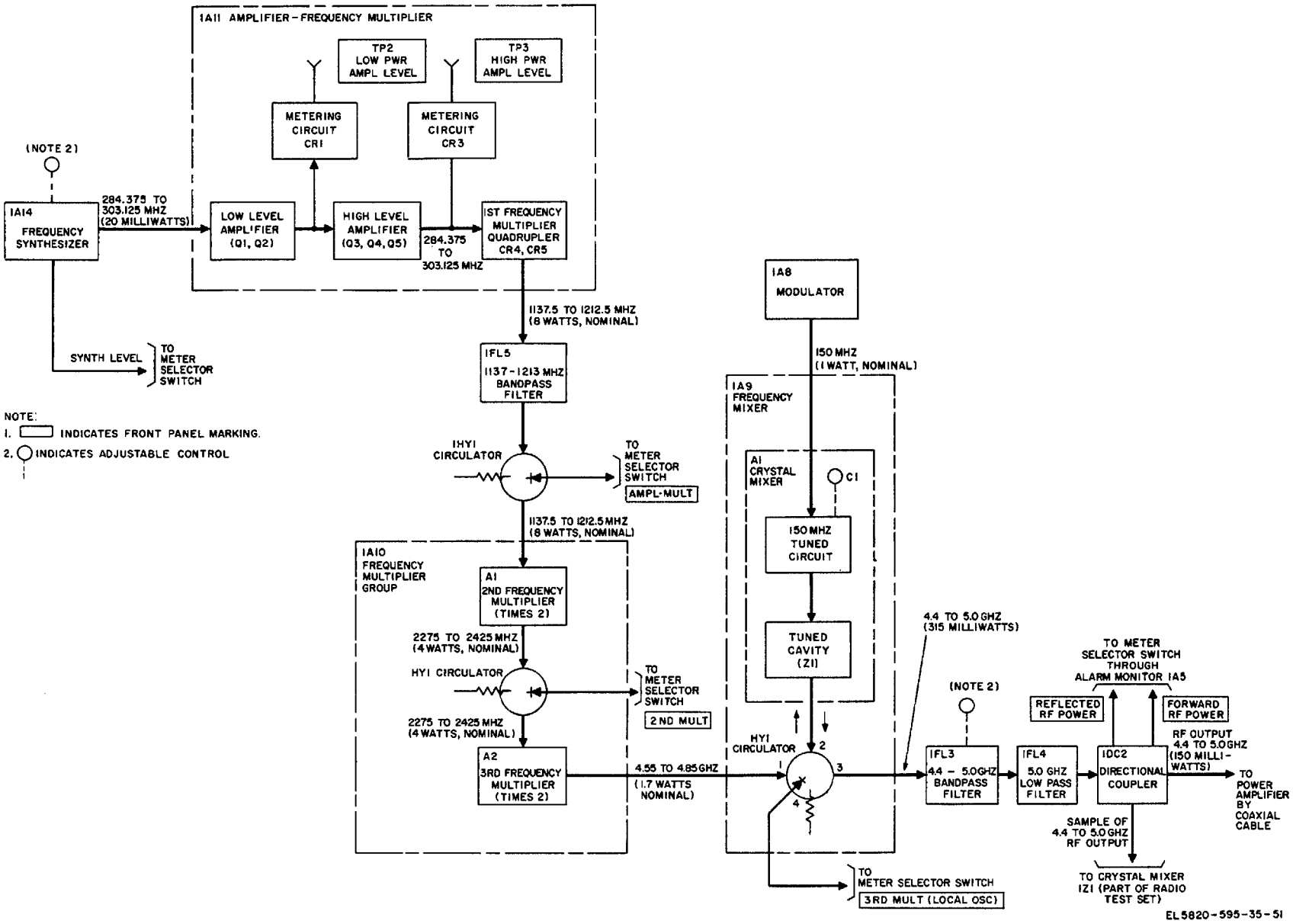


Figure 1-16. Transmitter local oscillator and mixer circuits, block diagram.

frequency multiplier stage (CR4, CR5). The high level amplifier employs a driver transistor circuit (Q3) and two power transistors (Q4, Q5) which operate in a parallel circuit arrangement to obtain the 18-watt output. The output of the high level amplifier stage is also applied through metering circuit (CR3) to the HIGH PWR AMP LEVEL test point on the modules front panel. The 1st frequency multiplier (times 4) employs two varactor doubler circuits to accomplish the times 4 multiplication. The 1137.5 to 1212.5-MHz output of the 1st frequency multiplier is at a power level of 8 watts (nominal) with spurious and related harmonic signals down 30 db (minimum). The 1137.5 to 1212.5-MHz output is applied to frequency multiplier group 1A10 via 1137 to 1213MHz bandpass filter 1FL5 and 1137 to 1213-MHz circulator 1HY1. The circulator isolates the 1st frequency multiplier stage in amplifier-frequency multiplier 1A11 from the 2d frequency multiplier stage in frequency multiplier group 1A10. The circulator also provides a sample of the 1st multiplier's output signal to the meter selector switch on the transmitter's meter panel.

(2) Frequency multiplier group 1A10 is comprised of 2d frequency multiplier 1A10A1, 2275 to 2425-MHz circulator 1A10HY1, and 3d frequency multiplier 1A10A2. The 2d frequency multiplier employs a tuned circuit, a varactor diode doubler and a tuned cavity to multiply the frequency up to 2275-MHz at 4 watts (nominal). The 2275 to 2425-MHz circulator (1A10HY1) isolates the 2d frequency multiplier stage (1A10A1) from the 3d frequency multiplier stage (1A10A2) and also provides a sample of the 2d multiplier's output signal to the meter selector switch on the transmitter's meter panel. The third frequency employs a low pass filter, a varactor diode doubler, and tuned cavity to multiply the frequency up to 4.55-4.85 GHz at 1.7 watt (nominal). The 4.55 to 4.85-GHz signal is applied to frequency mixer 1A9 where it is mixed with the frequency modulated 150-MHz signal from the modulator (1A8).

b. Frequency Mixer 1A9. The frequency mixer (1A9) translates the frequency modulated 150 MHz signal to the 4.4 to 5.0-GHz band. This is accomplished by heterodyning the local oscillator frequency (4.55-4.85 GHz) with the 130-MHz signal in a varactor type mixer. Frequency conversion is accomplished by the nonlinear capacitance-voltage relationship of the varactor diode.

(1) The frequency mixer circuits consists of crystal mixer 1A9A1 and 4.4 to 5.0-GHz circulator 1A9HY1. The 4.55 to 4.85-GHz local oscillator signal enters port number 1 of the circulator and leaves at port number 2, entering varactor cavity Z1 in the crystal mixer (1A9A1). The 150-MHz signal is applied at the opposite end of the varactor cavity via the 150 MHz tuned circuit. This circuit tunes out the varactor capacity at the 150-MHz frequency. Front panel variable capacitor C1 is used when aligning the tuned circuit. The tuned circuit also prevents RF from leaking back to modulator 1A8. The 4.55 to 4.85 GHz local oscillator fundamental frequency is suppressed in the varactor cavity by two tuned stubs producing the upper and lower band for frequency modulated 150-MHz signals. The bands (4.4-4.7 GHz and 4.7-5.0 GHz) are reflected out of the tuned varactor cavity, enter the circulator at port number 2, and leave at port number 3. The output from port number 3 is applied to 4.4 to 5.0-GHz bandpass-filter 1FL3 which is tuned to the desired carrier output signal and passes the selected carrier output signal to 5.0-GHz lot pass filter 1FLM4. The unwanted band is rejected at port number 3 and applied to port number 4 of the circulator where it is absorbed in a dummy load. The circulator also provides a sample of the 3d multiplier's output signal to the meter selector switch on the transmitter's meter panel.

(2) The 4.4 to 5.0-GHz bandpass filter 1FL3 has a bandpass of 38 MHz and is tuned to the desired frequency in the 4.4 to 5.0-GHz band by setting the filter's tuning knob to the appropriate frequency. The bandpass filter passes the desired frequency through 5.0-GHz low pass filter 1FL4, directional coupler 1DC2, and an interconnecting cable to the power amplifier unit 3. The RF power output from directional coupler 1DC2 to the interconnecting cable is 150 milliwatts. The directional coupler provides three additional outputs. Two outputs are dc levels which indicate the transmitter's forward RF power and reflected RF power. These outputs are applied to the meter selector switch on the transmitter meter pane through alarm monitor 1A5. The third output from the directional coupler provides a sample of the 4.4 to 5.0-GHz output signal which is 27 db down from the RF power output signal. This sampled signal is applied to crystal mixer 1Z1 of the radio test set.

c. Metering Circuits. Front panel monitoring of the local oscillator and mixer circuits is provided by RF detector diodes (in circulators 1HY1, 1A10HY1, and 1A9HY1), meter calibration potentiometers (1A16R4, 1A16R3, 1A16R2), the

meter selector switch, and the transmitter meter. In addition, front panel monitoring of the forward and reflected RF power at the output of the transmitter is provided by RF detector diodes (in directional coupler 1DC2), alarm monitor 1A5, the' meter selector switch, and the transmitter meter.

1-27. Frequency Synthesizer 1A14/2A21 Functional Operation

a. General.

(1) Two identical frequency synthesizers are used in the radio set. One is in the transmitter and is designated 1A14. The other is in the receiver and is designated 2A21. The transmitter and receiver local oscillator operating frequencies are derived from the associated frequency synthesizer. The frequency synthesizer generates one output signal selectable within the frequency range of 284.375 MHz to 303.125 MHz which is subsequently converted (external to the frequency synthesizer) to a radio set operating frequency within the range of 4400.0 MHz through and including 5000.0 MHz.

(2) The frequency synthesizer output frequency is selected by setting thumbwheel switches. This frequency is increased by frequency multipliers and mixers in the transmitter (or receiver) to the required final operating frequency. Thumbwheel switch settings on the frequency synthesizer are direct reading and are calibrated to indicate (in MHz) the operating frequency of the transmitter (or receiver), not the frequency synthesizer output frequency.

(3) The frequency synthesizer is an application of the phase-locked loop principle. The frequency synthesizer uses a voltage controlled oscillator (vco) to generate the frequency synthesizer output signal. The frequency of the vco is maintained with crystal oscillator frequency accuracy because it is controlled by a crystal oscillator standard (operating at 8 MHz). The output signal of the vco is returned, through a feedback network which lowers the frequency, and it is compared in phase with the crystal oscillator standard frequency. A difference in frequency between the vco signal and the crystal oscillator standard frequency is detected as a phase error. A phase error detector generates a signal which in turn adjusts the frequency of the vco as required. This feedback loop is designated a "phase-locked loop" since it locks the vco frequency in step with the crystal oscillator control frequency.

(4) The correlation between the, transmit operating frequency and the frequency synthesizer RF output frequency, the correlation between the receive operating frequency and the frequency synthesizer RF output frequency, the correlation between the thumbwheel switch settings and the frequency synthesizer's RF output frequencies, and the overall block diagram description of the frequency synthesizer are described in b through e below.

b. Correlation Between the Transmit Operating Frequency and the Frequency Synthesizer RF Output Frequency. The thumbwheel switches on frequency synthesizer 1A14 are direct reading in MHz and are set to the desired transmit operating frequency within the radio set operating range of 4400.0 MHz to 5000.0 MHz. When the thumbwheel switches are set in the 4400.0 to 4699.9-MHz range, the frequency synthesizer RF output frequency is in the 284.375 to 303.118750-MHz range. When the thumbwheel switches are set in the 4700.0 to 4999.9-MHz range, the frequency synthesizer RF output is again in the 284.375 to 303.118750-MHz range. For 5000 MHz the frequency synthesizer RF output is 303.125 MHz. The operating frequencies of the radio set (thumbwheel settings) and corresponding frequency synthesizer output frequencies for all thumbwheel switch settings from 4400.0 to 5000.0 MHz are listed in a above. The correlation between the transmit operating frequency and the frequency synthesizer RF output frequency is described below.

(1) If the thumbwheel switches on 1A14 are set to 4400.0 MHz (transmit operating frequency), the RF output frequency of 1A14 is 284.375 MHz. The 284.375-MHz signal is multiplied up to a 4550-MHz local oscillator signal by times 16 frequency multiplier circuits in the transmitter. The 4550 MHz local oscillator signal is then mixed with a 150-MHz frequency modulated signal containing the intelligence to be transmitted. Frequency selective circuits in the transmitter select the lower sideband (4550 MHz minus 150 MHz produced by the mixing process to obtain the selected 4400 MHz (4.4 GHz) transmit operating frequency.

(2) If the thumbwheel switches on 1A14 are set to 4700.0 MHz (transmit operating frequency), the RF output of 1A14 is 284.375 MHz. The 284.375-MHz signal is multiplied up to a 4550-MHz local oscillator signal and mixed with 150 MHz as described above. However, to obtain

the 4700-MHz (4.7 GHz) transmit operating frequency, frequency selective circuits in the transmitter select the upper sideband (4550 MHz plus 150 MHz).

c. Correlation Between the Receiver Operating Frequency and the Frequency Synthesizer RF Output Frequency. The thumbwheel switches on frequency synthesizer 2A21 are set to the desired receive operating frequency within the range of 4400.0 to 5000.0 MHz. The corresponding frequency synthesizer RF output frequencies are the same as described in b above. The incoming receive operating frequency is used as a mixing signal to obtain a 70-MHz IF signal containing received intelligence. The correlation between the receive operating frequency and the frequency synthesizer RF output frequency is described below.

(1) If the thumbwheel switches on 2A21 are set to 4400.0 MHz (receive operating frequency), the RF output frequency of 2A21 is 284.375 MHz. The 284.375-MHz signal is multiplied up to 4550 MHz by the times 16 multiplier circuits in the receiver. The 4550-MHz signal is then mixed with a 220-MHz signal. Frequency selective circuits in the receiver select the lower sideband (4550 MHz minus 220 MHz) produced by the mixing process to obtain a 4330-MHz local oscillator signal. The 4330-MHz signal is then mixed, with the 4400 MHz incoming signal (receive operating frequency). Frequency selective circuits in the receiver select the lower sideband (4400 MHz minus 4330 MHz) producing the required 70-MHz IF signal which contains the received intelligence.

(2) If the thumbwheel switches on 2A21 are set to 4700.0 MHz (receive operating frequency), the RF output of frequency synthesizer 2A21 is 284.375 MHz. The 284.375-MHz signal is multiplied up to 4550 MHz by times 16 multiplier circuits in the receiver and mixed with 220 MHz as described above. However, in order to obtain the correct receiver local oscillator frequency (4770 MHz), frequency selective circuits in the receiver select the upper sideband (4550 MHz plus 220 MHz). The 4770-MHz local oscillator frequency is then mixed with the 4700-MHz incoming signal (receive operating frequency). Frequency selective circuits in the receiver then select the lower sideband (4770 MHz minus 4700 MHz) producing the required 70-MHz IF signal which contains the received intelligence.

d. Correlation Between Thumbwheel Switch Settings and Frequency Synthesizer RF Output Frequencies. As previously stated, the thumbwheel switches on the front panel of the frequency synthesizer select and indicate a specific operating frequency in the 4400.0 to 5000.0-MHz range. Any frequency in this range can be selected. The frequency synthesizer RF output frequencies from 284.375 MHz to 303.11875 MHz correspond to radio set operating frequencies from 4400.0 MHz to 4699.9 MHz. This RF output frequency range (284.375 to 303.11875 MHz) is repeated for operating frequencies from 4700.0 to 4999.9 MHz. A frequency synthesizer RF output frequency of 303.125 MHz corresponds to a thumbwheel switch setting of 5000.0 MHz. Thus, the thumbwheel switches provide for the selection of 6001 different operating frequencies in 0.1 MHz steps. The 5000.0-MHz frequency down to and including the 4000.0-MHz frequency is a range of 600.1 MHz. In steps of 0.1 MHz this is 6601 separate operating frequencies. The four thumbwheel switches provide a direct reading of five digits in MHz. The first thumbwheel switch (on the left) sets the first two digits of the radio set operating frequency. The last three digits of the operating frequency are set respectively by the remaining three thumbwheel switches. The chart below lists the frequency synthesizer RF output frequency (frequency A) resulting from the thumbwheel switch settings for the first three digits of the radio set operating frequency. It also lists the additive frequency increments resulting from setting the thumbwheel switches for the remaining two digits (fourth and fifth) of the radio set operating frequency. The fourth digit additive frequency is listed as frequency B. The fifth digit additive frequency is listed as frequency C. Therefore, when the last two (of five) digits are set at a number other than zero, the frequency synthesizer RF output frequency. (F,) is the sum of frequency A and the two additive frequencies B and C (F8 = Frequency A + Frequency B + Frequency C). For example, assume that the thumbwheel switches are. set to a radio set operating frequency of 4765.9 MHz. From the chart below, the corresponding frequency synthesizer RF output frequency (F8) is calculated as follows:

Frequency A (first three digits showing 476)	= 288.125000 MHz
Frequency B (fourth digit showing 5)	= 0.312500 MHz
Frequency C (fifth digit showing .9)	= 0.056250 MHz
	F. = 288.493750 MHz

Thumbwheel switch setting-

First and second digit	Third digit	Frequency A (MHz)
44 or 47	0	284.375000
	1	285.000000
	2	285.625000
	3	286.250000
	4	286.875000
	5	287 500000
	6	288.125000
	7	288.750000
	8	289.375000
	9	290.000000
First and second digit	Third digit	Frequency A (MHz)
45 or 48	0	290.625000
	1	291.250000
	2	291.875000
	4	292.500000
		293.125000
	5	293.750000
	6	294.375000
	7	295.000000
	8	295.625000
	9	296.250000
First and second digit	Third digit	Frequency A (MHz)
46 or 49	0	296.875000
	1	297.500000
	2	298.125000
	3	298.750000
	4	299.372000
	5	300.000000
	6	300.625000
	7	301.250000
	8	301.875000
	9	302.500000
50	0	303.125000

Thumbwheel switch setting		Thumbwheel switch setting	
Fourth digit	Frequency B (MHz)	Fifth digit	Frequency C (MHz)
0	0.0000	0	0.000000
1	0.062500	1	0.006250
2	0.125000	2	0.012500
3	1.187500	3	0.018750
4	0.250000	4	0.025000
5	0.312500	5	0.031250
6	0.375000	6	0.037500
7	0.437500	7	0.043750
8	0.500000	8	0.050000
9	0.562500	9	0.056250

e. Overall Block Diagram Description of Frequency Synthesizer 1A14/2A21. Figure 8-11 is an overall block diagram of the frequency synthesizer. The main signal flow (heavy lines on diagram) between plug-in modules (Al through A7) is shown. The dc power distribution from dual power supply A8 to modules A1 through A7 is also shown. Each module is represented by a block on the diagram. Main chassis circuits (i.e. thumbwheel switches) are also shown as blocks on the diagram. The main signal flow through frequency synthesizer 1A14 is described in (1) through (5) below. The description also applies to frequency synthesizer 2A21, except the reference designations are prefixed with 1A14 instead of 2A21 and the word "transmitter" is used instead of "receiver."

(1) RF oscillator 1A14A1 utilizes a voltage controlled oscillator (vco) to produce an RF output signal in the 284.3750 to 303.1250-MHz frequency range. The specific frequency of the RF output signal is determined by the vco bias signal. Two RF output signal levels (high and low), at the same frequency, are provided by RF oscillator 1A14A1. The 20-milliwatt (nominal) RF output (high) signal is applied through the frequency synthesizer main chassis (synth output) to the frequency multiplier circuits of the transmitter. A detected RF output signal level (meter), derived from the RF output (high) signal is applied through the main chassis (synth level) to the transmitter meter selector switch. The 1-milliwatt (nominal) RF output (low) signal is applied to electronic frequency converter 1A14A2 (part of phase-lock loop circuits). The vco bias voltage input to 1A14A1 is derived from a comparison of the RF output (low) signal from 1A14A1 with a reference signal. A lamp test signal from the main chassis TEST switch is applied to test the failure lamp in 1A14A1. The failure lamp lights when the RF output signal is not present.

(2) Electronic frequency converter 1A14A2 converts the RF output (low) signal from 1A14A1 to an intermediate frequency (IF) output signal that is compatible with the digital integrated circuits in variable frequency dividers No. 1 (1A14A4) and No. 2 (1A14A5). This is accomplished by first dividing the RF output (low) signal (284.375 to 303.125 MHz) by two and then mixing the resulting frequency (142.1875 to 151.5625 MHz) with a 128-Hz reference frequency. The 128-MHz reference signal is produced in 1A14A2 by multiplying the 8-MHz signal from standard RF oscillator 1A14A7 by 16. The intermediate frequency (14.1875 to 23.5625 MHz) is produced by mixer circuits within 1A14A2 and is applied to variable frequency divider No. 1 1A14A4.

(3) Variable frequency divider No. 1 (1A14A4) operates in conjunction with variable frequency divider No. 2 (1A14A5) to divide the IF output signal from 1A14A2. Variable frequency divider No. 1 (1A14A4) has the capability of dividing the IF output signal by 200. The divided IF output signal (count) from 1A14A4 is applied to variable frequency divider No. 2 (1A14A5). Variable frequency divider No. 2 has the capability of dividing the input signal by 80. Thus, variable dividers 1A14A4 and 1A14A5 have the capability of dividing the IF output signal from 1A14A2 by 16,000 (200 x 80). However, the maximum division capability is not utilized. The division ratio is established by the thumbwheel switches on the frequency synthesizer front panel. The thumbwheel switches can be set between 4400.0 and 5000.0 MHz to provide a divisor from 9080 to 15080. When the thumbwheel switches are set between 4400.0 and 4699.9 MHz, the intermediate output signal from electronic frequency converter 1A14A2 is divided by between 9080 and 15078 respectively. Each 0.1-MHz step in the switch changes the divisor by two, e.g., switch setting 4400 establishes division by 9080 and switch setting 4400.1 establishes division by 9082. When switches are set between 4700.0 and 4999.9 MHz, the division is again between 9080 and 15078, respectively. When the switches are set to 5000 MHz, the divisor is set at 15080. Variable frequency divider No. 1 (1A14A4) divides the IF output frequency from 1A14A2 in accordance with the 1 and 0.1-MHz thumbwheel switch settings. Variable frequency divider No. 2 (1A14A5), divides the count output from variable frequency divider No. 1 (1A14A4) in accordance with the 1000-, 100-, and 10-MHz switch settings. The variable frequency dividers (1A14A4 and 1A14A5) divide the IF output signal from 1A14A2 to produce the divide-by-N (-N) signal. When phase-lock is established (RF output from 1A14A1 is exactly at the frequency indicated by the thumbwheel settings), the frequency of the divide-by-N pulses is exactly 1.5625 kHz. If the thumbwheel switch settings are changed to a new frequency, the countdown in the variable frequency divider circuits changes causing the frequency of the divide-by-N pulses to change. For this condition (phase-loop unlocked), the frequency of the divide-by-N pulses is not exactly 1.5625 kHz. The divide-by-N output pulses from 1A14A5 are applied to fixed frequency divider 1A14A6 and AF phase error detector 1A14A3.

(4) Fixed frequency divider 1A14A6 produces a 1.5625-kHz reference signal from the 8 MHz input signal from standard RF oscillator 1A14A7 and compares the 1.5625-kHz reference signal with the divide-by-N pulses received from 1A14A5. A two-bit correction signal and a phaselock signal are generated within 1A14A6 as a result of this comparison. The two-bit correction signal is used in determining the vco bias voltage which is produced by AF phase error detector 1A14A3. The phase-lock signal is applied (synth alarm) to the transmitter alarm circuits and is used to control an alarm indicator on the transmitter meter panel. If the 1.5625-kHz reference signal and the divide-by-N pulses are in phase, the two-bit correction signal remains fixed and the phase-lock signal indicates a phase-lock condition (normal indication on transmitter meter panel). If the 1.5625-kHz reference signal and the divide-by-N pulses are not in phase, the two-bit correct signal (20 and 21) cycles through four states (00, 01, 10, and 11), causing the vco bias voltage produced in 1A14A3 to cycle through four voltage levels. Also, for this condition, the phaselock signal indicates an out-of-phase condition causing an alarm indication on the transmitter meter panel.

(5) AF phase error detector 1A14A3 receives the 1.5625-kHz reference and two-bit correction signals from 1A14A6 and the divide-by-N pulses from 1A14A5. The 1.5625-kHz reference signal is used to start a sawtooth waveform generated within 1A14A3. The sawtooth waveform is superimposed on dc level(s) determined by the two-bit correction signal. For a phase-lock condition, the dc level remains fixed. For an out-of-phase condition, the two-bit correction signal cycles through its four states causing the vco bias voltage to cycle through four voltage step levels. The sawtooth waveform, superimposed on each step level, is of sufficient amplitude to overlap adjacent step levels. Thus, the step levels provide coarse tuning of the vco bias voltage and the sawtooth waveform provides fine tuning of the vco bias voltage within each step voltage changes. The divide-by-N pulses are used to gate and store the sawtooth waveform level. The stored voltage is the vco bias voltage which is applied to the vco in 1A14A1 thereby controlling the RF output frequency. When the divide-by-N pulses and the 1.5625-kHz reference frequencies are equal (phase-lock condition), the gate opens at the same point on the sawtooth range for each vco bias voltage sample; thus, the vco bias voltage will remain constant causing the RF output frequency to remain constant. If the divide-by-N pulses and the 1.5625-kHz reference signal are not exactly the

same frequency (a changing phase), the sampling point on the sawtooth waveform varies and the vco bias voltage changes. If the phase (time) between the pulses is decreasing (corresponding to an increase in the vco RF output frequency), the sawtooth is sampled at a lower point on the sawtooth ramp and the vco bias voltage is reduced which will decrease the vco RF output frequency to produce the phase-lock condition. Conversely, if the phase difference increases (corresponding to a decrease in RF output frequency) the sawtooth is sampled at a higher point on the sawtooth ramp and the vco bias voltage is increased which will increase the vco RF output frequency to produce the phase-lock condition. Once phase-lock is accomplished, the correction cycling is halted and the vco bias voltage remains fixed.

1-28. Frequency Synthesizer 1A14/2A21 Detailed Block Diagram Description

(fig. 8-12)

Figure 8-12 is a detailed block diagram of the frequency synthesizer. The functional relationships between the plug-in module (A1 through A8) and chassis components are shown. Plug-in modules Al through A6 are functionalized and the signal paths through each module and between each module are shown. Modules A7 and A8 are shown as single blocks on the diagram because they are sealed units (nonreparable). Paragraphs 1-29 through 1-33 provide a detailed block diagram description of frequency synthesizer 1A14 used in the transmitter. The modules are described in signal flow sequence starting with RF output signal from 1A14A1 and proceeding through the phase-lock loop modules (1A14A2, 1A14A4, 1A14A5, 1A14A6, and 1A14A3). The descriptions also apply to frequency synthesizer 2A21 used in the receiver, except the reference designations are prefixed with 2A21 instead of 1A14 and the word "receiver" is used instead of "transmitter."

1-29. RF Oscillator 1A14A1 Block Diagram Description

(fig. 8-12)

The RF oscillator consists of three printed circuit boards (A2, A3, and A4) and one encapsulated vco subassembly (Y1). When 28 vdc is applied to A3 board, the regulator (VR1) and lamp circuits on board A3 are energized. The regulator applies 20 vdc to vco subassembly (Y1) and to boards A2 and A4. The vco subassembly (Y1) produces an RF signal between 284.3750 and 303.1250 MHz. The specific RF signal depends upon the vco bias signal level (4.5 vdc to 16.0 vdc) applied to the vco subassembly (Y1). The RF output signal between 284.3750 and 303.1250 MHz from the vco subassembly (Y1) is applied to boards A2 and A4.

a. Board A4. The RF output signal between 284.3750 and 303.1250 MHz from vco subassembly (Y1) is amplified by buffer amplifier (Q4 and Q5) to a 20 milliwatt output level. The amplified RF output (high) signal, is applied through the main chassis OUTPUT connector (synth output) to the transmitter local oscillator circuits. A sample of the amplified signal from the buffer amplifier (Q4 and Q5) is detected by meter detector diode CR3 to produce a dc current proportional to the RF signal level. The meter current (detected RF level) is 25 microamperes when the RF output (high) signal level is 20 milliwatts. The detected RF level is applied through main chassis low pass filter 1A14RL4 and applied to synthesizer position of transmitter selector switch as a synth level output signal used to monitor output of frequency synthesizer 1A14.

b. Board A2. The RF output signal (between 284.3750 and 303.1250 MHz) from vco subassembly (Y1) is amplified by digital amplifier (Q1 and Q2) to a 1-milliwatt output level. The amplified RF output (low) signal, is applied to electronic frequency converter 1A14A2. The amplified output signal from the digital amplifier. (Q1 and Q2) is detected by lamp detector diode CR1 and applied to diode CR2 on board A3. The detected signal is then applied to lamp drive Q3 on board A3. When the RF output level from the digital amplifier is 1 milliwatt (normal condition), the detected signal biases the lamp driver Q3 off causing the failure lamp DS1 to be extinguished. When the RF output level from the digital amplifier Q1 and Q2 drops below 1 milliwatt (alarm condition), the lamp driver Q3 is biased on causing the failure lamp to light red. The lamp is tested by pressing the TEST button on the frequency synthesizer front panel.

1-30. Electronic Frequency Converter 1A14A2 Block Diagram Description.

(fig. 8-12)

The electronic frequency converter consists of two printed circuit boards Al and A2 that translate the RF output (low) signal from RF oscillator 1A14A1 to an intermediate frequency which is applied to variable frequency divider No. 1

1A14A4. The RF output (low) signal is between 284.3750 and 303.1250 MHz and is applied to a divide-by-two circuit consisting of Q1, Q2 and Q3 on board Al. The divided signal (142.1875 MHz to 151.5625 MHz) is amplified by RF amplifiers Q4 and Q5 and applied to the local oscillator input port of mixer Z1. The 8-MHz signal' from standard RF oscillator 1A14A7 is applied to board A2 where it is multiplied by 16 through multiplier stages Q1, Q2, and Q3 producing a 128-MHz output signal. The resultant 128-MHz signal is applied through emitter follower Q4 to the signal input port of mixer Z1 on board A1. The mixer Z1 output is the difference frequency (14.1875 to 23.5625 MHz) of the two input signals to the mixer Z1. The 14.1875 to 23.5625-MHz IF output signal is amplified through video amplifiers Q6 and Q7 and applied to variable frequency divider No. 1 1A14A4. The amplified 14.1875 to 23.5625-MHz IF output signal is also applied to bias diode CR6 on board A1 which rectifies the signal to provide a turnoff bias voltage for lamp friver Q8. With lamp driver Q8 turned off, the failure lamp DS1 is extinguished (normal condition). When the IF output signal is not present, or drops to a low level, the turnoff bias is reduced and lamp driver Q8 turns on causing the failure lamp DS1 to light red (alarm condition). The failure lamp DS1 is tested by pressing the TEST button on the frequency synthesizer front pane. Pressing the TEST button applies 5 vdc to lamp driver Q8 producing a bias which overrides the turnoff bias and causes failure lamp DS1 to light. Voltage regulator diode CR5 on board Al produces 6.2 vdc which is applied to RF amplifier Q4 and Q5, the divide-by-two circuit Q1 through Q3 and lamp driver circuit Q8.

1-31. Variable Frequency Dividers 1A14A4 and 1A14A5 Block Diagram Description

(fig. 8-12)

a. General. The variable frequency divider modules divide the IF output frequency from 1A14A2 in accordance with the thumbwheel switch settings (4400.0 to 5000.0 MHz) to produce the divide-by-N output pulses. As stated previously, the variable divider circuits have the capability of dividing the 'IF output frequency by 16,000, but the divisor is limited to a number from 9080 to 15080 by the thumbwheel switch settings b below). The thumbwheel switches provide ground connections to the. switch gate inputs of the variable frequency divider modules in accordance with their settings (para 1-73*a*). The ground connections preset the number in the associated registers. The 1000-MHz and 10-MHz thumbwheel switches present the divide-by-eight ripple through counter registers in 1A14A5 with a number from 4 to 7. The 10-MHz thumbwheel switch presets the 10 MHz divide-by-ten registers in 1A14A5 with a number from 0 to 9. The 1-MHz thumbwheel switch presets the 1-MHz divide-by-ten registers in 1A14A4 with a number from 0 to 9. The 0.1-MHz thumbwheel switch presets the 0.1-MHz divide-by ten registers in 1A14A4 with a number from 0 to 9. Variable frequency divider No. 1 1A14A4 also contains a circuit which divides the IF output frequency by two before it is applied to the 0.1 MHz divide-by-ten registers. The registers in both modules count down the divided-by-two IF output frequency until the count in the registers reaches unique numbers (decimal 74 and 64) in 1A14A5 and 1A14A4 respectively. The unique number of 7464 establishes the upper frequency limit for the divisor required for dividing the IF output from 1A14A2 (b below). When the number 7464 is decoded, the control circuits reset the registers to an initial condition and the registers are preloaded with the count set by the thumbwheel switch settings. After the preloading sequence, the IF signal causes the registers to count down to zero. The next pulse produces the divide-by-N pulse output from 1A1A5. The pulse width of the divide by-N output is equal to 40 periods of the IF output signal whose sine wave frequency is between 14.1075 and 23.5625 MHz depending upon the RF output frequency of 1A14A2. The registers in 1A14A5 contain the most significant bits and will reach their unique number (decimal 74) before the registers in 1A14A4 have reached their number (decimal 64).

b. Thumbwheel Switch Settings/Divisor Ratios. Variable frequency dividers 1A14A4 and 1A14A5 divide the 14.1875 to 23.5625-MHz IF output frequency from 1A14A2 by a number from 9080 to 15080 depending upon the thumbwheel switch settings. The 14.1875 to 23.5625-MHz IF output frequency is divided down to 1.5625 kHz to accomplish phase-lock. For example, for a thumbwheel setting of 5000.0 MHz, the required IF output frequency is 23.5625 MHz. At this frequency, the variable frequency dividers divide the IF output frequency from 1A14A2 by 15080 (23.5625 MHz *15080=1.5625 kHz). The divisor is obtained by adding the counts to reach the unique number, initialize, inhibit and preload sequence count and the thumbwheel settings (1 + 536 + 3 + 7000 = 7540). Multiplying the count by two (2 X 7540 = 15080) supplies the divisor. The count is multiplied by two because the frequency of the IF output is divided by two in 1A14A4 before it is applied to the registers. How a thumbwheel switch setting of 5000.0 MHz

produces a divisor 15080 in the variable frequency divider circuits is explained in (1), (2), and (3) below.

(1) For a thumbwheel switch setting of 5000.0 MHz, the 0.1-MHz, 1.0-MHz, and 10-MHz divide-by-ten registers in variable frequency dividers 1A14A4 and 1A14A5 are preloaded with zeros. The divide-by-eight ripple through registers are preloaded with the number 7 ((3) below). The countdown cycle starts a 0000 (1 count), then counts down from 7999 to the unique number of 7464 (536 counts), after this count an initialize, inhibit, preload sequency takes place (3 counts) and the thumbwheel switch settings are loaded into the registers. The registers then count down from 7000 (corresponds to 5000.0 MHz) through 0000 (7000 counts) until the unique number appears again in the registers. The cycle then repeats as described above.

(2) Note that any divisor (D) can be calculated by adding 540 to the number (N) preloaded into the registers and multiplying by 2 (D = 2) (N + 540). For example, for a thumbwheel switch setting of 4400.0 MHz, the number preloaded into the registers is 4000. The divisor is calculated as follows: 2(4000 + 540) = 2(4540) = 9080.

(3) The following tables list the thumbwheel switch settings with corresponding closed switch contacts (fig. 8-12) and the resulting decimal numbers which are loaded into the associated registers.

S1-I and S1-II

1000- and 100-MHz switch settings	Closed switch contacts	Decimal number preloaded into ripple through register (÷8)
44	None	5
45	C	6
46	B	4
47	NONE	5
48	C	6
49	B	7
50	BAND C	

S1-III

10-MHz switch settings	Closed switch contacts	Decimal number preloaded into 10-MHz register (÷10)
0	A,B,C,D,E	0
1	B,C,D,E	1
2	C,D,E,	2
3	D,E,	3
4	E	4
5	NONE	5
6	A	6
7	A.B	7
8	A,B,C	8
9	A,B,C,D	9

S1-IV or S1-V

1-MHz or 0.1-MHz switch settings	Closed switch contacts	Decimal number preloaded into 1-M register (÷10) or 0 MHz register (÷10
0	NONE	0
1	1	1
2	2	2
3	1.2	3
4	4	4
5	1.4	5
6	2,4	6
7	1,2,4	7
8	8	8
9	1,8	9

c. Variable Frequency Divider No. 1 1A14A4 Block Diagram Description (fig. 8-12). With the thumbwheels set for 5000 MHz, the IF output signal of 23.5655 MHz from 1A14A2 is applied to board AI on variable frequency divider No. 1 1A14A4 where it is clamped by diode CR1 and applied to the divide-by-2 circuit Z1 through driver Q1. The divided pulses are inverted through input inverter Z2 and are the clock pulses for operating both the first stage of the 0.1-MHz divided-by-10 register and the control flip-flops Z5 and Z7. The countdown cycle begins when all stages of the two registers 0.1 MHz and 1 MHz contain zeros and control flip-flops Z5 and Z7 are reset. The next pulse from the input inverter Z2 triggers the 0.1 MHz register which triggers the 1-MHz registers which in turn produces a count output. This count output is applied through count inverter Z14 to variable frequency divider No. 2 1A14A5 where it triggers the 10-MHz register; this triggers the divide-by-8 ripple-through counter registers which triggers the output register and produces the divide-by-N(+ N) pulse. After 20 pulses from the input inverter Z2 (equal to 40 periods of the IF output signal), an overflow from the 0.1-MHz divide-by-10 register into the 1-MHz divide-by-10 register causes an output reset pulse to be applied to variable frequency divider No. 2 1A14A5 which resets output register Z10 in 1A14A5. The divide by-N (+N) output is

then applied to the fixed frequency divider 1A14A6 through output inverter Z1 on 1A14A5.

(1) The clock pulses from input inverter Z2 are applied to the registers causing the countdown sequence (0000 to 7464). At the unique count -(decimal 74, 1 + 536 count), the registers in variable frequency divider No. 2 1A14A5 are decoded and produce a reset enable level which is applied to control circuits in variable frequency divider No. 1 1A14A4. The reset enable level from reset enable gate Z1 on board Al of 1A14A5 is applied to control gate Z3 through the reset inverter Z14 on board A2 of 1A14A4. When the reset enable level is received and the count in the 0.1 and 1-MHz divide-by-10 registers reach the unique count (decimal 64, 1 + 536 count) required by control gate Z3, flip-flop Z5 becomes set. When flip-flop Z5 is set, the initialize pulse (537 + 1 count) is applied to all the registers in 1A14A4 and 1A14A5 which sets the registers to a count which enables the registers to be modified by the thumbwheel switch setting. The initialize pulse also prevents an additional count from being accumulated by the 0.1-MHz register.

(2) The next clock pulse following the initialized condition is not counted by the registers but sets flip-flop Z7. When flip-flop Z7 is set, the initialize condition is terminated and an inhibit level is produced (537 + 2 count) and applied to all registers.. The next clock pulse resets flip-flop Z5 but is inhibited to the registers. When flip-flop Z5 is reset, a preload pulse (537 + 3 count) is generated and applied to the register switch gates Z4, Z9 and Z16 on board Z2 causing the switch gates Z4, Z9 and Z16 to open (540 count). With the switch gates Z4, Z9 and Z16 opened, the thumbwheel switch settings modify the count in the registers.

(3) The next clock pulse is applied to the registers and resets flip-flop Z7; this terminates the inhibit condition The registers will then count down from the preloaded count to all zeros, during the next countdown cycle.

(4) Bias diode CR6 on board Al of 1A14A2 rectifies the count output signal to provide a turnoff bias for the lamp driver Q8. With the lamp driver Q8 turned off, failure lamp DS1 is extinguished. When the count output signal is not present or drops to a low level, the turnoff bias is reduced and lamp driver Q8 turns on causing the failure lamp DS1 to light red (alarm condition). Pressing the TEST button on the frequency synthesizer front panel applies 5 vdc to the lamp transistor driver causing the failure lamp to light red

d. Variable FREQUENCY Divider No. 2 1A14A5 Block Diagram Description (fig. 8-12). Variable frequency divider No. 2 contains one printed circuit board Al that divides the output from variable frequency divider No. 1 1A14A4 in accordance with the settings of the 1000100 and 10 MHz thumbwheel switch sections (5000.0 MHz for this description). The count pulse from variable frequency divider No. 1 1A14A4 are applied to the 10-MHz divide-by-10 register Z3 through Z6. The output pulses from the 10-MHz divide-by-10 register trigger the divide-by-eight ripple through counter registers Z7, Z8 and Z9.

(1) The countdown cycle continues until all of the registers Z2 through Z9 contain zeros. The next count pulse triggers the divide-by-eight ripple through counter registers Z7, Z8 and Z9 which sets the output register Z10 and produces a divide-by-N (-N) pulse. At this time one of the 10-MHz registers conditions the output register Z10 to be reset. After 40 cycles of the IF output frequency signal have been counted in variable frequency divider No. 1 1A14A4 an output reset signal is sent to reset output register Z10 which terminates the divide-by-N pulse. At the unique count (decimal 74, 1 + 536 count), the registers in 1A14A5 are in the required condition to satisfy the conditions for the reset enable gate Z1 and a reset enable level is applied to variable frequency divider No. 1 1A14A4. When the registers in variable frequency divider No. 1 1A14A4 are at their unique count (decimal 64, 1 + 536 count), control flip-flops Z5 and Z7 on 1A14A4 are triggered to produce the inhibit, initialize, and preload signals (537 + 3 count). The inhibit level is applied to the 10-MHz counter register to prevent it from accumulating a false count. The initialize pulse is applied to the registers in variable frequency divider No. 2 1A14A5 and they are set to a count which enables the registers to be modified by the thumbwheel switch settings. The preload pulse is applied to all the register switch gates Z12 through Z14 causing the switch gates to open. With the switch gates Z12 through Z14 opened, the thumbwheel switch settings modify the count in the registers. The preloaded registers then count down during the next countdown cycle.

(2) The divide-by-N signal is monitored by lamp driver Q1 and if it is not within the required amplitude and frequency limits, the lamp bias changes and failure lamp DS1 lights red. Pressing

the TEST button on the frequency synthesizer front panel applies 5 volts dc direct to the lamp transistor driver circuit causing the failure lamp DS1 to light red. For normal operating conditions the failure lamp DS1 is extinguished.

1-32. Fixer Frequency Divider 1A14A6 Block Diagram Description
(fig. 8-12)

a. The fixed frequency divider contains two printed circuit boards Al and A2 that perform three functions: the 8.0-MHz signal from the standard RF oscillator 1A14A7 is divided by 5120 to produce the 1.5625-kHz reference signal, the 1.5625-kHz reference signal and the divide-by-N (N) signal from variable frequency divider No. 2 1A14A5 are compared, and if the signals are not in phase, the fixed frequency divider generates a phase-lock alarm signal and produces the two-bit correction codes for the AF phase error detector 1A14A3.

b. The 8.0-MHz sinusoidal signal from the .standard RF oscillator 1A14A7 is applied to board A2. The 8.0-MHz signal is changed by clamp diode CR1 and inverted through inverter Z15 and applied to divider stages Z1 through Z10 and Z11 through Z13. These stages divide the 8 MHz signal by 5120 to provide the 1.5625-kHz reference signal. The 1.5625-kHz reference signal is applied to the AF phase error detector 1A14A3 through output register Z14 and inverter Z24. The 1.5625-kHz reference signal is also applied to fixed frequency divider board Al through output register Z14. The 1.5625-kHz output from divider Z13 is monitored by failure lamp DS1 through bias diode CR3 and lamp driver Q1. For normal conditions, lamp driver Q1 is turned on and a transistor in the lamp assembly is turned off causing the failure lamp DS1 to be extinguished. When the 1.5625-kHz output from divider Z13 is not present, lamp driver Q1 turns off and the transistor in the lamp assembly turns on causing the failure lamp DS1 to light red. Pressing the TEST button on the frequency synthesizer front panel applies 5 vdc to the lamp transistor driver causing the failure lamp to light red.

c. The divide-by-N signal from variable frequency divider No. 2 1A14A5 is also applied to board A1 of 1A14A6 where it is compared with the 1.5625-kHz reference signal in the phase-lock detector circuits Z16 through Z18. If the signals are in phase, the phase-lock detector circuits are balanced. For this condition (phase-loop locked), the output of the phase-lock detector circuits is unchanged and no signals are applied to inverter Z24. The output of inverter Z24 is applied through alarm bias diode CR1 to the failure lamp DS1 assembly and to alarm driver Q2. With no signals applied to inverter Z24, the failure lamp DS1 is extinguished (normal condition) and alarm driver Q2 is turned off. The output from alarm driver Q2 is applied through main chassis low pass filter 1A14FL3 (synth lock) to the SYNTH LOCK indicator on the transmitter meter panel. With alarm driver Q2 turned off, the SYNTH LOCK indicator lights green (normal indication). If the divide-by-N pulses and the 1.5625-kHz signals are not in phase, the phaselock detector circuits become unbalanced and square wave pulses are applied to inverter Z24. For this condition (phase-loop unlocked), the failure lamp DS1 on 1A14A6 lights red (alarm condition) and alarm driver Q2 turns on. With alarm driver Q2 turned on, the SYNTH LOCK indicator on the transmitter meter panel also lights red (alarm condition).

d. The output of the phase-lock detector circuits is also applied to counter circuit Z19 through Z23. With the phase-lock detector circuits balanced (phase-lock condition), the counter remains in a fixed condition. Therefore, the output of the counter is fixed causing the output of the two-bit gates Z18 to be fixed. For this condition, the two bit correction signal (20 and 21) applied to AF phase error detector 1A14A3 remains fixed. When the phase-lock detector circuits become unbalanced (phase-loop unlocked), the counter begins counting and the two-bit correction signal applied to phase error detector 1A14A3 cycles through its four conditions (00, 01, 10, and 11).

1-33. AF Phase Error Detector 1A14A3 Block Diagram Description
(fig. 8-12)

a. The AF phase error detector consists of one printed circuit board Al that converts the phase difference between the 1.5625-kHz reference signal from fixed frequency divider 1A14A6 and the divide-by-N signal from variable frequency divider No. 2 1A14A5 into a bias voltage which controls the frequency of the vco in oscillator 1A14A1. The 1.5625-kHz pulses from fixed frequency divider 1A14A6 are applied to sawtooth generator Q3 and Q4 to restart the sawtooth waveform. The divide-by-N signal controls sample and hold circuit Q7 which samples the sawtooth

signal and controls the hold signal transistors buffer amplifiers Q10 and Q11. When the 1.5625 kHz reference signal and the divide-by-N pulses are identical in frequency (zero time phase variation), the sampling point will occur at the same point on the sawtooth ramp resulting in a constant hold voltage. When the two signals are not identical in frequency (a changing time phase), each sample will occur at a different point on the sawtooth ramp resulting in a varying hold voltage (sawtooth in characteristic). The frequency of the varying hold voltage is equal to the difference frequency between the 1.5625-kHz reference signal and the divide-by-N pulses. The sampled voltage level is amplified by dc amplifier Q12, and Q13, filtered, and applied to the vco subassembly Y1 in 1A14A1 as a vco bias varying voltage to correct the output frequency. Thus, the reference and divide-by-N pulses are brought to the same frequency (no time phase variation between them).

b. The pull-in frequency range of the phase-lock process is restricted to a portion of the total vco frequency range (RF output frequency range). In order to accomplish phase-locking of the vco over its entire range, it is necessary to "step change" the vco frequency in four discrete increments, each increment being less than the phase-lock loop pull-in range. This is implemented by coarse tuning the vco bias voltage in four discrete dc voltage steps produced by the two-bit correction code (21 and 20) and digital-to-analog converter Q8 and Q9. In an out-of-lock condition, the correction code cycles through its four states 00, 01, 10, and 11 causing the vco bias voltage to cycle through its four step voltage levels. The sawtooth waveform is superimposed on each step level and is of sufficient amplitude to overlap adjacent step levels. Thus, the sawtooth provides the fine tuning vco bias voltage within each step voltage change. The composite signal is used to phase-lock the vco subassembly Y1. When the combined step voltage and sawtooth covers the portion of the bias voltage range that includes the desired RF output frequency, the loop starts to phase-lock. When phase-lock is achieved, the correction code cycling halts in one of its four coded states producing a corresponding fixed coarse tuning vco bias voltage. The constant stored voltage used to bias the vco to the exact frequency required is the combined coarse tuning dc voltage level and the fine tuning fixed error correction voltage produced 'by constant point sampling of the sawtooth ramp. For any given required vco frequency setting, the phase-lock loop automatically selects the correction code state and the sawtooth constant sampling point to maintain a phase-lock condition. Within any two coarse tuning increments, the sawtooth constant sampled point is positioned along the sawtooth ramp producing the required vco fine tuning frequency increments. The loop automatically positions the constant sampling point by adjusting the fixed phase difference between the identical frequency 1.5625-kHz reference pulses and the divide-by-N sampling pulses. The: higher the required vco frequency, the greater the phase difference, the higher the sawtooth ramp constant voltage sampling point.

c. The sawtooth waveform output from the sawtooth generator Q3 and Q4 is buffered by Q5 and Q6 and rectified by ac detector Q1. The resulting dc voltage biases the transistor in the failure lamp DS1 assembly off, causing the failure lamp DS1 to be extinguished. When the sawtooth signal is not present or its amplitude drops to a low level, the ac detector biases the transistor in the failure lamp assembly DS1 on, causing the failure lamp DS1 to light red (alarm condition). Pressing the TEST button on the frequency synthesizer front panel applies 5 vdc to the failure lamp transistor causing the lamp to light red.

d. Voltage regular Q2 provides 20 vdc to operate transistor circuits Q3 through Q6 and Q8 through Q13.

1-34. Alarm Monitor 1A5 Block Diagram Description
(fig. 8-13)

a. Alarm monitor 1A5 receives monitor signals (traffic monitor, RF power monitor, reflected power monitor, and synthesizer monitor signals) and controls the associated alarm indicators on the transmitter meter panel. Depending upon the signal level received, the associated indicator lights either green (normal indication) or red (alarm indication). The alarm monitor also contains a summary alarm circuit which is enabled when any one of the alarm conditions occur. The traffic monitor signal indicates the signal level input to modulator 1A8. The RF power monitor and reflected power monitor signals indicate the forward RF power and reflected power levels at the output of the transmitter. The synthesizer alarm signal is received direct from frequency synthesizer 1A14 and indicates if the signals from variable frequency divider No. 2 (1A14A5) and standard RF oscillator (1A14A7) are phaselocked. An identical alarm monitor (2A20) is used

in the receiver, however, the jumper connections on the associated plate assembly connectors are different for each module. The receiver's alarm monitor module is described in paragraph 1-92.

b. The following description is based on the circuits shown in figure 8-13.

(1) The TRAF, RF POWER, REFL RF POWER, and SYNTH LOCK indicators on the transmitter meter panel are controlled by Schmitt trigger circuits in alarm monitor 1A5. The Schmitt trigger circuits cause the associated indicators to light green (normal indication) or red (alarm condition). The input signals to the alarm monitor control the operation of the associated Schmitt trigger circuits.

(2) The traffic monitor signal is supplied by modulator 1A8 through pcm attenuator 1A3. The traffic monitor signal is applied directly to operational amplifier (integrated circuit) AR1. The operational amplifier output is detected and applied to the traffic meter through a potentiometer and to Schmitt trigger circuit Q5, Q6 through dc emitter follower Q1. If the traffic monitor signal exceeds a predetermined level, the dc voltage developed by detector CR1, CR2 will cause Q5 to turn on, causing Q6 to turn off and Q7 to turn on. With Q7 turned on, a low impedance path to ground is provided for the normal traffic indicator lamp, and the TRAF indicator lights green. Since Q6 is turned off, a high impedance path to ground is provided for the alarm traffic indicator lamp causing the indicator lamp (red) to remain off. When the traffic monitor signal falls below the predetermined voltage, the de voltage applied to the base of Q5 is not sufficient to keep Q5 conducting. With Q5 turned off, Q6 turns on and Q7 turns off. For this condition, a high impedance path to ground is applied to the normal traffic indicator lamp and a low impedance path to ground is applied to the alarm traffic indicator lamp. Consequently, the TRAF indication changes from green to red. Also with Q7 turned off, the Q7 output dc voltage is high, enabling the OR gate which causes Q23 to turn on. With Q23 turned on, a transmitter summary alarm indication is provided.

(3) The synthesizer monitor signal is derived from frequency synthesizer 1A14. The signal (dc level) is applied direct to Schmitt trigger Q14, Q15. Circuit operation is identical to that described above for the traffic monitor circuit. If the synthesizer monitor signal exceeds the predetermined dc level, the: SYNTH LOCK indicator lights green (normal indication). If the synthesizer monitor signal is below the predetermined level, the SYNTH LOCK indicator lights red (alarm condition) and, in addition, the summary alarm circuit is enabled.

(4) The RF power monitor signal is a detected dc voltage supplied by directional coupler 1DC2. The dc signal is applied to operational amplifier (integrated circuit) AR3 and the RF power meter circuit through an attenuator. The output of AR3 is applied direct to Schmitt trigger Q11, Q12. The operation of the Schmitt trigger is identical to that described above for the traffic monitor circuit. If the RF power monitor signal exceeds the predetermined dc level, the RF POWER indicator lights green (normal indication). If the RF monitor signal is below the predetermined level, the RF POWER indicator lights red (alarm indication) and the summary alarm circuit is enabled.

(5) The reflected power monitor signal is a detected dc voltage supplied by directional coupler 1DC2. The dc signal is applied to operational amplifier (integrated circuit) AR2 through a variable attenuator circuit. An output from the attenuator circuit is also applied to the reflected power meter circuit. The output of AR2 is applied to Schmitt trigger Q8, Q9. The operation of Schmitt trigger Q8, Q9 is similar to that previously described for the other monitor circuits except the alarm and normal outputs are reversed. The outputs of Schmitt trigger Q8, Q9 are reversed because it is the presence rather than the absence of a dc voltage at the Schmitt trigger input that results in an alarm condition.

(6) The summary alarm circuit is comprised of diode OR gate (CR12-CR15) and transistor Q23. Each of the normal outputs is connected to the OR gate. For normal operation, transistor Q23 is off (nonconducting). When any one of the alarm conditions occur, the OR gate switches Q23 on (conducting state) cause a transmitter summary alarm condition.

1-35. Radio Test Set Block Diagram Description
(fig. 1-17)

The radio set provides two separate test signals (one for each receiver channel) which can be used to align, test, or troubleshoot the receiver. The two test signals are obtained by mixing a portion of the transmitter output with the output from 100-MHz RF oscillator 1A2. The resulting receiver input signals are 100 MHz away from the

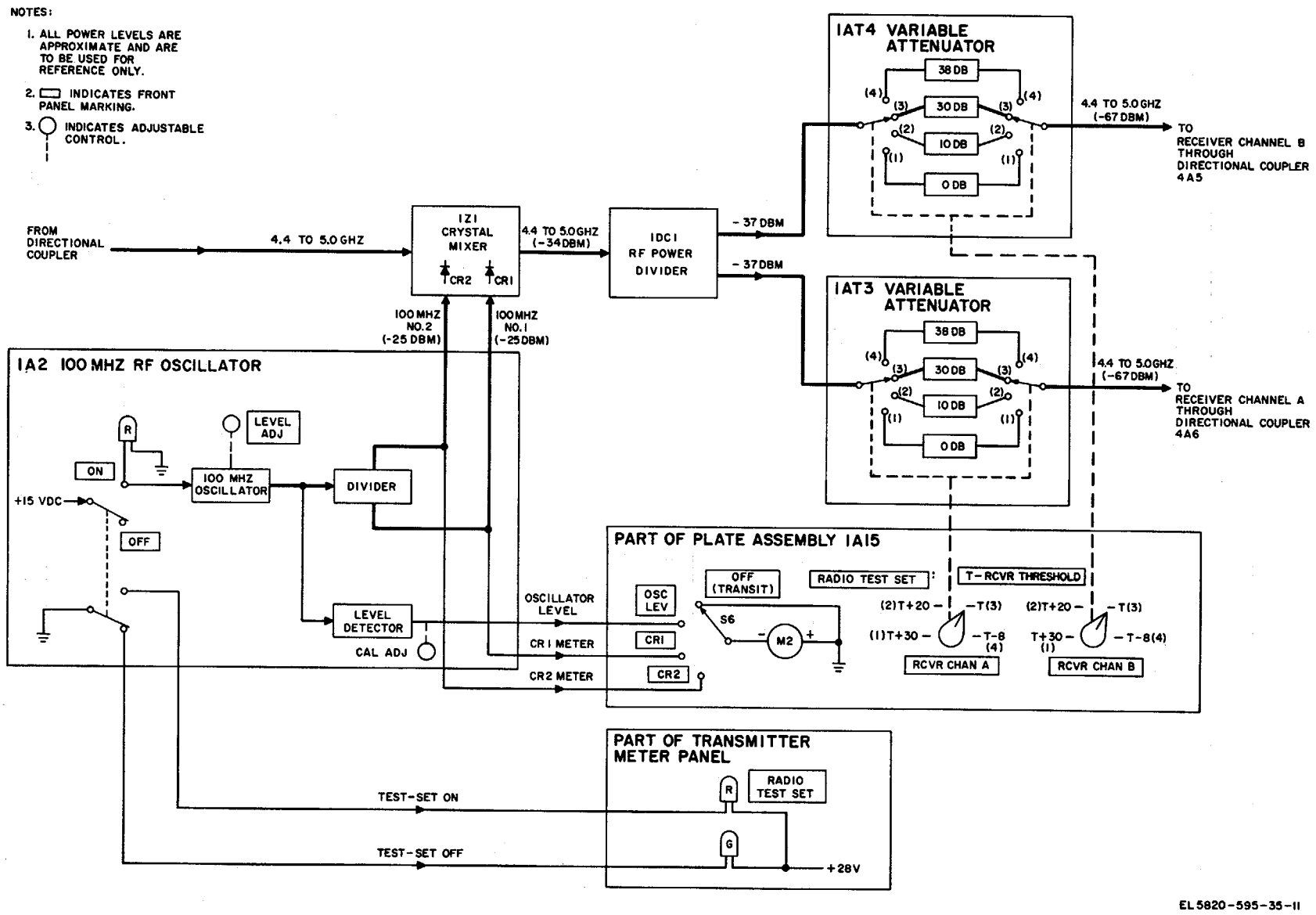


Figure 117. Radio test set, block diagram.

transmitter frequency. The radio test set consists of 100-MHz RF oscillator 1A2, crystal mixer 1Z1, RF power divider 1DC1, variable attenuators 1AT3 and 1AT4, and the radio test set panel. Controls for the two variable attenuators, a meter selector switch, and a meter are provided on the radio test set panel. The meter selector switch permits monitoring of the 100-MHz oscillator output level and the crystal mixer diode currents of mixer diodes 1Z1CR1 and 1Z1CR2.

a. When testing, aligning, or troubleshooting the receiver, two 100-MHz signals are applied to crystal mixer diodes 1Z1CR1 and 1Z1CR2. The 100-MHz signals are generated when the 100-MHz RF oscillator's ON-OFF switch is placed in the ON position. With the switch in the ON position, the indicator on the oscillator module is lighted, the RADIO TEST SET indicator on the transmitter meter panel is lighted red, and supply voltage is applied to the oscillator. The LEV ADJ control is used to adjust the oscillator's output level for 12 or 24-channel pcm operation. The output level is monitored by setting the RADIO TEST SET switch to the OSC LEV position and the meter face is marked to indicate the oscillator output level required for 12 to 24-channel operation. The crystal mixer diode currents (CR1 or CR2) can also be monitored by setting the RADIO TEST SET switch to the appropriate position.

b. Crystal mixer 1Z1 receives a portion of the transmitter output signal from directional coupler 1DC2. The signal is in the 4.4 to 5.0-GHz frequency range at a level approximately 21 db down from the transmitter output. This signal is mixed with the 100-MHz output signal from oscillator 1A2 producing frequencies 100 MHz above and below the 4.4 to 5.0-GHz input. The signal level output of the crystal mixer for 12-channel operation is approximately -34 dbm (9 db below each 100-MHz input level to the crystal mixer). RF power divider 1DC1 provides two equal output signals which are approximately -37 dbm (3 db down from the input level). The two equal signal levels are then applied to the channel A and channel B variable attenuators (1AT3 and 1AT4 respectively). Each variable attenuator provides four attenuation levels (0, 10, 30, and 38 db). RCVR A and RCVR B (on the radio test set) attenuator switch positions T+30, T+20, T, and T-8 correspond to the 0, 10, 30, and 38 attenuation levels. T represents the receiver threshold which is -100 dbm for 12-channel operation and -97 dbm for 24-channel operation. The -100 dbm or -97 dbm threshold level is obtained by adjusting the 100-MHz RF oscillator output level as previously described.

c. The -100 dbm threshold input to receiver channels A and B is obtained as follows:

(1) The output of crystal mixer 1Z1 is approximately -34 dbm (level was set by adjusting output of 100-MHz RF oscillator for 12 channel operation).

(2) RF power divider 1DC1 provides two equal outputs of -37 dbm (3 db down from -34 dbm input).

(3) Variable attenuators 1AT3 and 1AT4 provide 30 db attenuation when RCVR CHAN A and RCVR CHAN B switches are set to T. Thus the output of each attenuator is -67 dbm.

(4) Directional couplers 4A5 and 4A6 provide a fixed decoupling loss of 20 db. Each directional coupler contains a variable attenuator which provides an additional loss of 0-20 db. The variable attenuators are calibrated at the direct support level to provide the remaining loss required for a -100 dbm input to each receiver channel. The receiver threshold for 12-channel operation is -100 dbm. The variable attenuators compensate for inequalities in the RF cabling losses and other RF components between RF power divider 1DC1 and the receiver inputs.

d. The RCVR CHAN switch settings and corresponding receiver input levels for 12-channel and 24-channel operation are listed below.

Switch settings	Receiver input levels	
	12-channel operation	24-channel operation
T + 30	-70 dbm	-67 dbm
T + 20	-80 dbm	-77 dbm
T	-100 dbm	-97 dbm
T - 8	-108 dbm	-105 dbm

e. To insure that the transmitter carrier frequency is of the same polarity as the receiver carrier frequency, the transmitter must be tuned 100 MHz above or below the receiver operating frequency as follows:

(1) If the receiver is tuned to any frequency between 4400.0 and 4699.9 MHz, the transmitter must be set in the same band between 4400.0 and 4699.9 MHz. For example, if the receiver carrier frequency is 4685.2 MHz, the transmitter carrier frequency must be set to 4585.2 MHz (but not 4785.2) in order to operate the radio test set.

(2) If the receiver is tuned to any frequency between 4700.0 and 5000.0 MHz, the transmitter must be set in the same band between 4700.0 and

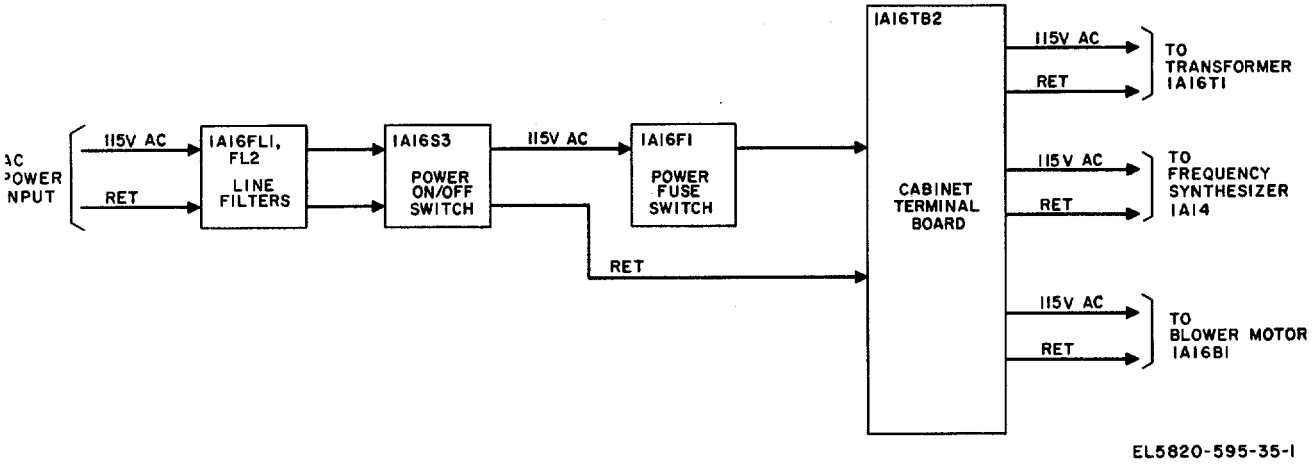


Figure 1-18. Transmitter primary power distribution.

5000.0 MHz. For example, if the receiver carrier frequency is 4785.7 MHz, the transmitter carrier frequency must be set to 4885.7 MHz (but not 4685.7 MHz) in order to operate the radio test set.

f. When the radio test set is not in use, the 100-MHz RF oscillator (1A2) must be turned off. With the oscillator's ON-OFF switch in the OFF position, the indicator on the oscillator module is extinguished, the RADIO TEST SET indicator on the transmitter meter panel is lighted green, and the supply voltage is removed from the 100-MHz RF oscillator. For this condition, the test signals to the receiver are removed.

1-36. Transmitter Primary Power Distribution
(fig. 1-18)

The 115 vac primary power is applied to the transmitter through AC POWER INPUT connector 1A16J7. The 115 vac input passes through line filters 1A16FL1 and FL2 to the POWER ON-OFF switch on the transmitter meter panel. When the POWER ON-OFF switch is set to the ON position, 115 vac passes through the 5 AMPS SLO-BLO power fuse and is distributed via terminal board 1A16TB2 to transformer 1A16T1, frequency synthesizer 1A14, and blower motor 1A16B1. Refer to the transmitter interconnecting diagram (fig. 8-14) for detailed primary power connections.

1-37. Transmitter Dc Power Distribution
(fig. 8-15)

The 115 vac input to transformer 1A16T1 is stepped down to ac output voltages of 8.5, 11, 13.5, 15, 16, 16.5, 27.5, and 30 vac. The ac output voltages are applied to voltage regulators in power supply 1A1. Four 5/6v regulators, for 12v regulators, and three 15/28v regulators are utilized. A typical voltage regulator circuit is described in paragraph 1-38. The voltage regulators provide regulated dc voltage outputs and associated dc returns. The dc voltages and return lines are distributed to the modules and other cabinet components. Cabinet terminal board 1A16TB2 and plate assembly terminal board 1A15TB1 are used to distribute certain voltages. Refer to the transmitter interconnecting diagram (fig. 8-14), and power supply 1A1 interconnecting diagram (fig. 8-16), for detailed de voltage connections.

1-38. Typical Voltage Regulator Block Diagram Description
(fig. 1-19)

Both the transmitter and receiver power supplies, 1A1 and 2A3, use the same type regulator modules, except the receiver does not require a 5/6v regulator. The following is a breakdown of regulators used and their module designations:

	1A1	2A3
5/6v	1A1A1 through 1A1A4	NA
12v	1AA6 through 1A1A9	2A3L.43
15/28v	1A1A10 through 1A1A12	2A3A1, 2A3A2, 2A3A4

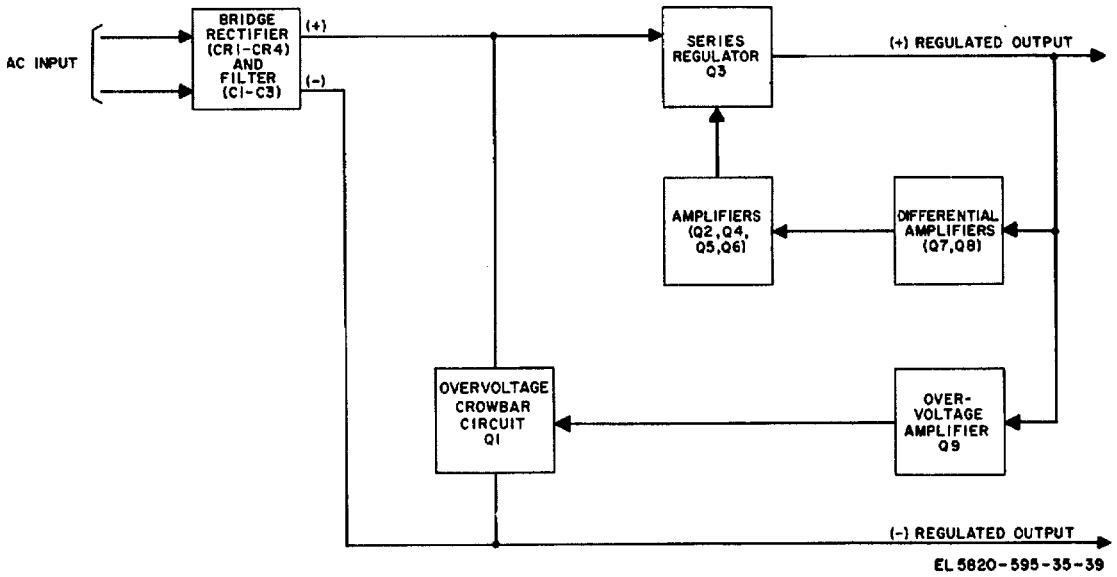


Figure 1-19. Typical voltage regulator, block diagram.

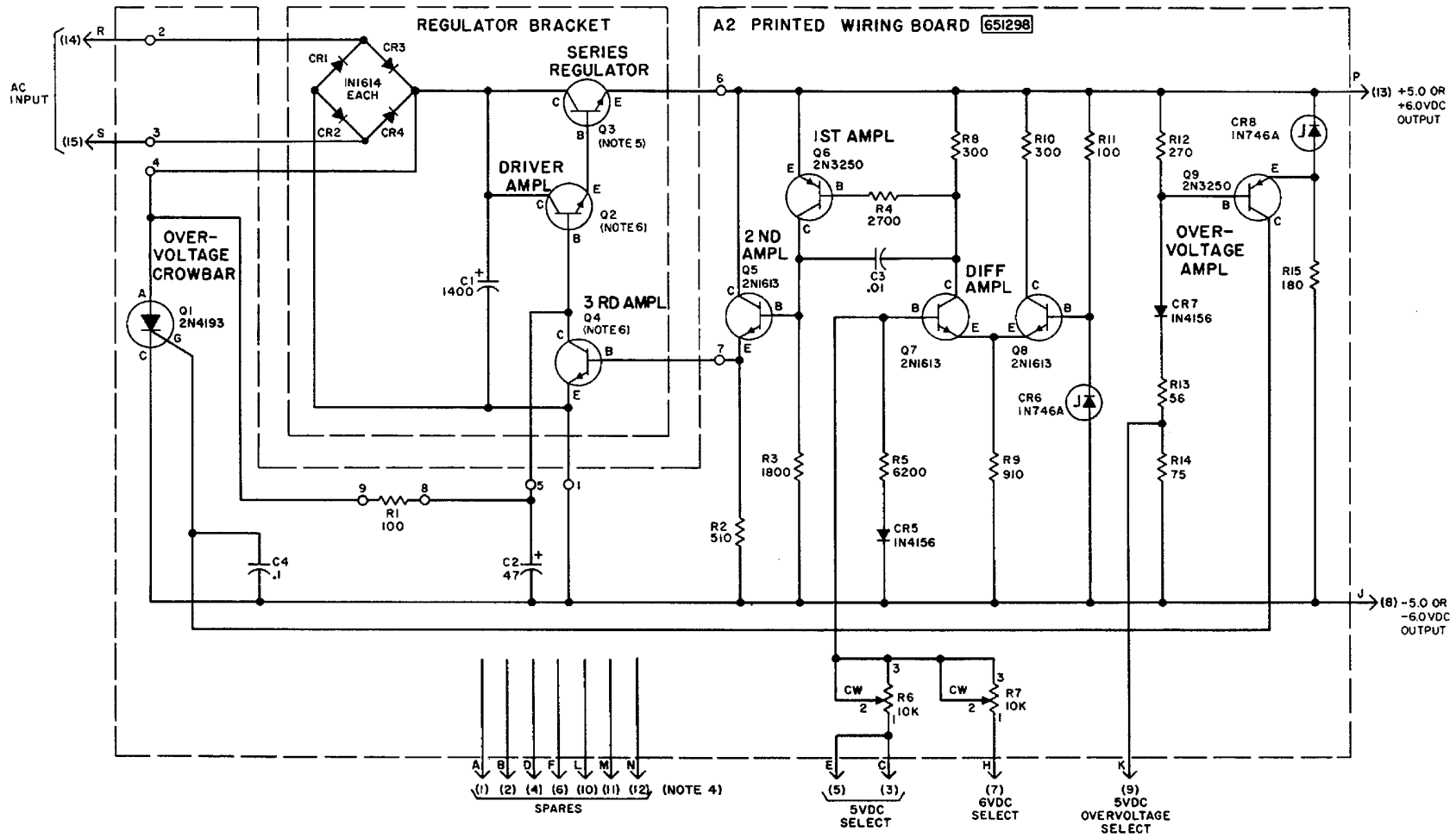
Since the-5/6v, 12v, and 15/28v regulator modules are similar, the following description of a 15/28v regulator covers, in general; the operation of all three regulator modules. The regulators consist of a bridge rectifier and filter, series regulator, and overvoltage protection circuits. The description is based on the block diagram shown in figure 1-19. Detailed circuit theory descriptions for each -regulator are given in paragraphs 1-41 through 1-43.

a. Bridge Rectifier and Regulator Circuit. The output of bridge rectifier CR1 through CR4 is filtered by capacitors C1 through C3. The filtered but unregulated output is applied to the collector of series regulator QS. Series regulator Q3, under control of differential amplifier (Q7, Q8), amplifier (Q4-Q6), and driver amplifier Q2 introduces the voltage drop necessary to maintain voltage regulation at its emitter output.

b. Overvoltage Protection Circuit. Overvoltage protection is provided by Thyristor (SCR) Q1. Atn overvoltage condition at the output is sensed by overvoltage amplifier Q9 which triggers Q1 into conduction. With Q1 conducting, the rectifier output is short circuited causing the fuse in the AC input line to open. This circuit is known as a "crowbar." 1-39. Module Circuit Theory The transmitter module circuit theory descriptions are provided in paragraphs 1-40 through 1-81. Module circuit theory descriptions appear in sequential reference designation order and are given at the schematic diagram level. Circuit theory descriptions and schematic diagrams are not provided for the transmitter's nonrepairable modules (i.e. 1137 to 1213-MHz circulator 1HY1, 4.4-5.0-GHz bandpass filter 1FL3, etc.). Theory coverage for the nonrepairable modules is limited to the block diagram descriptions. All module interconnections are shown in the transmitter interconnecting diagram (fig. 8-14).

1-40. Power Supply 1A1 Circuit Theory

Power supply 1A1 contains the voltage regulator modules (1A1A1 through 1A1A4 and 1A1A6 through 1A1A12) which provide the dc supply and control voltages required in the transmitter. The power supply chassis (1A1A13) provides the following: a connector for each regulator module; an ac fuse at the input of each regulator module; and, a failure lamp and a test point at the output of each regulator module. Figure 8-16 illustrates the chassis mounted components and the module: connections. The circuit theory descriptions for the regulator modules are given in paragraphs 1-41 through 1-43.



NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A1A1, A2, A3, OR A4.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
5. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650729.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730.

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Figure 1-20. 5/6v regulator, 1A1A1 through 1A1A4, schematic diagram .

1-41. 5/6V Regulator 1A1A1 through 1A1A4 Circuit Theory
(fig. 1-20)

a. The rectified dc voltage from bridge rectifier CR1 through CR4 is filtered by capacitor C1 and applied to the collector of series regulator Q3. The series regulator, controlled by differential amplifier Q7, Q8, in conjunction with amplifiers Q4, Q5, Q6 and driver amplifier Q2, introduces a voltage drop which maintains voltage regulation at the emitter output. An overvoltage condition at the power supply output terminal is sensed by Q9, which triggers Q1. When triggered, Q1 short circuits the rectifier output causing the fuse in the ac input supply to blow. (This circuit is referred to as a crowbar configuration.)

b. The base of differential amplifier stage Q8 is clamped to 3.3 volts above ground by reference diode CR6 and diode current limiter R11. The voltage at the base of Q7 is determined by a voltage divider consisting of R5 and either R6 or R7. Variable resistor R6 or R7 is connected through the connector jumper to the power supply positive output lead pin 13. Resistor R6 is used when the regulator is to deliver 5 volts and resistor R7 is used when the regulator is to deliver 6 volts and permit adjusting the output voltage. The emitter resistor R9 is large to maintain a constant emitter current which is determined by the reference voltage. Since R9 is the common emitter resistor to both stages Q7 and Q8, changes in the operating conditions in one stage interact with the other stage. An increase of the Q7 base voltage above 3.3 volts causes the transistor to draw higher collector current. An increase in Q7 collector current causes an equal decrease in Q8 collector current. As a result, the voltage across R8 increases. The voltage developed across R8 is applied to the base of Q6 through base current limiting resistor R4. Collector current in Q6 increases raising the voltage across R3 and causing Q5 to conduct more. Due to the increase in current, the voltage across R2 rises and causes Q4 to conduct more. Since the current source for Q4 is through R1 the voltage at terminal 5 will decrease lowering the voltage at the base of Q2 and thereby decreasing its collector current. Transistor Q2 supplies base current to series regulator Q3, therefore, transistor drive is reduced which increases its collector to emitter voltage drop. Thus, the regulator output voltage is restored to the desired regulated level.

c. An overvoltage condition is sensed by Q9. The emitter of Q9 is clamped 3.3 volts below the output voltage by reference diode CR8; resistor R15 limits the current through CR8. The base voltage for Q9 is derived from the voltage divider consisting of R12, R13 and R14. When the regulator is configured to operate at 5 volts, resistor R14 is short circuited by connecting terminal K to the negative output lead. When the output is in regulation, the voltage at the base of Q9 is approximately 3.0 volts below the regulator output voltage. The emitter is clamped at 3.3 volts below the output voltage; therefore, the transistor is turned off. When the output voltage rises above the regulation level, the base of Q9 becomes negative with respect to its emitter and the transistor conducts. This gates on silicon-controlled rectifier Q1 and short circuits the rectifier output voltage. The short circuit current is limited by the transformer winding resistance.

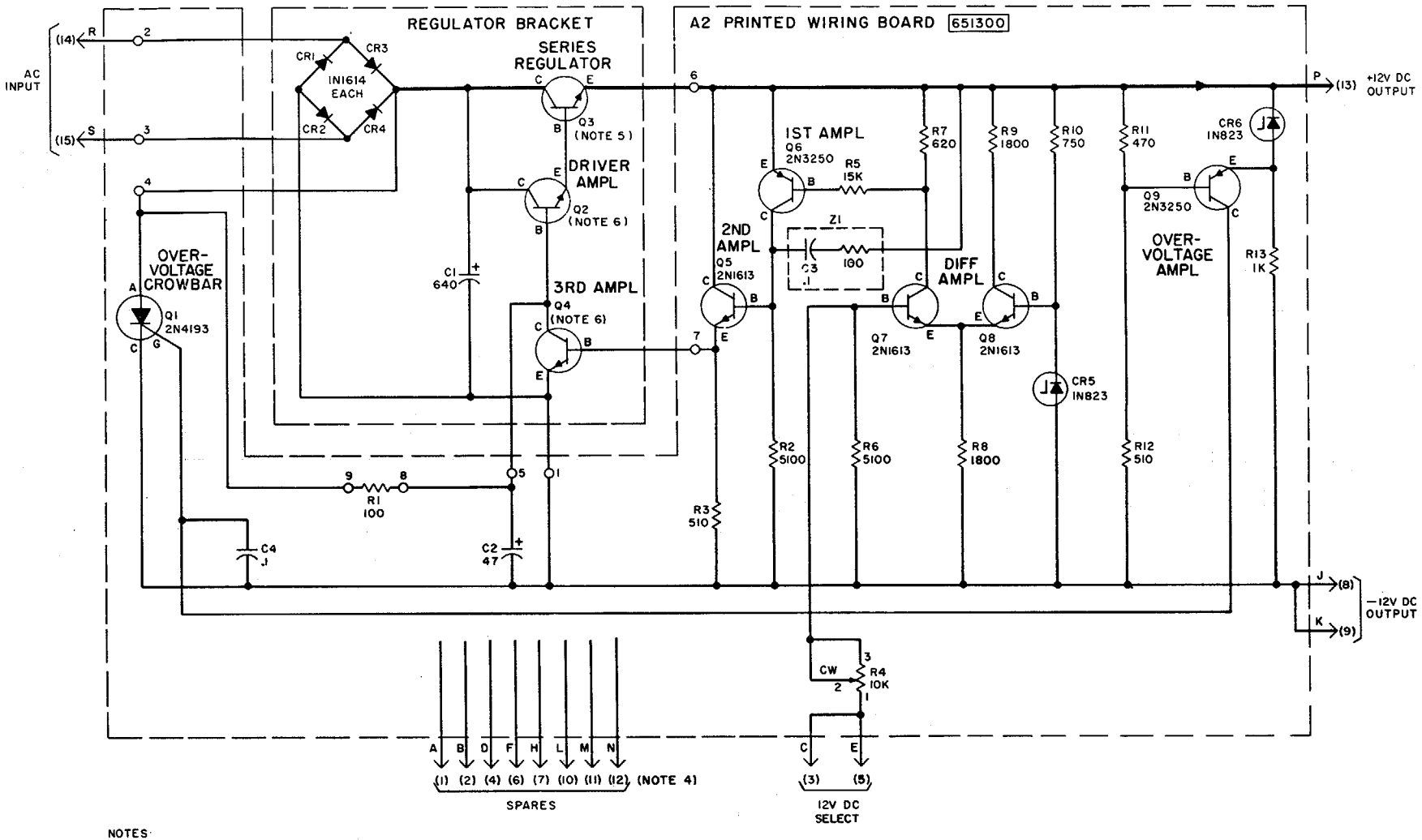
d. Oscillations and noise in the high gain feedback regulator are prevented by C2 and Z1. Capacitor C4 shunts any disturbances at Q2 base to ground. Capacitor/resistor Z1 supplies negative feedback to the base of Q6 to prevent oscillations. Capacitor C4 suppresses any noise which otherwise could trigger Q1 during normal operating conditions. Diodes CR5 and CR7 are temperature compensating diodes in the base circuits of Q7 and Q9.

1-42. 12V Regulator 1A1A6 through 1A1A9 Circuit Theory
(fig. 1-21)

This circuit functions the same as the 5/6v regulator previously described in paragraph 1-41. The difference between the circuits is that 6.2-volt Zener diode references are used (CR5 and CR6) in place of the 3.3-volt type (CR6 and CR8) used in the 5/6v regulator. Only one potentiometer (R4) is provided in the voltage divider path (R4 and R6) and the temperature compensating diodes in the base circuits of Q7 and Q9 are not used. The 12v regulator module is also used in position 2A3A3 of the receiver power supply.

1-43. 15-28V Regulator 1A1A10 through Circuit Theory
(fig. 1-22)

This circuit functions the same as the 5/6v regulator previously described in paragraph 1-41. The difference between the circuits is that 6.2-volt Zener diode references are used (CR5 and CR6) in place of the 3.3-volt type (CR6 and CR8) used



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A1A6 THROUGH A9 OR 2A3A3.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
5. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650729.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730.

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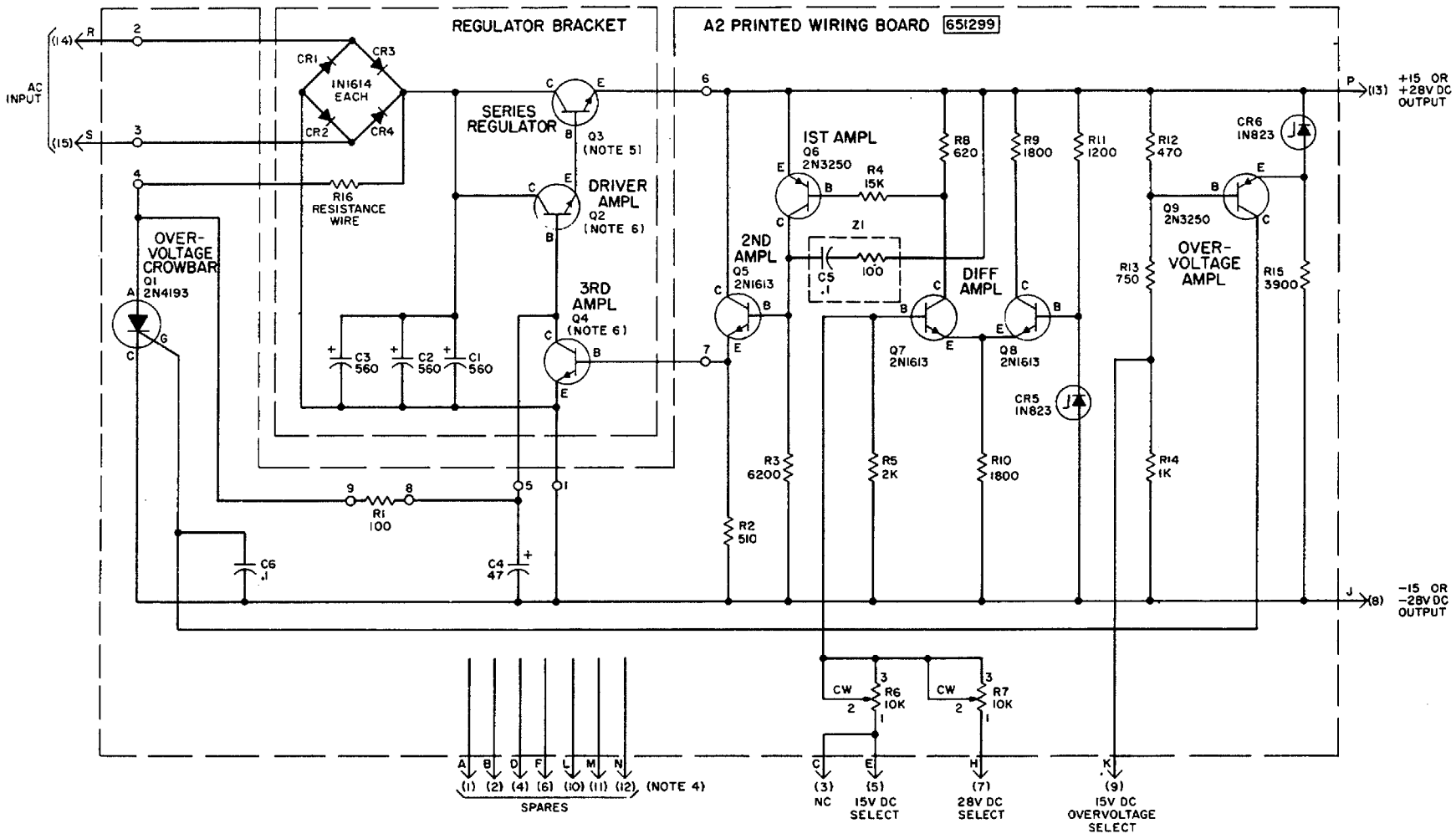
Figure 1-21. 12v regulator, 1A1A6 through 1A1A9 and 2A3A3, schematic diagram.



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A1A10 THROUGH 1A1A12 OR 2A3A1, 2A3A2 OR 2A3A4.
3. ☐ INDICATES MARKING ON EQUIPMENT.
4. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
5. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650729.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650730.

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Figure 1-22. 15/28v regulator, 1A1A10 through 1A1A11, 2A3A1A, A2, and A4, schematic diagram.

in the 5/6v regulator. Also, certain circuit resistance values are also different to accommodate the higher voltages in this module and the temperature compensating diodes in the base circuits of Q7 and Q9 are not used. In addition, resistor R16 is required to limit the "crowbar" current. The 15/28v regulator is also used in positions 2A3A1, 2A3A2, and 2A3A4 of the receiver power supply.

1-44. 100-MHz Rf Oscillator 1 A2 Circuit Theory
(fig. 8-17)

a. The 100-MHz RF oscillator (1A2), part of the radio test set, produces a precise 100-MHz signal, which is mixed with the output signal of the transmitter to produce a signal offset by 100 MHz from the transmitter frequency. The signal is used in aligning, testing and troubleshooting the receiver. The basic oscillator consists of transistor Q1, crystal Y1, and tank circuit (L3, C7, C10). Crystal Y1 operates in series resonance on the fifth overtone. Transistor bias is provided by resistors R3, R4 and RS. Resistor R5 is also in the oscillator's feedback path. Inductor L4 tunes out stray capacitance in the crystal unit. Capacitor C6 provides RF bypass. Dc power is applied through switch S1, and two filter sections (L1, C1, C3 and L2, C4, C5). The switch also controls ON-OFF signal lamps on the transmitter meter panel and ON-OFF lamp DS1 on oscillator module 1A2 through current dropping resistor R2.

b. When voltage is applied, the starting transient causes oscillations to start. Crystal oscillations are fed to the emitter of Q1, amplified in the transistor, and applied to the tank. The tank, closely tuned to the crystal frequency, resonates and feeds a reinforcing signal to the crystal through C8. The signal builds up in the loop until the transistor gain has decreased to unity, at which point a sustained level is maintained. Small changes are made in operating frequency by means of variable capacitor C10 in the tank circuit. When the tank circuit is tuned to resonate above the natural frequency of the crystal, the feedback signal to the crystal leads the crystal signal. This causes the crystal to oscillate at a higher frequency and restores a zero phase condition. Since the crystal Q is very high compared to that of the tank, the change in crystal frequency required to restore zero phase is very small relative to the change in resonant frequency in the tank circuit. The oscillator output is taken off at the upper tap of L3, through coupling capacitor C9. The output level is controlled by resistor R6 and variable resistor R7. The signal is fed to a divider network (R10, R11, R12, R13, R14) which also isolates the oscillator from the load. Each output is coupled through blocking capacitor C13 (C14) to the output cable W1 (W2). These cables are connected to balanced mixer unit 1Z1. The blocking capacitors prevent diode currents in the mixer from feeding back to the oscillator stage.

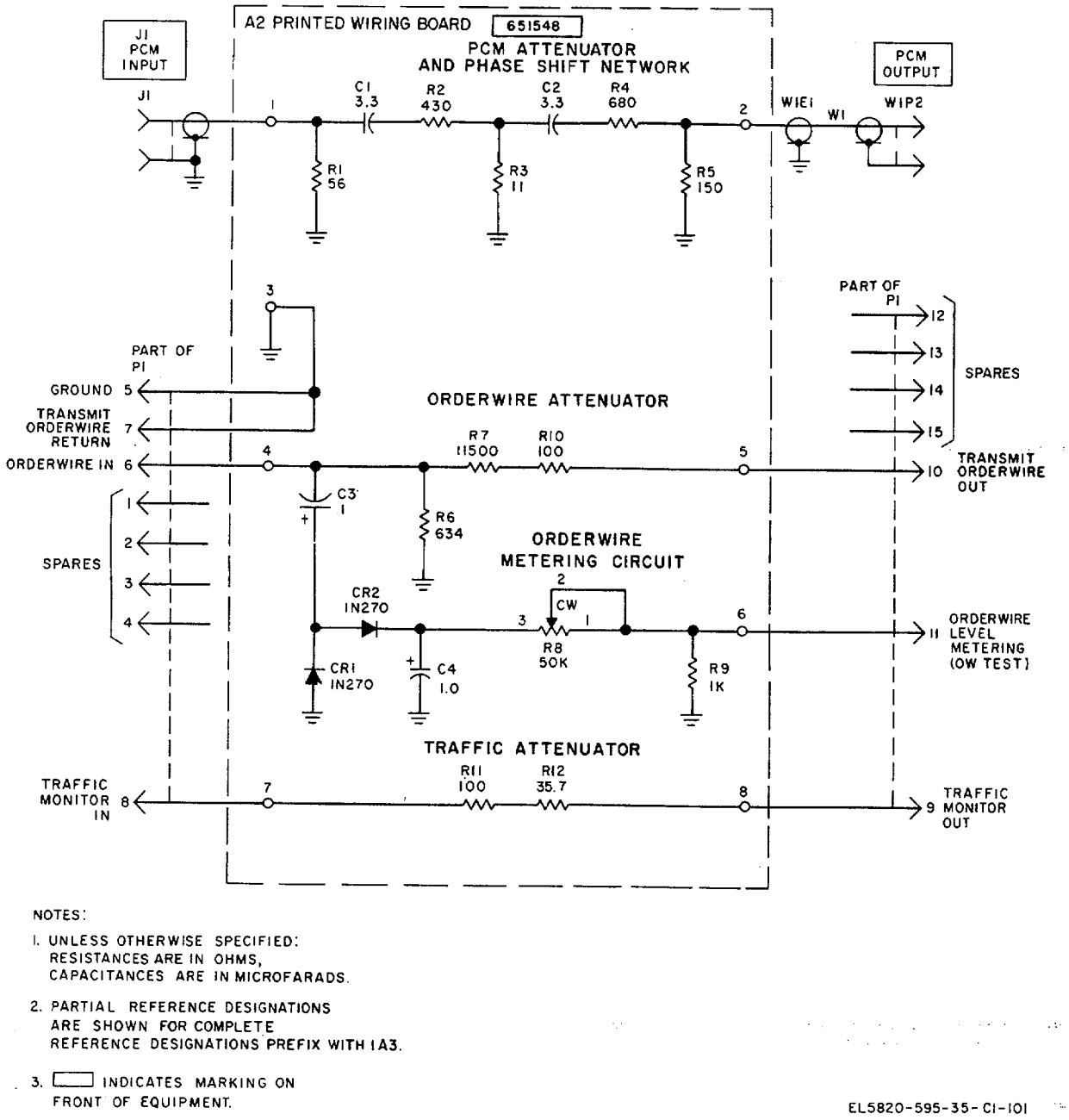
c. Several metering circuits are provided. A level detector circuit, consisting of CR1, R8, and variable R9 is capacitively coupled by C11 to the variable arm of R7. This circuit produces a dc level proportional to the signal level. The dc level (osc output level) is applied to the meter selector switch on the radio test set panel. Resistor R9 is used to adjust the meter deflection and capacitor C12 as an RF bypass. Circuits for metering the crystal mixer currents in mixer 1Z1 are also provided. The CR1 metering and CR2 metering outputs are applied to the meter selector switch on the radio test set panel. Since the metering circuits are identical, only the CR1 metering circuit is described. Blocking, bypassing, and filtering is accomplished by L5, C15, C17, C19 and L7. These components prevent loading of the RF signal and also prevent RF from appearing at the output. R15 and R17 comprise a voltage divider which established the proper level for the meter. TP1 provides a means to monitor the B+ voltage (+ 15v). Resistor R1 serves as a dropping resistor and capacitor C2 serves as an RF bypass.

1-45. Pcm Attenuator 1A3 and 1A18 (12 and 24 Channel), Circuit Theory
(fig. 1-23 and 1-24)

a. The pcm attenuators adjust the input level to the modulator to produce the proper fm deviation for the selected channel capacity. The 12-channel pcm attenuator, in conjunction with the gain setting on AF-RF amplifier 1A4, establishes an input of 9 millivolts rms for a 250-kHz peak deviation of the modulator. The 24-channel pcm attenuator, in conjunction with the gain setting on AF-RF amplifier 1A4, establishes an input of 18 millivolts for a 500kHz peak deviation of the modulator.

b. The 12 channel pcm attenuator is shown in figure 1-21. The pcm attenuator and phase shift network circuit consists of R1, C1, R2, R3, C2, R4 and R5. This network provides 52 db attenuation of the incoming pcm signal. Its input impedance is 50 ohms resistive and its output impedance 150 ohms resistive. The complete circuit provides 29

degrees phase shift at 300 Hz. The order wire attenuator consists of R6, R7 and R10. This network has a 600-ohm input impedance and attenuates the order wire level so that its magnitude is 15 to 20 percent of the pcm level at the point where the pcm and order wire signals are added together in AF-RF amplifier 1A4. The transmit order wire, signal is coupled by C3, detected by diodes CR1 and CR2, filtered by C4, and attenuated by the combination of variable R8 and R9. The output dc is applied via P1-11 to the order wire level position on the transmitter meter panel. Resistor R8 is used to calibrate this metering level. A detected sample of the pcm plus order wire traffic is derived in modulator 1A8 and coupled back through traffic attenuator R11, R12



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE REFERENCE DESIGNATIONS PREFIX WITH 1A3.
3. ▭ INDICATES MARKING ON FRONT OF EQUIPMENT.

Figure 1-23. 12-channel pcm attenuator 1AJ, schematic diagram.

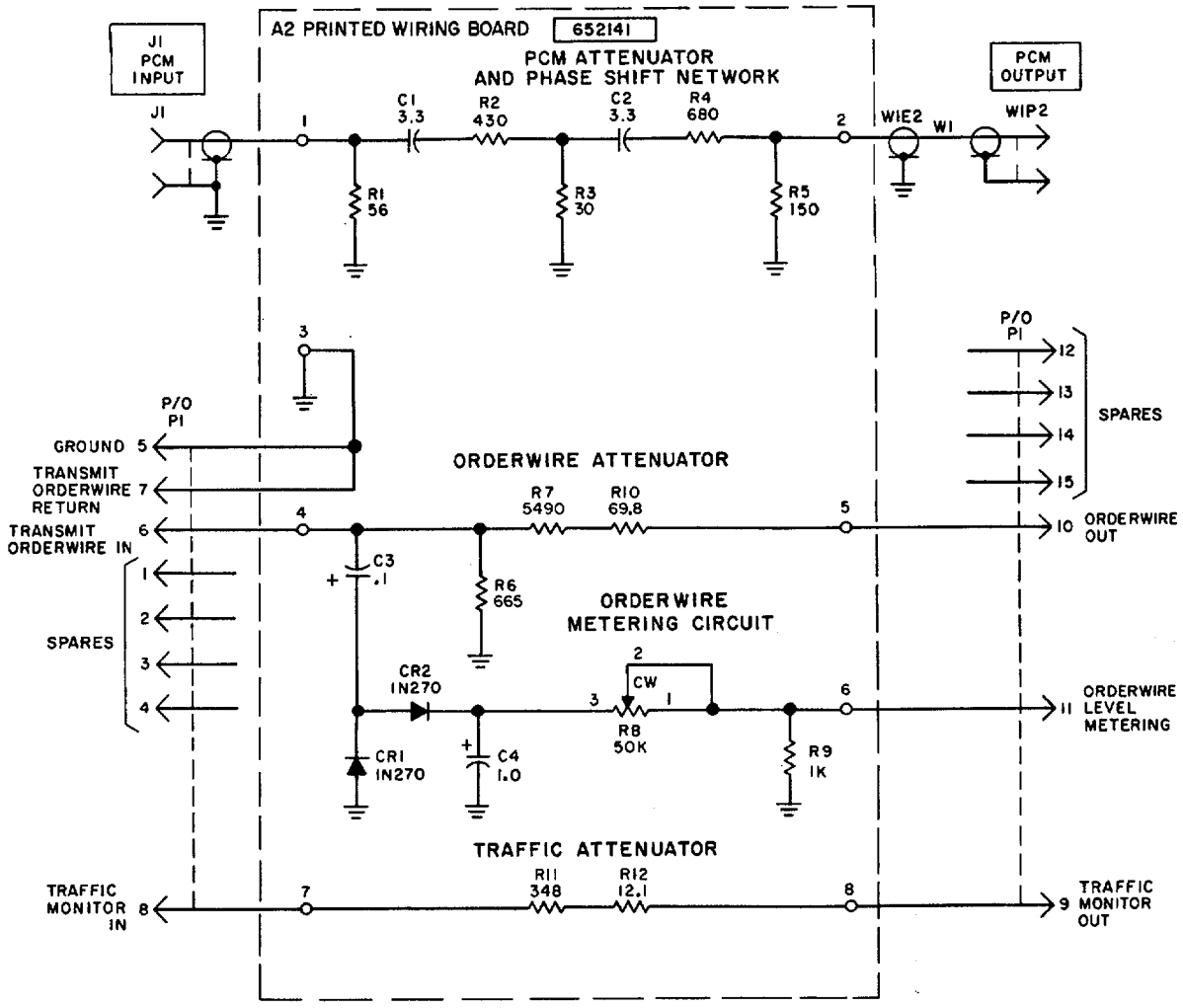
in pcm attenuator 1A3 and coupled to the traffic monitor in alarm monitor 1A5.

c. The 24-channel pcm attenuator is shown in figure 1-24. The pcm attenuator and phase shift network circuit consists of R1, C1, R2, R3, C2, R4 and R5. This network provides 42 db attenuation of the incoming pcm pulse train. Its input impedance is 50 ohms resistive and its output impedance is 150 ohms resistive. The complete circuit provides 29 degrees phase shift of 300 Hz. The order wire attenuator and traffic attenuator networks function the same as described in b above except the component values are changed to accommodate the higher levels of modulator deviation.

1-46. AF-RF Amplifier 1A4 Circuit Theory

(fig. 1-25)

AF-RF amplifier 1A4 is a wide band video amplifier which provides a continuously adjustable gain



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE REFERENCE DESIGNATIONS PREFIX WITH 1A18.
3. ☐ INDICATES MARKING ON EQUIPMENT.

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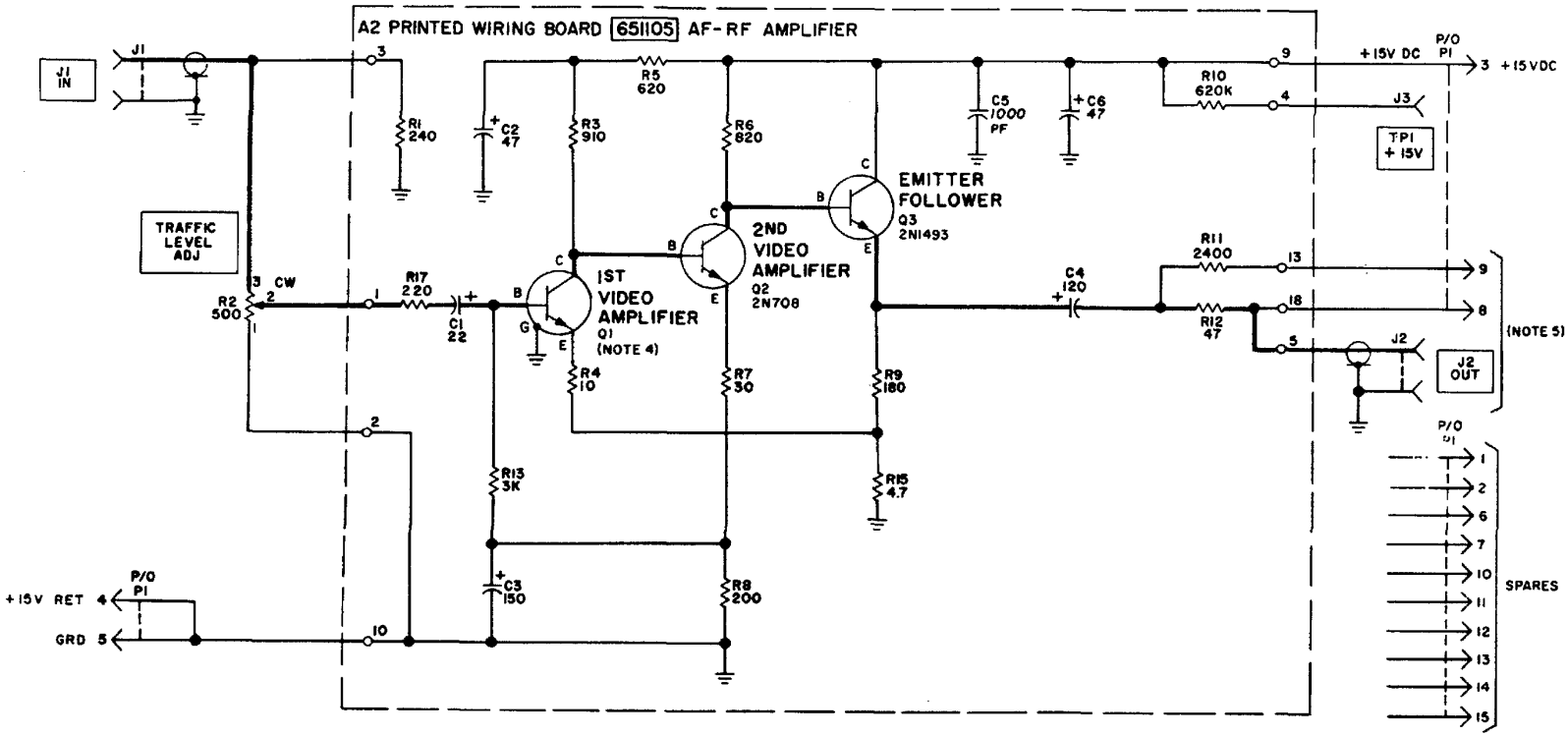
Figure 1-24. 24-channel pcm attenuator 1A18, schematic diagram.



RECEIVER	
CONNECTOR	FUNCTION
J1 IN	PCM/ORDERWIRE
J2 OUT	TRAFFIC OUT
P1 PIN 9	TRAFFIC MONITOR
P1 PIN 8	NOT USED
TRANSMITTER	
CONNECTOR	FUNCTION
J1 IN	PCM
J2 OUT	TRAFFIC OUT
P1 PIN 8	ORDERWIRE IN
P1 PIN 9	NOT USED

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS.
2. *PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:*
   PREFIX THE PARTIAL REFERENCE DESIGNATIONS WITH 1A4 OR 2A19.
3. ☐ INDICATES MARKING ON EQUIPMENT.
4. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-653211.
5. REFER TO TABLE FOR FUNCTIONAL IDENTIFICATION OF RECEIVER AND TRANSMITTER SIGNALS.

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Figure 1.-5. AF-RF amplifier 1A4/1A19, schematic diagram

(TRAFFIC LEVEL ADJ control) to a maximum of 25 db. The AF-RF amplifier consists of first video amplifier Q1, second video amplifier Q2, and emitter follower Q3. The B+ supply (+15 vdc) is provided via P1-3. Three decoupling capacitors (C2, C5, and C6) are used in the B+ circuit to remove ac ripple from the circuit. Test point TP 1 (+ 155v) can be connected to the transmitter meter with a test lead. Resistor R10 is a metering resistor.

NOTE

The AF-RF amplifier is also used in the receiver in module position 2A19 (para 1-110).

a. 1st Video Amplifier. The pcm signal from pcm attenuator 1A3 is applied to input jack J1 IN. TRAFFIC LEVEL ADJ potentiometer R2 determines the input level of the pcm signal coupled through C1 to the base of first video amplifier Q1. The input impedance is 150 ohms (parallel combination of R1, R2, and input impedance of first video amplifier Q1). Transistor (Q amplifies the pcm signal which is direct coupled to the base of second video amplifier Q2. Resistor R17, in the base circuit of Q1, stabilizes the input impedance of Q1. Resistor R3 is the collector load for transistor Q1 and resistor R5 provides decoupling negative feedback to reduce distortion. A feedback path is used from the emitter of Q3 (junction of R9 and R15) to the emitter circuit (R4) of Q1. A feedback path is also used from the emitter circuit (junction of R7 and R8) of Q2 to the base circuit (junction of R13 and C3) of Q1.

b. 2nd Video Amplifier. Second video amplifier Q2 amplifies the pcm signal. The amplified output is direct coupled to the base of emitter follower Q3. Resistor R6 is the collector load. Resistors R7 and R8 are in the emitter circuit of Q2. C3 is an ac bypass capacitor.

c. Emitter Follower. Emitter follower Q3 provides an impedance match between the second video amplifier and the output. Q3 also provides negative feedback to Q1. The amount of negative feedback determines the overall gain and bandwidth of the AF-RF amplifier. The pcm signal is coupled (C4, R12) from the emitter of Q3 to output jack J2 (J2 OUT). The transmit order wire input signal from pcm attenuator 1A3 is also routed to the J2 OUT jack via P1-8. Thus, the order wire signal is added to the amplified pcm signal and the combined pcm and order wire signal is routed to the 1.3-MHz low pass filter (1A6) via the J2 OUT jack. The alarm output (P1-9) is not used in AF-RF amplifier 1A4.

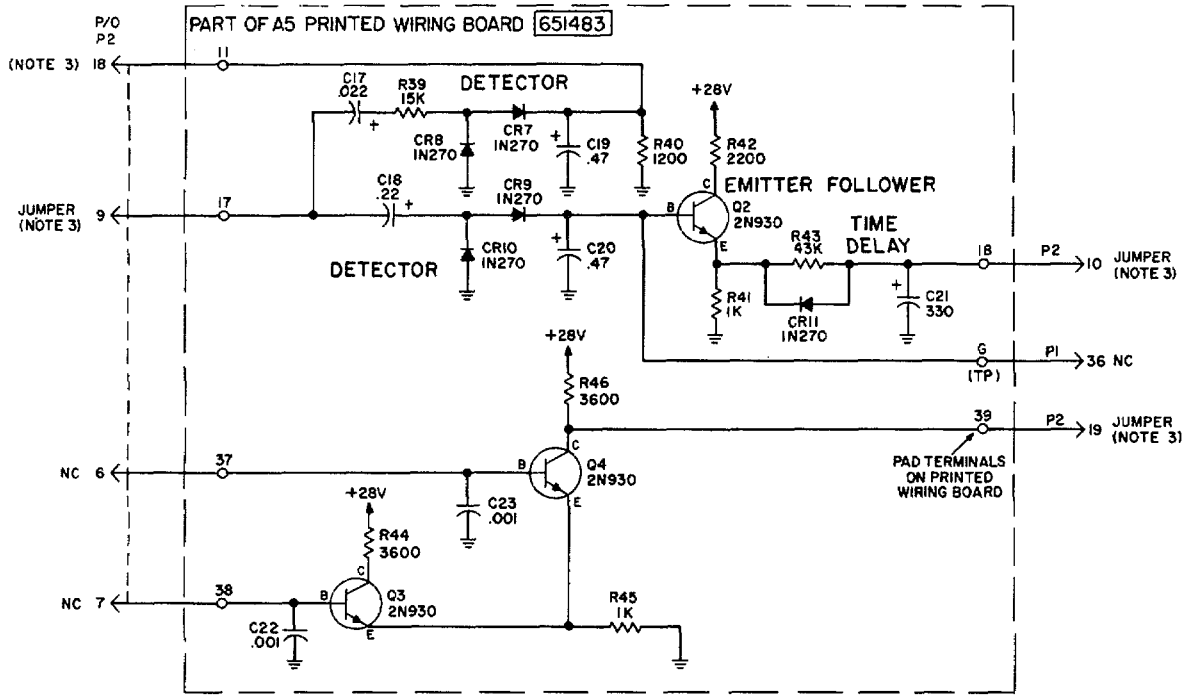
1-47. Alarm Monitor lA5, Circuit Theory
(fig. 1-26)

a. The alarm monitor input circuits are shown in figure 1-24. Low level alarm monitor input signals are amplified by operational amplifiers AR1, AR2 and AR3. Operational amplifiers AR1, AR2, and AR3 are type µA702A integrated circuits (fig. 8-18 (1)). The amplifiers are connected in different configurations to accommodate each particular transmitter alarm monitor input signal. The inverting input of the integrated circuit amplifier is pin 2, the non-inverting input is pin 3, and the output signal is taken from pin 7. The feedback resistance connected from the output pin 7 to the inverting input pin 2 establishes gain of the amplifier.

NOTE

The alarm monitor module is also used in the receiver in module position 2A20 (para 1-111).

b. The traffic monitor signal from pcm attenuator 1A3 is coupled in pin A3 to the inverting input pin 2 of amplifier AR1 (fig. 1-26 (). The network consisting of C1 and R4 connected across the differential inputs (pins 2 and 3) provides lag compensation which increases the high frequency response. The amplified traffic signal is applied to a diode peak detector circuit consisting of capacitors C4, C5 and diodes CR1 and CR2. The positive peak-detected dc voltage forward biases emitter follower stage Q1 which couples the signal through an attenuator network R10, R11 and R12 to its associated Schmitt trigger circuit on board A5 (fig. 1-24 (2)). The Schmitt trigger circuit for the traffic monitor signal consists of transistors Q5 and Q6.. When no signal is present, transistor Q6 conducts and holds transistor Q5 off due to the voltage developed across common emitter resistor R48. The incoming peak-detected traffic monitor signal will forward bias transistor Q5 when the magnitude of the peak-detected traffic signal exceeds the magnitude of the voltage developed across common emitter resistor R48. When this occurs, the states will reverse with transistor Q5 conducting and transistor Q6 off until the peak detected signal again drops below the voltage level of the common emitter resistor R48. The output of the Schmitt trigger (Q5, Q6) is a series of positive square pulses which are developed at the collector of transistor Q6. These pulses are applied to the base of inverter stage Q7 and forward biases it into condition. When inverter Q7 is conducting, its collector is at a low level; this provides a low impedance path to ground to light



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 1A5 OR 2A20
3. THE ALARM MONITOR MODULE IS USED IN TRANSMITTER MODULE POSITION 1A5 AND RECEIVER MODULE POSITION 2A20. REFER TO THE TABLES I THROUGH III TO DETERMINE THE CONNECTIONS USED FOR EACH MODULE POSITION. TABLE I LISTS P2 CONNECTIONS, TABLE II LISTS P1 CONNECTIONS AND TABLE III LISTS THE JUMPER CONNECTIONS MADE ON THE MATING CONNECTORS AT EACH MODULE POSITION. FUNCTIONS FOR P1 AND P2 THAT DO NOT CHANGE IN THE MODULE POSITIONS ARE SHOWN ADJACENT TO THE PIN CONNECTIONS.

TABLE I

CONNECTION	SIGNAL NAME	
	TRANSMITTER (1A5)	RECEIVER (2A20)
P2 — 13	NOT USED	TRAFFIC MONITOR
P2 — A3	TRAFFIC MONITOR	NOT USED
P2 — A1	NOT USED	VCO LOCK MON-A
P2 — A2	NOT USED	VCO LOCK MON-B
P2 — 14	REFLECTED POWER MONITOR	NOT USED
P2 — 15	REFLECTED POWER METER	NOT USED
P2 — 2	RF POWER MONITOR	NOT USED
P2 — 4	RF POWER METER	NOT USED
P2 — 18	NOT USED	VCO FREQUENCY DIFFERENCE METER
P2 — 20	NOT USED	CARRIER (IF) MONITOR-A LEVEL
P2 — 22	NOT USED	CARRIER (IF) MONITOR-A LEVEL
P2 — 16	NOT USED	CARRIER LEVEL-B

TABLE II

CONNECTION	SIGNAL NAME	
	TRANSMITTER (1A5)	RECEIVER (2A20)
P1 — 29	REFLECTED POWER ALARM	VCO LOCK ALARM
P1 — 30	REFLECTED POWER NORMAL	VCO LOCK NORMAL
P1 — 26	RF POWER NORMAL	NOT USED (SPARE ALARM)
P1 — 25	RF POWER ALARM	NOT USED (SPARE NORM)
P1 — 14	NOT USED	CARRIER (IF) A NORM
P1 — 15	NOT USED	CARRIER (IF) A ALARM
P1 — 23	NOT USED	CARRIER (IF) B NORM
P1 — 20	NOT USED	CARRIER (IF) B ALARM

TABLE III

JUMPER CONNECTIONS	
TRANSMITTER (1A5)	RECEIVER (2A20)
P1 — 24 TO P1 — 27	P1 — 12 TO P1 — 13
P1 — 28 TO P1 — 31	P1 — 21 TO, P1 — 22
P2 — 8 TO P2 — 11	P1 — 28 TO P1 — 31
	P2 — 8 TO P2 — 9
	P2 — 10 TO P2 — 11

EL5820-595-35-CI-4 (1)

Figure 1-26(1). Alarm monitor 1A5/2A20, schematic diagram (part 1 of 3).

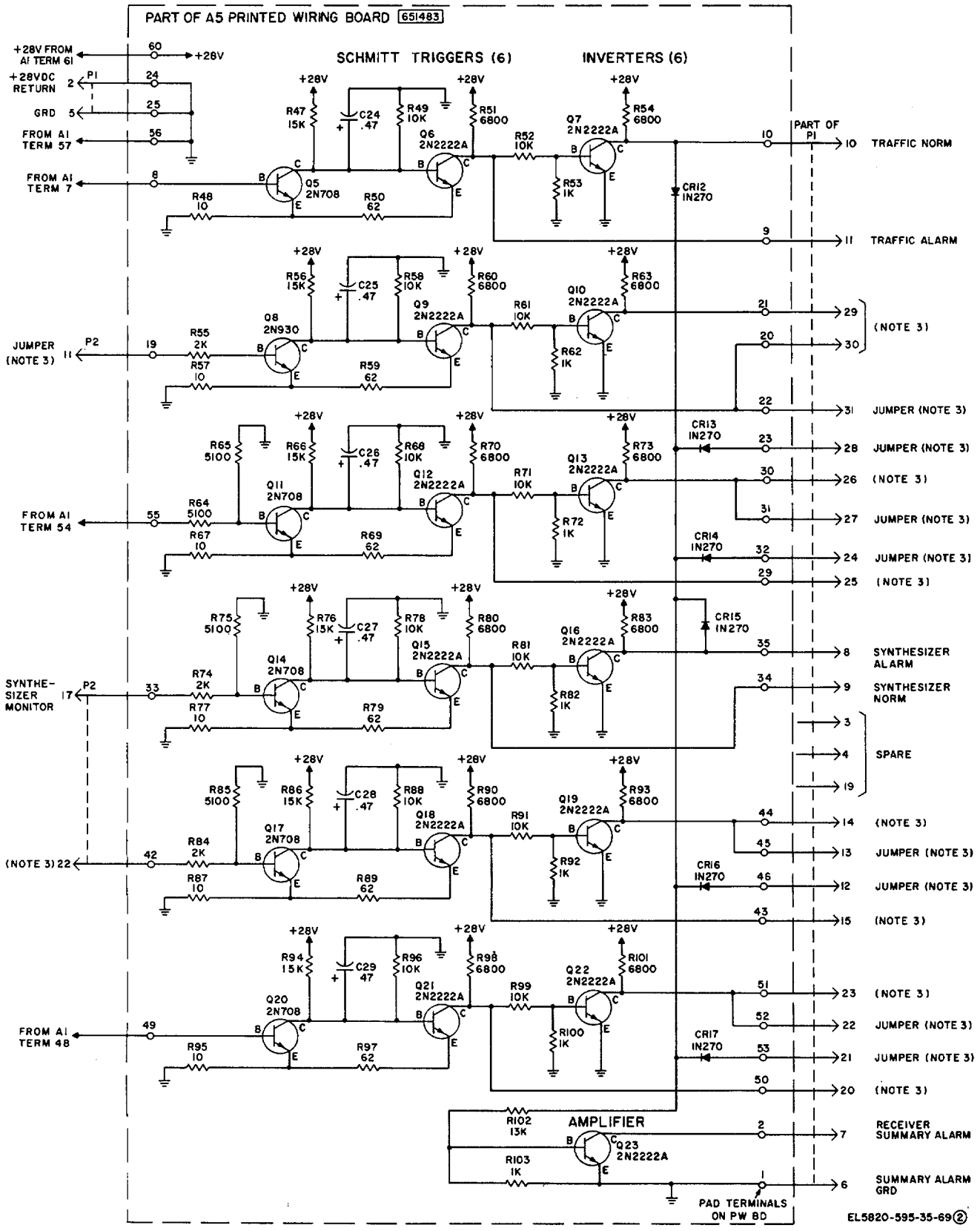


Figure 1-26 (2). Alarm monitor 1A5/2A20, schematic diagram (part 2 of 3).

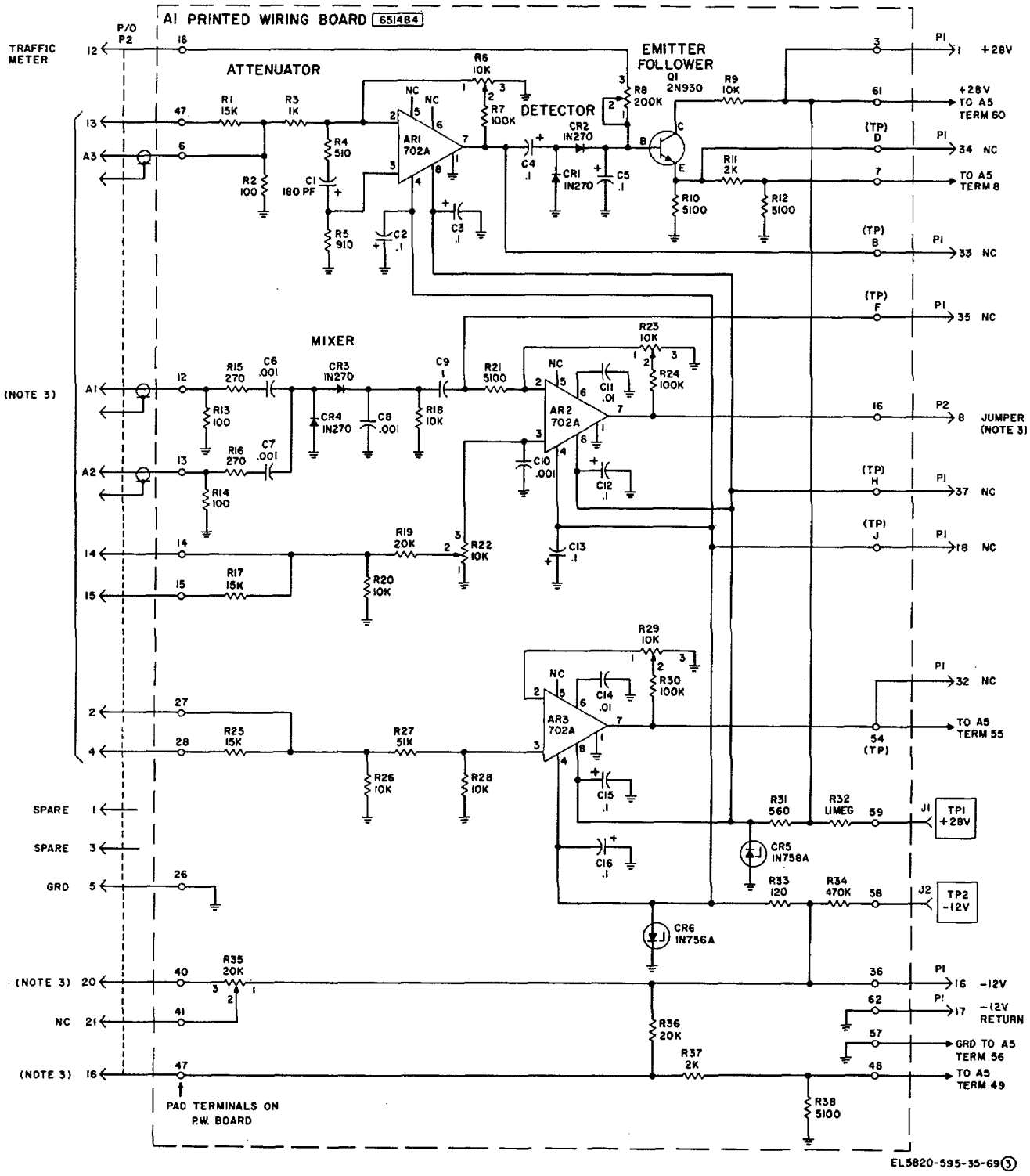


Figure 1-26 (3). Alarm monitor 1A5/2A20, schematic diagram (part 3 of 3).

the normal (green) TRAF indicator lamp on transmitter meter panel. When no traffic monitor signal is detected and Q6 is conducting to hold Q5 off, the low level output of Q6 collector provides a low impedance path to ground for alarm (red) TRAF indicator amp.

c. The reflected RF power monitor signal is developed by a diode detector in directional coupler 1DC2 and coupled in pin 14 to the non-inverting input pin 3 of operational amplifier AR2 (fig. 1-24 (3)). Resistors R19, R20 and potentiometer R22 provide a variable pad at the amplifier input. The incoming detected signal is also coupled through resistor R17 and out pin 15 to the meter selector switch. Capacitor C10, at the non-inverting input, integrates the input signal which is amplified and is coupled to the input of its associated Schmitt trigger circuit by a jumper wire from pin P2-8 to pin P2-11 through series resistor R55 (fig. 1-26 (2)). The Schmitt trigger circuit consists of transistors Q8 and Q9 which functions in an identical manner to Schmitt trigger Q5 and Q6 previously described in b above with the exception that the normal indication is taken from the collector of Q9 and the alarm indication is taken from the collector of Q10. The presence of an input signal (high reflected power) will cause an alarm indication, the absence of an input signal (low reflected power) will produce the normal indication.

d. The RF power monitor signal representing a sample of the forward power is developed by a diode detector in directional coupler 1DC2 and coupled in pin 2 to the non-inverting input pin 3 of operational amplifier AR3 (fig. 1-26 (3)). Resistors R26, R27 and R28 in the signal input path are a pad that provides approximately 15 db of attenuation. The amplified output from operational amplifier AR3 is connected via a jumper between terminal E54 and terminal E55 to the base of transistor Q11 (fig. 1-26 (2)). Transistors Q11 and Q12 form a Schmitt trigger circuit that functions in a similar manner to Q5 and Q6 previously described in b above. When the RF power is above a minimum threshold level, established by the setting of the input attenuator, output transistor Q13 is conducting and provides a low impedance ground path for the normal indicator. When no signal is present transistor Q12 is conducting and provides a low impedance ground path for the alarm indicator.

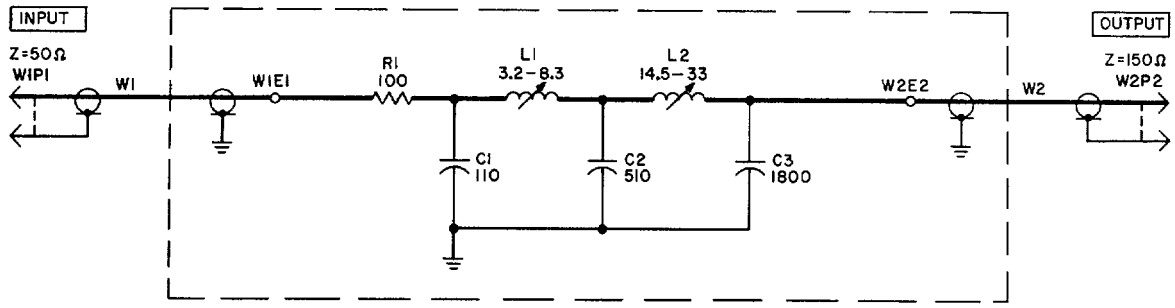
e. A synthesizer monitor signal is developed in frequency synthesizer 1A14 and applied as an input to transistor Q14 via pin P2-17 (fig. 1-26 (2)). This signal indicates when the frequency synthesizer is not phase-locked and is in a search mode attempting to correct the oscillator frequency. The Schmitt trigger consists of transistors Q14 and Q15. When the frequency synthesizer is phased-locked, a plus 2-volt level is applied to input pin 17 to forward bias transistor Q14. This in turn, cuts off transistor Q15 and turns on transistor Q16 providing the normal (green) indication. When the frequency synthesizer is not phase-locked, the input signal drops to zero volts which turns on transistor Q15 producing the alarm (red) indication.

f. A six-input diode OR gate and inverting transistor provides the summary alarm function. This circuit consists of diodes CR12 through CR17, transistor Q23 and resistors R102 and R103 (fig. 1-26 (2)). When the anode of any input diode has a positive voltage level applied to it, it conducts and forward biases transistor Q23 into conduction producing a summary alarm condition. When all of the diodes have a low (or zero) voltage applied to their anodes, they are non-conducting and transistor Q23 is turned off producing a normal indication.

g. Two Zener diodes are incorporated on board Al, these provide regulated plus and minus voltages for the integrated circuits (fig. 1-26 (3)). Zener diode CR5 in conjunction with resistor R31 provides a regulated plus 10 volts. Zener diode CR6, in conjunction with resistor R33 provides a regulated minus 8.2 volts.

1-48. 1.3-MHz Low Pass Filter 1A6, Circuit Theory (fig. 1-27)

The 1.3-MHz low pass filter is incorporated in the combined order wire/pcm signal path to modulator 1A8. This filter shapes the pulses before frequency modulation. It is a five-pole low pass filter and is tuned to approximate Gaussian shaping. The 3 db bandwidth of the filter is 1.3 MHz. At 1.84 MHz the filter attenuation is G db and at 3.6 MHz it is 20 db. The attenuation increases with frequency and at higher frequencies provides 40 db attenuation. Source impedance is 50 ohms and load impedance is 150 ohms. Circuit components L1, L2, and C1, C2, C3 are the poles of the filter. Resistor R1 provides impedance matching.



NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN PICOFARADS
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATION WITH 1A6.
3. ☐ INDICATES MARKING ON EQUIPMENT.

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Figure 1-27. 1.8-MHz low pass filter 1A6, schematic diagram.

1-49. Electronic Frequency Control 1A7 Circuit Theory

(fig. 8-19)

Electronic frequency control 1A7 produces an afc signal which stabilizes the center frequency of the 150 MHz vco in modulator 1A8. The electronic frequency control module is comprised of the following circuits: 70-MHz frequency modulated input, reference crystal oscillator, multivibrator, amplifier-limiter chain, discriminator driver, ac amplifier, and phase detector.

a. 70-MHz Frequency Modulated Input. The 70-MHz frequency modulated signal (FREQ CONT INTERCONN) from modulator 1A8 is applied to emitter follower Q3 via coupling capacitor C5 and connector J1 (INPUT). This stage isolates the input from the load. Resistor RS, which is RF grounded by capacitor C9, provides the proper termination at the input. The stage is biased by resistors R9, R10, and R26. The output from R11 is fed to a diode gate through C14. C27 and C30 are bypass capacitors. L9 is an RF choke. The gate consists of series diodes CR4, CR5, CR6, coupling capacitors C21, C22, and load resistors R18, R19. Gate configuration provides isolation to prevent signal distortion when conducting. Approximately 3 vdc is impressed on the cathode of CR6 from a voltage divider consisting of R12 and R13 (L8 is an RF choke). Depending on the operating state of Q5, the anode of CR4 is at either approximately +14 volts (Q5 cut off) or below 1.0 volt (Q5 saturated). When this voltage is high, the diodes are forward biased, and the signal from Q3 appears at the output. With CR4 anode low, the diodes are reverse biased, and no signal flows.

b. Reference Crystal Oscillator. The reference crystal oscillator generates a precise 70-MHz reference signal, which is compared with the sample 70-MHz signal from the modulator 1A8. The oscillator stage is comprised of transistor Q1, crystal Y1, tank circuit C7 and L2, bias resistors R1, R2, R3, R5 and R6, loading resistor R4, RF choke L1, bypass capacitors C1, C2, C3, and C10, and coupling capacitor C4 and C6. The crystal operates in series resonance on the fifth overtone. When voltage is applied, the starting transient causes oscillations to start. The crystal signal at Q1 emitter causes an amplifier signal to appear at Q1 collector. The tank circuit which is tuned closely to the crystal frequency, resonates and feeds a reinforcing signal back to the crystal through C6. This causes further buildup in the signal level of the tank, and increased feedback to the crystal. This increase in level continues until the transistor gain drops to unity, at which time a sustained level is maintained. Variable inductor L2 in the tank is used to adjust the frequency of oscillation by a small percentage. With the tank tuned above the crystal frequency, the tank appears capacitive to the signal at the collector, causing the feedback signal to lead the crystal

frequency. The crystal pulls to a higher frequency to restore a zero phase condition. Since the crystal has a very high Q, while that of the tank is quite low, the crystal frequency shift is very small compared to that of the tank. The crystal oscillator is dc coupled to emitter follower Q2 through resistor R75. The collector is isolated from +15 volts by L3 and C11. This stage decouples the oscillator from the following circuit. The output is taken off at the junction of bias resistors R14 and R15, and is coupled to a diode gate through capacitor C12. The gate circuit consists of series diodes CR1, CR2, CR3, coupling capacitors, C19, C20, load risistors R16, R17, and decoupling networks L5, C13, and L7, C18. The operation of this gate is identical to the CR4, CR5, and CR6 gate previously described.

c. Multivibrator. The multivibrator is a symmetrical, free running multivibrator consisting of transistor stages Q4 and Q5. Its function is to supply gating signals to the previously described diode gates. These signals consist of positive rectangular pulses appearing alternately at the Q4 and Q5 collectors. When the pulse is present at Q4 collector, diode gate CR1, CR2, CR3 is enabled. During this period the pulse is absent at Q5 collector, so that its associated gate, CR4, CR5, CR6 is open. The multivibrator drive to the gates is applied through S1. When this switch is in the OPR position, the gates are under control of the multivibrator. In the TEST position, the multivibrator is disconnected and CR4, CRS, CR6 gate is held on by the +15 volts applied through R7.

(1) When voltage is applied, one transistor conducts more heavily due to noise or small component variations. For discussion purposes, assume that Q4 is initially conducting. Q4 collector voltage drops from +15 volts to alower value. Since the charge across a capacitor cannot change instantaneously, the voltage at the negative plate of C15 drops causing Q5 base voltage to decrease. Q5 conduction decreases, and its collector voltage rises.. This increase is coupled to Q4 base through capacitor C23 causing the Q4 collector current to increase further. This loop is repeated until Q5 is driven below cutoff, and Q4 goes into saturation. The above occurs so rapidly that the resulting ware is essentially a step function. CR8 is now forward biased and current flows through it and resistors R21, R24, and R25 to ground. As a result, Q5 collector is at approximately +14 volts and the drop across R25 is approximately +13 volts. Diode CR7 is reverse biased and therefore blocks the + 13 volts from Q4 collector.

(2) Since the charge across C15 and the bias of R25 are aiding, C15 discharges through Q4, R25 and R23, in an exponential fashion. Then Q5 reaches cutoff, it begins to conduct, causing its collector voltage to drop, pulling down Q4 base. Q4 collector voltage increases, and this increase is coupled back to Q5 base through C15. The feedback process as previously described results, but, in the reverse order, causing Q4 to be cut off and Q5 to go into saturation. CR7 is now forward biased and current flows through it and resistors R20, R24, and R25 to ground. The charge across C23 discharges through Q5, R25, and R22. Thus, a square wave is produced alternately at the Q4 and Q5 collectors.

d. Amplifier-Limiter Chain. The amplifier-limiter chain is comprised of transistor stages Q7 through Q11. The two diode gates, previously described, provide alternate input signal to the amplifier; limiter chain. This results in the 70-MHz frequency modulated signal from the modulator (1A8) and the 70-MHz reference signal from the crystal oscillator appearing alternately at the junction of C25 and C26. Since the multivibrator is symmetrical, these signal samples are of equal duration.

(1) Each signal sample is impressed across gate load resistor R29 at the base of emitter follower Q7, through coupling capacitor C29. Q7 is biased by R28, R30 and R31, the latter also serving as the emitter load. C28 and C32 are bypass capacitors and L10 provides decoupling. C34 prevents oscillation. The output of Q7 is coupled, via C37, to limiter stage Q8, which is in the common base configuration. Inductor L12 is used to tune the collector to the signal frequency. L11 provides isolation and C33, C35, and C36 are bypass capacitors.

(2) Q8 operates with approximately 12.2 volts fixed bias on the base, dervied from voltage divider R32 and R33. The emitter current through R34 and R35 produces a quiescent emitter voltage of approximately 11.5 volts, so that the quiescent base to emitter voltage is approximately 0.7 volt. Thus, when the instantaneous signal level during the positive half cycle exceeds about 0.7 volt, the transistor cuts off, clipping the positive portion at the collector. Q9 is also a common base limiter stage and is driven by Q8 through C40. Fixed bias is provided by resistors R37-R49. Signal tuning is provided by L15. L13 and L14 provide isolation and C38-C42 are bypass capacitors. Q9 operation is identical to that of Q8.

(3) Emitter follower Q10 is driven by common base amplifier Q9 .through coupling capacitor C45 and attenuating resistor R45. The transistor is fixed biased by R43, R44, R46 and R47. The

collector is bypassed by C47, and decoupled by L16, L17, and C46.

(4) The final stage in the amplifier-limiter chain is discriminator driver Q11, which is operated in the common base configuration. The drive signal is applied at the junction of R51 and R52, via C49. The base is dc biased at +2.1 volts by voltage divider R48 and R49 and bypassed by C48. the quiescent emitter voltage is around + 1.4 volt, giving a base to emitter voltage of 0.7 volt.

(5) A metering circuit is also provided at the output of limiter stage Q9. This is a diode detector, consisting of CR9, C43, C44, R41 and R42. R41, a variable resistor provides output level adjustment. The dc output of J3 permits observing the response, and is used, for example, when tuning variable inductors L12 and L15.

e. Discriminator Driver. The discriminator driver is comprised of transformer T1, diode detectors CR10 and CR11, diode equalizing resistors R76 and R77, load resistors R53 and R54, coupling capacitor C51, tuning capacitors C52 and C53, temperature compensating capacitor C68, bypass capacitor C54, and decoupling network L18 and C50. the discriminator operates on the phase shift principle. The output is a square wave in which the differential level represents the frequency difference between the reference signal from the modulator and the signal from the reference crystal oscillator..

(1) Both the primary and secondary of T1 are tuned to 79 MHz. Connector J4 (TP4 DISCR) is used for observing the response during alignment. Tuning is accomplished by means of variable capacitors C52 and C53. Q11 output is connected to the primary at terminal 3 (via parasitic suppresser resistor R50), and to the secondary center tap (terminal 5) through dc blocking capacitor C51. At resonance (input signal at 70 MHz), the voltages across the two halves of the secondary are in quadrature with the voltage across the primary and in opposition to each other. When the input signal frequency is higher or lower than the resonant frequency, the phase angle between one half of the secondary and the primary will be greater than 90 degrees. The phase angle between the other half secondary and the primary will be less than 90 degrees, and as in the resonat conditions will be 180 degrees out of phase with the other half secondary.

(2) The signal at the anodes of CR10 and CR11 are the vector sums of the primary and associated half secondary voltages. At resonance, they will be of equal amplitude; in all other cases they will be unequal. The circuit is arranged so that CR10 anode voltage exceeds that at CR11 anode when the input frequency is below resonance, resulting in a positive signal appearing at R55. Each diode conducts when its anode is positive with respect to its cathode. Thus CR10, conducts on one half cycle, while CR11 conducts during the next half cycle. Consequently, the output from the discriminator is the difference between the two. At resonance, the levels are equal and the output is zero. Above resonance the signal at CR11 is higher and therefore a negative signal is produced. Actually, because of the phase difference between the two voltages, the output is a pulsating wave with a repetition rate at the input frequency. This wave is averaged by RC network (R55, C56) to produce an essentially dc level.

f. Ac Amplifier. The discriminator square wave output is amplified in an ac amplifier chain consisting of transistor stages Q12, Q13, Q14, and Q15. Negative feedback is employed for stabilization. The input appears at Q12 base via R57 and C57. Q12, in turn, drives Q13, the Q12 emitter being tied directly to Q13 base. To prevent positive feedback, Q12 collector is isolated by R61 and bypassed by a large capacitor (C58). Q13 is developed at its collector. The output (across R59) is dc coupled to Q14 base. Bypass capacitor C60 removes high frequency components from Q14. The input to Q14 goes to ground through R63. Since this resistor is also connected to the base circuit of Q12 through R58, it provides a dc bias at Q12. A large bypass capacitor (C62) prevents positive feedback to Q12. Q14 collector output across R62 is in turn, dc coupled to the base of emitter follower Q15. Resistor R65 in Q15 emitter circuit is also in the emitter circuit of Q13, and provide negative feedback to Q13. The output appears at Q15 emitter across negative feedback to Q13. The output appears at Q15 emitter across R64 and R65, and is coupled to the phase detector through C65 and R66. L20 and C59 provide power supply decoupling.

g. Phase Detector. The output from stage Q15 is an ac square wave, whose peak amplitude represents the frequency difference between the sampled modulator frequency and the reference crystal oscillator frequency. However, the signal does not identify whether the

modulator frequency is high or low. This information is provided by the phase detector. The phase detector is comprised of transformer T2, detector diodes CR12 and CR13, and associated components. (1) The Q15 output is applied to the primary of T2, where high frequency components are bypassed by capacitor C64. This signal is also applied to J5 (TP3 AMPL) for monitoring. The drive to the secondary center tap is supplied by the Q4, Q5 multivibrator through emitter follower Q6, coupling capacitor C31 and R36. Q6 is driven through R74 from the square wave used to trigger the diode gate which controls the modulator frequency sample input. This signal also appears at J2 (TP1 SYNC) and is used as an oscilloscope sync for waveforms taken at J3, J4, and J5. The positive portion of the signal from Q6 is synchronized with the half cycle from Q15 and corresponds to the modulator frequency error signal.

(2) During the positive half cycle of the gating pulse, diodes CR12 and CR13, conduct. The ground return for this current path is located in the differential amplifier in the modulator module. When the modulator error signal is positive during this period a current flows through resistor R70 from top to bottom. Conversely, when the modulator error signal is negative, the current flows from bottom to top of R70. When the gating signal goes negative, both diodes are back biased and only a small current flows through R70. Thus the phase detector output is a positive or negative square wave above or below the zero axis. The square wave is converted to a dc signal by RC networks in the modulator differential amplifier. Diodes CR14 and CR15 comprise a limiter, which limits the voltage amplitude at the input to CRI2 and CR13. Variable resistor R78 and capacitor C69 form a phase detector balance and are used to set the ac ground point. Resistors R68 and R69 are diode load resistors. The circuit is arranged so that the FREQ CONT lead at P1-8 is positive with respect to the FRRQ CONT RETURN lead at P1-2 when the modulator frequency is high. The FREQ CONT signal is also applied to the meter selector switch through metering resistors R71 and R72 as Center Freq Metering and Center Freq Metering Return.

(3) The supply voltage (+15 volts) is supplied from an external source to P1-3. Industries L4, L19, L21, and L22, and capacitors C63, C66, and C67 provide power supply isolation. The +15 volts is applied to J6 (TP5) through R67 for monitoring.

1-50. Modulator 1A8 Circuit Theory

(fig. 8-20)

Modulator 1A8 is comprised of modulator circuits and frequency control circuits. The modulator circuits produce a 150 MHz subcarrier which is frequency modulated by the baseband input signal (combined pcm and order wire signal). The frequency control circuits produce a 70-MHz signal (sample of modulator frequency) which is applied to electronic frequency control 1A7 where it is compared with a precise, locally generated, 70-MHz signal. A dc signal, proportional to the modulator frequency error, is generated in electronic frequency control 1A7 and applied to the modulator circuits for center frequency correction (para 1-49).

a. Modulator Circuits. The modulator circuits consist of a baseband amplifier, differential amplifier, 150 MHz vco, and amplifier-limiter stages.

(1) The baseband input at J1 is applied to operational amplifier Al through coupling capacitor C23 from the parallel terminating resistors R1 and R2. Variable resistor R2, is a front panel control which is used to adjust the baseband level into the vco, thereby setting the system deviation. Resistors R4 and R6 establish bias and C3 provides bypass. Resistors R5, RS, R29, and capacitors C5 and C6 are compensation elements which set the gain and shape the amplifier response. The supply voltage to this stage is bypassed by C8. The output at pin 7 of A1 is applied from load resistor R67 to the tank circuit of the 150 MHz vco, through coupling capacitor C7. Emitter follower A2D, also connected to the input at J1 through coupling capacitor C1, samples the baseband input. Resistors R3 and R9 set the bias for emitter follower A2D. The output (TRAFFIC MONITOR) of A2D is routed from load resistor R7 through coupling capacitor C4 to alarm monitor 1A5, and to the meter selector switch on the transmitter meter panel. With the meter selector switch in the TRAFFIC position, the meter indicates the presence of a baseband signal at the modulator input.

NOTE

Amplifiers A1 and A2 are integrated circuits. Al is type ,A702 and A2 is type CA3018. These circuits are illustrated in figure 8-18(1).

(2) Differential amplifier A2A and A2B is driven by the low level dc correction signal from electronic frequency control 1A7. Resistors R10,

R11, R12, and R13 provide bias for the base circuits and R16, R17, and R18 set the emitter voltages. CD through C13 are bypass capacitors. The correction signal is applied between the bases of A2A and A2B through isolating resistors R20 and R21. With no driving signal present, both transistors will conduct. Since they are identically biased, their collector currents will be essentially equal. Therefore the output of A2A (junction of R14 and R15) will be positive with respect to the collector output of A2B. This results in a reverse bias being impressed (through isolating resistor R77 and RF choke L3, L4) across varactor diodes CR1 and CR2 in the 150 MHz vco. When the correction signal at A2A goes positive with respect to A2B, A2A will conduct more and A2B will conduct less. With increased current through collector resistor R14, the output voltage of A2B will decrease. Similarly, the output (collector) voltage of A2A will increase because of the reduced voltage drop across R19. Thus, the voltage difference between these outputs decreases resulting in a decrease in the bias voltage applied to the varactor diodes in the 150 MHz vco. It will also be seen that when A2B input signal is positive with respect to A2A, the bias applied to the vco will increase. EFC DISABLE switch S1 is connected across the error signal input from electronic frequency control 1A7. With this switch closed, the error signal is disabled, and A2A and A2B conduct under internal bias conditions. This facility is used while adjusting the 150 MHz vco center frequency.

(3) The 150 MHz vco consists of transistor Q1, bias resistors R22, R23, R24, R26, coupling capacitors C16, C18, bypass capacitors C14, C17, C19, C20 and tank circuit L2, C15, CR1, CR2, R73. CR1 and CR2 are varactor diodes, which are always operated reverse biased. They exhibit an inverse square law capacitance-reverse bias characteristic, that is, the capacitance varies approximately as the inverse of the square root of the reverse bias voltage. By varying the bias voltage, or baseband input signal, the resonant frequency of the tank is made to vary. With only the bias voltage from the differential amplifier applied, the tank resonant frequency will determine the oscillator frequency. If the bias is increased, the diode capacitance will decrease, causing the tank to resonate at a higher frequency. Similarly, a decrease in bias will cause a decrease in the resonant frequency. Since this bias voltage represents the center frequency error, as detected in electronic frequency control 1A7, the vco center frequency follows the frequency of the reference oscillator in electronic frequency control 1A7. The vco center frequency is initially set during alignment by means of variable capacitor C15. If now a baseband signal is applied at the junction of CR1 and CR2, the oscillator frequency will be made to vary about the center frequency; thereby producing a frequency modulated 150-MHz output. Since electronic frequency control 1A7 senses the average vco frequency, it only corrects for center frequency drift and has no effect on the frequency modulation of the carrier. The vco output across load resistor R25 is applied to emitter follower Q2 which prevents loading of the 150 MHz vco stage. The collector of this stage is bypassed by C21 and its output is developed across R27. The output of Q2 is applied through coupling capacitor C22 and resistor R28 to the base of amplifier limiter stage Q3.

(4) Amplifier limiter Q3 amplifies the input signal. The operating point of Q3 is set by biasing resistors R31, R32, and R34 and load resistor R33. The emitter is bypassed by capacitor C26 and FL1 provides power supply isolation. A diode limiter (CR3, CR4, and C24) is connected to the Q3 collector output. Its purpose is to prevent amplitude variations (amplitude modulation) from appearing at the modulator output. CR3 and CR4 are silicone diodes. The' limiting action is achieved by utilizing a semiconductor junction characteristic, known as junction barrier potential. Essentially this means that, with forward voltage applied to the diode, forward conduction cannot start until the junction barrier potential is exceeded. In silicon junctions this potential is approximately 0.65 volt. During the positive half cycle of the signal, CR3 is forward biased while CR4 is reversed biased. When the instantaneous signal level reaches approximately 0.65 volt, CR3 conducts bypassing higher levels through bypass capacitor C24 to ground. During the negative half cycle, the bias conditions of CR3 and CR4 are reversed. At an instantaneous signal level of - 0.65 volt, CR4 conducts, bypassing higher amplitude (more negative) voltages to ground. Thus, the output of amplifier limiter stage Q3 is a frequency modulated sine wave, but clipped at a peak amplitude of -0.65 volt. The output of Q3 is coupled through capacitor C25 to amplifier Q4, which in turn is coupled via capacitor C27 to amplifier Q8. Q4 and Q8 are conventional, dc biased voltage amplifiers. Biasing is by means of resistors R35, R36, R37, and R54, R55 and R56. C29 and C48 are emitter bypass capacitors. At each amplifier output (Q4 and Q8) is a low pass matching section consisting of L23, C28 and L16, C47.

The low pass matching sections suppress the harmonics generated by the clipping action in the limiter. Q4 is decoupled from the 28V supply by L22, R72, FL2, and L5. L17, FL6, and L15 provide isolation for Q8. Capacitor C49 couples the output of Q8 to power amplifier Q9, which operates class C. The operating point is set by bias resistors R69 and R70. Resistor R69 is variable and permits bias adjustment. L18, R71, and FL8 block signal currents from the bias circuit. The Q9 collector output is tuned by L19 and C51 and coupled by C52 to a low pass filter (L20 and C53). The filter suppresses harmonics produced in the amplifier. This stage is decoupled from the 28V supply by FL7, C50, C54, and L21. The filter output (frequency modulated 150 MHz signal) is applied to frequency mixer 1A9 via connector P1 (150 MHz OUTPUT) and attenuator/matching network (R63, R64, R65) and to the transmitter's meter selector switch via a metering circuit and pin P3-9 (output level metering). The metering circuit consists of coupling capacitor C60, load resistors (R59 and R61), diode detector CR10, and metering resistors R62 and R66. Resistor R66 is variable and is used to adjust the meter deflection. Capacitor C61 bypasses ripple. The 150-MHz output of low pass filter (L20 and C53) is also applied to transformer mixer T3 in the frequency control circuits through an attenuator network (R60, R68, and R74).

b. Frequency Control Circuits. The frequency control circuits consist of a 110-MHz crystal controlled oscillator, a frequency doubler, a mixer, and two 70-MHz amplifier stages.

(1) The 110-MHz crystal oscillator consists of transistor Q5, crystal Y1, tank circuit L6, C31, C32, and C33, bias resistors R40, R41, and R42, load resistors R76, bypass capacitor C30, coupling capacitor C34, and isolating network FL3, L9, C37. The crystal operates at series resonance in the fifth overtone. When voltage is applied, the starting transient causes oscillations to start. The crystal signal at Q5 emitter is amplified and appears at the collector of Q5. The tank circuit follows the oscillation, and feeds a regenerative signal. For this condition, the crystal frequency the oscillator signal builds up, until the transistor gain is reduced to unity, at which point a stable level is sustained. Variable capacitor C33 provides a means of varying the frequency by a small incremental value. To illustrate, assume the tank is tuned to a frequency above that of the crystal. This will cause the tank to appear slightly capacitive to the collector signal. As a result, the signal fed back to the crystal leads the crystal oscillating signal. For this condition, the crystal frequency will pull to a higher frequency, in an attempt to restore a zero phase condition. This will result in a reduced phase difference between the collector signal and the tank, and consequently a smaller lead angle in the crystal feedback signal. As a result, the crystal will assume a frequency of oscillation above its normal frequency at which the phase is essentially zero. The crystal frequency shift is very small compared to that of the tank, because the crystal Q is very high and the Q of the tank is relatively low.

(2) The 110-MHz crystal oscillator signal is applied to the primary of T2 in the frequency doubler. This circuit is, in effect, a full wave rectifier, in which CR5 and CR6 alternately pass a half cycle of the input signal. The fundamental of this composite output is twice the input frequency. The wave also contains significant higher order harmonics, which are blocked by the output tuned circuit made up of C35, L8, and the inductance contributed by T3. The 220-MHz output of the frequency doubler is applied to the mixer circuit.

(3) The 220-MHz doubler output is connected to the primary of transformer T3 in the mixer, while the sampled 150 MHz from the modulator is applied to the center tap of T3 secondary. The voltage appearing across the transformer secondary is therefore the 220 MHz oscillator frequency superimposed on the 150-MHz modulator frequency. When terminal 3 of T3 is positive with respect to terminal 5, both diodes, CR7 and CR8 conduct, and the composite signal appears at the top of C38. With the reverse polarity, both diodes are reverse biased and no signal flows. As a result, only the portion of the composite signal above the zero axis appears at the C38, L10 junction. The envelope of this clipped wave is the 70-MHz difference frequency. C38, C39 and L10 form a low pass filter which extracts the 70-MHz envelope.

(4) The 70-MHz output from the mixer is applied to 70-MHz amplifier Q6 via coupling capacitor C40. This stage contains bias resistors R44, R45, R47; collector load resistor R46; and emitter bypass capacitor C42. Isolation is provided by FL4, L11, and L12. The stage is coupled to the second amplifier stage Q7 via coupling capacitor C41. The second stage is similar to the first. Dc bias is provided by R48, R49, R50, and R51. However, in the emitter circuit only R51 is RF bypassed by C43. Unbypassed R50 provides

negative feedback, for stabilization. The collector output is taken off at tap 2 of transformer T4. FL5 and L13 decouple the stage from the 15 volt supply. This signal is applied to cable W2 through coupling capacitor C44. Cable W2 is connected to P2 (FREQ CONTROL INTERCONN connector) which supplies the 70-MHz reference signal to electronic frequency control 1A7. A metering circuit is also connected to the output of Q7, at the load side of C44. The metering circuit produces a dc signal proportional to the 70-MHz level, which is fed to the meter selector switch on the transmitter meter panel. Diode detector circuit (CR9 and R52) operates in an identical manner to the 150-MHz oscillator output metering circuit previously described. L14 and C46 filter ripple at the output. Variable resistor R53 is used to adjust the output level.

1-51. Frequency Mixer 1A9 Circuit Theory

(fig. 1-28)

a. The frequency mixer is used to mix the RF signal from the RF frequency multiplier chain with the nominal 150-MHz fm modulated signal to produce the transmit carrier frequency. The mixer consists of crystal mixer 1A9A1 and 4.4- to 5.0-GHz circulator 1A9HY1.

b. Mixer 1A9A1 uses a single varactor diode CR1 to provide frequency conversion (due to the nonlinear capacitance-voltage relationship of the varactor diode). The 150-MHz fm signal is applied to jack J1 and is coupled to the mixer cavity through tuned circuit L1, and C4, C6. This circuit is tuned to the 150-MHz IF frequency and is used to tune out the varactor capacity at the IF frequency. Isolation of RF from the IF circuits is accomplished by a reentrant quarter wave choke (L-C). Two tuned stubs C4 and C5 suppress the fundamental L.O. frequency. The resulting side-bands are reflected out of the diode cavity Z1 and enter 4.4- to 5.0-GHz circulator 1A9HY1 at port No. 2 (J2).

c. The coaxial circulator has a bandpass from 4.4- to 5.0-GHz with a maximum insertion loss of 0.6 db (port 2 to port 3). This is a four-port coaxial circulator with a resistive termination at port 4. The reflected sidebands enter the circulator at port No. 2 (J2) and leave at port No. 3 (J3). A tunable bandpass filter is connected at port No. 3 and is tuned to the desired sideband which is passed by the filter. The unwanted side- band is rejected at port No. 3 of the circulator to port No. 4 where it is absorbed in the dummy load.

d. A diode type amplitude detector is incorporated in the circulator for monitoring the local oscillator chain pass band shape. The dc monitor output is taken from connector J4.

1-52. Frequency Multiplier Group 1A1O Circuit Theory

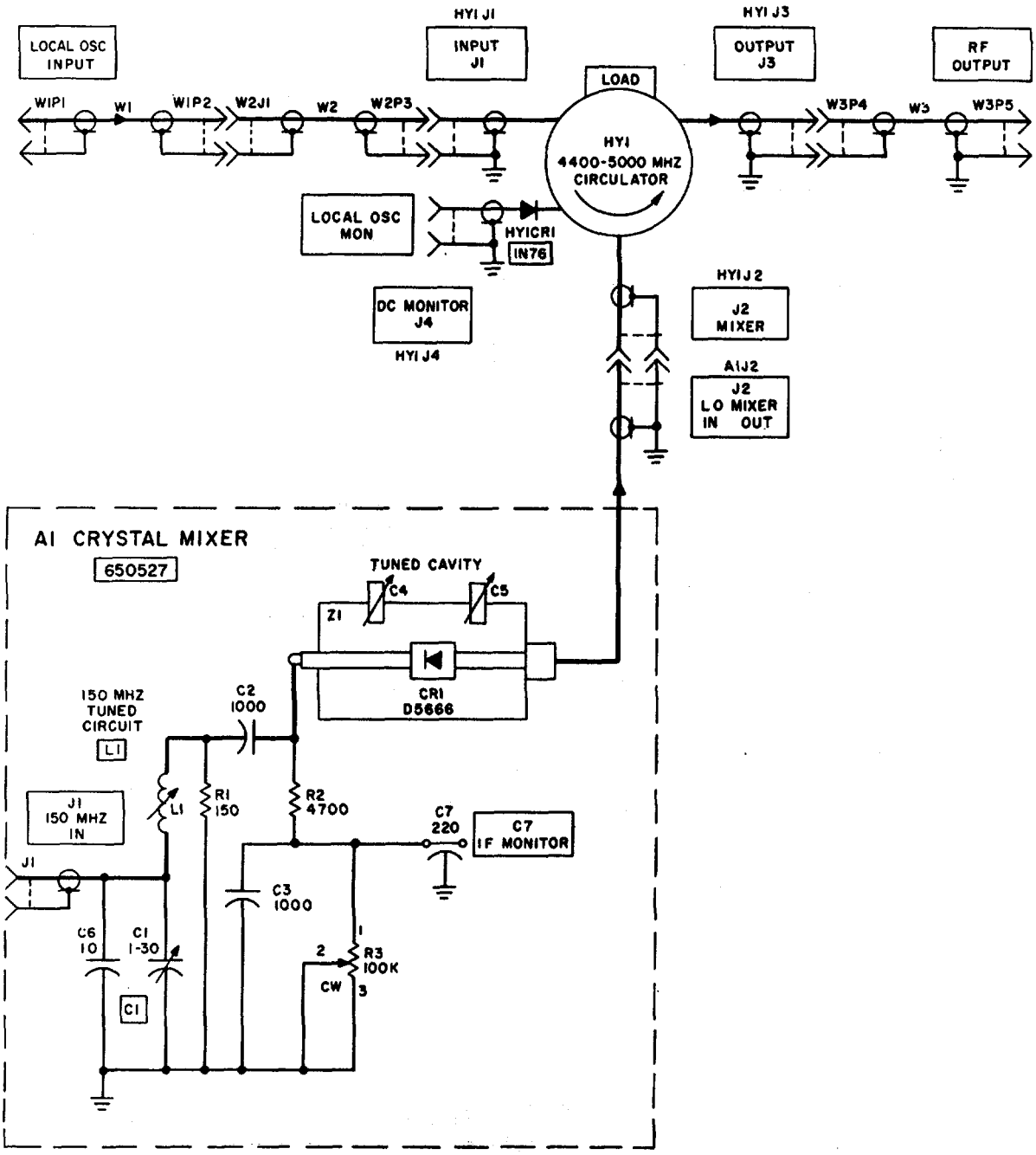
(fig. 1-29)

a. Frequency multiplier group lA10 multiplies the 1137.5- to 1212.5-MHz local oscillator frequency by four. The 4.55- to 4.85-GHz output frequency is at a level of 1.7 watt (minimum) and is applied to frequency mixer 1A9. The frequency multiplier group consists of 2d frequency multiplier lAlOA1 (times 2), 2275- to 2425-MHz circulator 1A1OHY1, and 3d frequency multiplier 1A1OA2 (times 2).

b. The input signal to 2d frequency multiplier lAlOA1 is applied to the low pass filter consisting of C1, L1 and C2. Variable capacitor C1 provides impedance matching at the input. Series variable capacitor C3 provides impedance matching to the varactor diode impedance (typically 1-10 ohms). The varactor diode is a step-recovery type. The step-recovery diode stores a charge as it conducts in the forward direction; when the applied volt- age is reversed the diode will conduct for a brief period in the reverse direction until the stored charge, is removed-conduction then ceases abruptly. The abrupt step in current through the diode produces a waveform that is rich in harmonic power. The 2d harmonic of the incoming frequency is selected by tuned coaxial cavities Z1A and Z2A. These cavities are resonant lines, tuning is provided by a plunger; input and output coupling is provided by adjustable probes.

c. The 2275- to 2425-MHz circulator (1A10HY1) isolates the 2d frequency multiplier from the 3d frequency multiplier. The input (J1 INPUT) and output (J2 OUTPUT) impedance's are 50 ohms resistive. The monitor output (J3 DC MONITOR) provides a sample of the 2d frequency multiplier's output signal to the meter selector switch on the transmitter meter panel. The insertion loss for the circulator is 0.3 db.

d. The 3d frequency multiplier (1A10A2) functions in a similar manner to the 2d stage frequency multiplier. However, since the frequencies are higher the input signal is coupled to the varactor diode via a tuned cavity and the second harmonic output is selected by a single coaxial cavity.



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS CAPACITANCES ARE IN PICOFARADS INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 1A9.
3. ☐ INDICATES MARKING ON EQUIPMENT.

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Figure 1-28. Frequency mixer 1A9, schematic diagram.

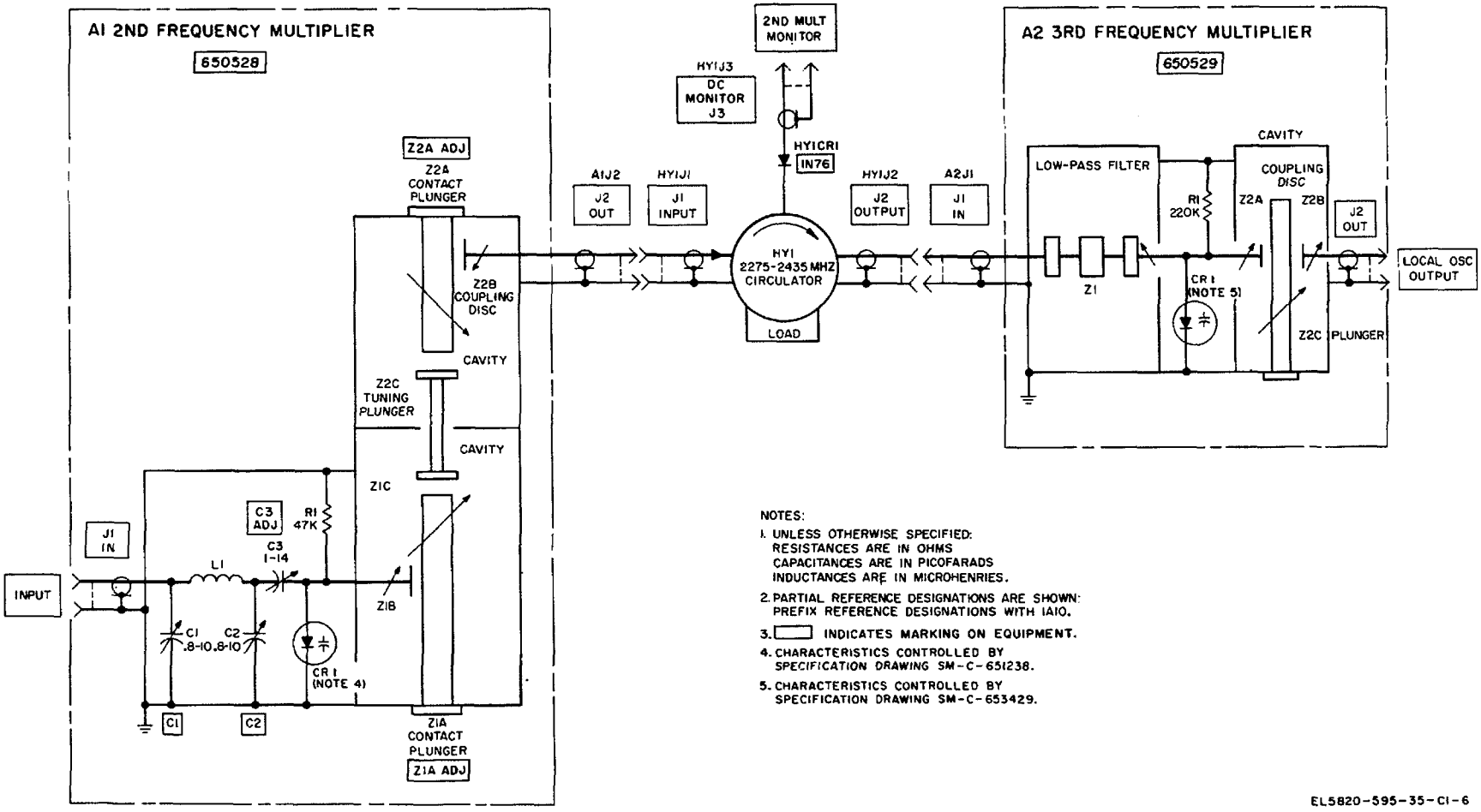


Figure 1-29. Frequency multiplier group 1A10, schematic diagram.

The input and output of the coaxial cavity is provided by adjustable probes.

1-53. Amplifier-Frequency Multiplier 1A11 Circuit Theory

(fig. 8-21)

Amplifier-frequency multiplier 1A11 amplifies and frequency multiplies (times 4) the 284.375- to 303.125-MHz output of frequency synthesizer 1A14. The output signal (1137.5 to 1212.5 MHz) is applied to bandpass filter 1FL5 in the transmitters local oscillator chain. The dc voltage supply for amplifier frequency multiplier 1All is applied through a waveguide switch/relay interlock circuit. The interlock circuit is arranged so that the supply voltage to amplifier-frequency multiplier 1All is interrupted when the waveguide switch (GFE) is in transit (between position). Amplifier-frequency multiplier 1All consists of a low level amplifier, a high level amplifier and a qadurupler stage. The transistors used in the amplifier stages operate in the common emitter configuration. They exhibit low input (base) resistance in series with a small inductance and a relatively high output (collector) resistance in shunt with a low capacitive reactance. In operating these transistors in cascade, the coupling circuitry must transform the output impedance of the driving stage to the input impedance of the driven stage.

a. Low Level Amplifier. The low level amplifier is comprised of transistor stages Q1 and Q2. The low level 283.375- to 303.125-MHz signal is applied to J1. This signal is fed to the base of class A amplifier Q1, via a matching section consisting of L26, C2, C3, C49; and R23. The matching section transforms the 50-ohm source impedance to the low input impedance of the transistor. The emitter is bypassed by C4, C5 & C54. Dc bias is controlled by CR6, R2, R3, R4 & R21 and the overall gain of Q1 is controlled by R22. Adjustable resistor R21 permits varying the base bias and R22 permits varying the collector output. Amplifier Q1 collector is coupled to the base of class C driver amplifier Q2 through a matching section, consisting of L3, CC, C7 and C8. L4 is an RF choke and C47 is dc blocking capacitor. The matching circuit transforms the collector impedance of Q1 to the low input impedance of Q2. The low level amplifier delivers 2 watts (nominal) output power to the high level amplifier.

b. High Level Amplifier. The high level amplifier is comprised of transistor stages Q3, Q4, and Q5. The output of low level amplifier stage Q2 is coupled to class C driver amplifier Q3 in a manner similar to that described for the low level amplifier, except that a 4 db attenuator (R6, R7 and R8) is incorporated in the coupling network. This attenuator limits the drive level into Q3, and also provides isolation between the low level and high level amplifiers. Q3 is coupled to power stages Q4 and Q5 via interstage matching circuitry similar to that previously described. It also contains a power divider consisting of quarter wave sections W2 and W3, and load resistors R11, and R12. In addition to dividing the Q3 output this circuit provides 50 ohms to all ports and isolates the output ports to Q4 and Q5 by greater than 20 db. Capacitors C13, C14 and C15 bypass low frequency components in the Q3 output. Power Stages Q4 and Q5 also operate class C. Their ouputs are fed through coupling networks to a hybrid consisting of quarter wave sections W4 and W5, and resistors R15 and R16. The hybrid combines the transistor outputs and provides isolation between the Q4 and Q5 outputs. As in the Q3 stage, capacitors C21, C22, C25, C28, C29, and C30 bypass low frequencies. The amplifier output of 283.375 to 303.125 MHz at 18 watts (nominal) is fed to the quadrupler stage via cable W6.

c. 1st Frequency Multiplier (Quadrupler). The quadrupler consists of two varactor frequency doubler stages (CR4 and CR5). Resistor R20 at the input is a stabilizing resistor which also provides a dc return for CR3. The input circuit consisting of C34, C35, C36 and L21 is tuned to the input frequency. It also provides impedance transformation between the 50-ohm input and the low varactor diode impedance. Resistor R18 biases diode CR4, which acts as a nonlinear element, thereby generating the harmonics required for frequency multiplication. Two matching networks transform impedance to and from 50 ohms to match the diodes. They are tuned to the second harmonic of the input frequency and are located between diodes CR4 and CR5. The first network consists of C37, C38, C39 and tL23; the second comprises C40, C41, L23 and L24A. Diode CR5, which is biased by R19, performs a function identical to that of CR4. A bandpass filter (C42, C43, and L24B) at the output is tuned to the fourth harmonic of the input frequency. The 1137.5- to 1212.5-MHz quadrupler output is applied to 1137 to 1213 MHz bandpass filter 1FL5 via OUTPUT connector J7.

1-54. Digital Data Modem 1A12
Circuit Theory

Digital data modem 1A12 contains the plug-in modules (printed wiring boards) and chassis mounted components which provide the signal interface between the radio set and the cable equipment. Also, the circuits in the digital data modem complete a dc current path between the cable input terminal and the cable output terminal. The following paragraphs describe the chassis mounted components and the de current path. Electrical operation of discrete place parts for the plug-in modules is provided in paragraphs 1-55 through 1-66. The complete functional description of the plug-in modules is provided in paragraphs 1-11 through 1-21. Refer to paragraph 1-8d for the meaning of the signal mnemonics used in the circuit theory descriptions.

a. Chassis Mounted Components. The chassis mounted component connections are shown on the digital data modem interconnecting diagram (fig. 8-22). The chassis mounted components provide signal interface between the modules, selection and indication of operating modes, filtering of signals, and power distribution.

(1) Capacitors 1A12A15A1TB2C15 through C23 and capacitor 1A12A15A1TB2C33 filter noise from the alarm monitor signal lines. Capacitors 1A12A15A1TB2C26, C29 and C31 filter the order wire signals. The order wire return lines are connected to chassis ground in the digital data modem via capacitors 1A12A15A1TB2C27, C28, C30 and C32. The same arrangement is provided for the receiver agc signal lines by capacitors 1A12A15A1TB2C24 and C25.

(2) TRAFFIC SELECT switch 1A12A15A1S2 connects the logic one level (+5 vdc) to either the 12-channel select line 1M12C or to the 24-channel select line OM12C. The logic zero is provided by the chassis ground connection through pins 3 and 4 of the selector switch.

(3) The power distribution bus on 1A12A15TB3 connects the power supply voltages to the various modules in the digital data modem. Capacitors 1A12A15A2TB1C5, C7, C9, C11, and C13 provide RF filtering of the power lines; capacitors 1A12A15A2TB1C6, C8, C10, C12, and C14 provide filtering of low frequency transients. All the ground lines from each plug-in module terminate at the common ground bus on terminal board 1A12A15TB3. This bus is connected to chassis ground via a 1/4-inch braid and a lug connected to the top rear of the case. Additional filtering of the power lines is provided at the input to. 4,608 MHz voltage controlled oscillator modules 1A12A1 and 1A12A14. Resistors 1A12A15A2R13 and 1A12A15AlR14 provide a decoupled test point for monitoring the modulation input voltages (RVC01 and CVC01). The signal ground for modules 1A12A1 and 1A12A14 is pin 3; the case ground connection is provided at pin 7.

(4) Indicator lamps 1A12A15A2DS1 through DS4 illuminate in response to the jumper plugs that are inserted onto printed wiring boards 1A12A2 and 1A12A13. The +5 volt power supply potential is connected to one side of the selected cable length indicator lamp by the jumper plug inserted into cable digital regenerator board 1A12A2. The +5-volt power supply return is connected to the other side of the selected cable length indicator lamp by the jumper plug inserted into radio digital processor 1A12A13. The selected cable length indicator lamp will light provided that the same cable simulation networks are connected at each board.

b. Dc Current Path. The dc current path through the digital data modem is shown in figure 8-23. The input from the cable is a combined signal consisting of the pcm signal, the order wire signal (when present) and the dc cable current. The combined signal is brought into the radio set through the FROM CABLE connector J1 and enters pin 1 of cable digital regenerator 1A12A2.

(1) The dc cable current is blocked by capacitor 1A12A2C1 and follows the branch through coils 1A12A2L1, 1A12A2L2: and 1A12A2L3. These coils offer a high impedance to the relatively high frequency of the pcm signal; consequently, the pcm signal passes through capacitor 1A12A2C1 to the pcm peaking circuits in the cable digital regenerator. The order wire signal is of relatively low frequency, therefore, it passes through coils 1A12A2L1, 1A12A2L2, and 1A12A2L3.

(2) The order wire and dc cable current flow is through the primary winding of transformer 1A12A15A1T1. The order wire signal appears across the secondary windings of this transformer and is coupled as the cable extracted orderwire signal (CCEXGW) to AF amplifier 1A12A5. Potentiometer 1A12A15A1R1 allows adjustment of this signal level. The low pass filter consisting of 1A12A15A1L1, C2 and C3 blocks the order wire and allows only the dc cable current to pass.

(3) A CABLE LOOP TEST switch (1A12A15A1S1) is incorporated in the digital

data modem. Placing this switch, located on the front panel, in the TEST position enables the digital data modem to substitute the cable loopback pcm test signal (OCLPCM) for the normal pcm signal originating from the radio. When the CABLE LOOP TEST switch is in NORMAL position, relay K1 is energized; when the switch is in TEST position the relay is deenergized. The position of the switch determines the mode of operation of the cable-to-radio circuits of cable digital processor 1A12A4 (para 1-13); the radio-to-cable circuits of alarm-monitor 1A12A6 (para 1-15) and radio digital processor 1A12A13. The effect of the switch on the operation of 1A12A13 is explained in paragraph 1-21(3); this information in relation to the relay is summarized below.

-

CABLE LOOP TEST switch position	PCM Traffic	ONΦR	1RPFAIL	Relay	1A12A13 output signal
NORMAL	Normal	Logic one	Logic one	Energized	Radio-to-cable pcm.
TEST	Normal	Logic one	Logic zero	Not Energized	Cable loopback pcm.
NORMAL	Failed	Logic zero	Logic one	Energized	No pcm.
TEST	Failed	Logic one	Logic zero	Not Energized	Cable loopback pcm.

With the relay deenergized, the resistor/capacitor/diode network on terminal board 1A12A12A2TB1 is switched into the direct current path and provides fault localizing information to Multiplexer TD-204/U at the other end of the cable system.

(4) The cable de current is conducted through normally-closed contacts 1 and 2 of relay 1A12A15A2TB1K1 to the secondary winding of transformer 1A12A15A2T2 where the cable transmit order wire signal (CCTOW) is inserted. The order wire and cable dc current are then coupled to radio digital processor board lA12A13 where the radio pcm signal is inserted via transformer lA12A13T1. The combined order wire plus dc cable current is coupled toTO CABLE output connector J2 to complete the cable path. Diodes 1A12Al3CR8 through CR15 protect the logic circuits from high voltage surges on the cable. The 1/4-mile cable simulation networks are inserted in the cable path when the distance from the radio set to the first cable multiplexer is less than 1 mile. The networks are selected on the basis of 1/4-mile increments to provide proper impedance to the signal.

1-55. 4608-kHz VCO 1A12Al/1A12A14 Circuit Theory

The voltage-controlled oscillator (vco) modules are sealed units that produce a frequency-stable square wave timing signal at a frequency of 4608 kHz. The frequency can be adjusted by means of a direct current applied to the control input. Additionally, the center frequency can be adjusted by means of a manual control to permit compensating for the frequency effects of aging. The output impedance is 470 ohms.

1-56. Cable Digital Regenerator 1A12A2 Circuit Theory

(fig. 824)

The complete functional description of cable digital regenerator 1A12A2 is provided in paragraph 1-11. Electrical operation of discrete piece parts is provided in a through e below.

a. Cable Simulation Networks. The cable simulation networks consist of three 1/4-mile sections. Selection is provided by plug P2. Resistors R1 through R7, capacitors C2, C3, and inductor L4 form one 1/4-mile network; R8 through R14, C4, C5, and L5 form a second network, and R15 through R21, C6, C7 and L6 form the third network. For example, if the cable input to the moden is 1/4 mile, set the plug connections to 1/4 mile. With this arrangement three simulated 1/4-mile networks are in series with the input 1/4 mile of cable providing a total equal to i mile of physical cable.

b. Amplifiers.

(1) Amplifier Q1 is a grounded emitter volt- age amplifier with a "peaked" response at 2304 kHz, due to tuned network R26, R22, C10 and L8. The signal input to amplifier Q1 is through transformer T1 which provides a voltage gain of two. The +12 volt supply voltage is connected to transistor Q1 through voltage dropping resistor R27 which is bypassed by capacitor C8. Capacitor C9 is a high frequency bypass that provides signal ground for the tuned circuit. Resistors R24 and R25 in the emitter circuit of transistor Q1 provide dc bias. Resistor R25 is bypassed for ac by capacitor C12. Since resistor R24 is not bypassed, it provides a small amount of signal (ac) feedback. Resistor R23 is an impedance match for the

secondary of transformer T1 because the input impedance of Q1 is high. Resistor R33 at the secondary side of transformer T2 has the same function. Cable traffic alarm signal XCPCM is taken from the secondary of T1 and sent to alarm monitor lA12A6. Resistor R46 is an isolating resistor to protect T1 and Q1 in the event of a malfunction in the external circuit.

(2) Amplifier Q2 is a grounded emitter amplifier with a voltage gain of approximately 35. The input signal to this amplifier is direct-coupled from transistor Q1. Resistor R28 is the collector load resistor and resistors R29, R30, and R31 provide dc bias. Resistors R30 and R31 are bypassed for ac by capacitors C11 and C13. Resistor R29 is not bypassed and provides a small amount of signal feedback. Dc feedback from the junction of resistors R30 and R31 to the base of transistor Q2 provides temperature compensation between transistors Q1 and Q2.

(3) Amplifier Q3 is an emitter follower which couples the output signal of transistor Q2 to the primary windings of transformer T2 with minimum loading on transistor Q2. Resistor R32 is the emitter load resistor. The ac signal is coupled to transformer T2 through capacitor C14. Transformer T2 provides a voltage gain of four.

(4) Dual transistor circuit Q5 contains a common emitter amplifier Q5A and a temperature compensating bias network consisting of Q5B, resistor R34 and bypass capacitor C15. This type of biasing results in a linear output which is direct-coupled to the input (pin 2) of slicer A1. Resistor R35 functions as the collector load resistor. Resistor R3C provides dc bias and is bypassed for ac by capacitor C16.

(5) Amplifiers Q7 and Q8 are a pnp-npn common-collector complementary pair designed to eliminate temperature drifting effects. Resistors R37 and R40 are the emitter load resistors. Resistor R38 is a current limiting resistor to protect Q8 against current surges, at turn on time or any time when C17 is discharged. The signal at the base of Q8 is rectified by the base/emitter junction to provide a dc reference in direct proportion to the signal level at the base, and is filtered by C17. Resistor R39 provides a minimum voltage across C17. This reduces the time required for input pulses to fully charge C17. Resistor R40 is variable so that the dc input level to the reference input of Al can be adjusted.

c. Slicer A1. Slicer A1 is an integrated circuit. See figure 8-18 for the circuit diagram. Capacitors C18 and C19 provide supply voltage decoupling. The -6 volts through resistor R41 speeds up transitions from logic one to logic zero.

d. Integrator and Lamp Driver. The integrator (transistor Q9) is an emitter follower. Resistors R42 and R43 and capacitor C20 determined the base emitter bias. Pulses of 1CSPCM charge capacitor C20 and maintain a positive dc voltage as long as signal 1CSPCM is active. The output voltage is coupled through current limiting resistor R44 and keeps transistor Q10 (which acts as a switch) turned on. Lamp DS1 then remains lighted as long as 1CSPCM activity continues. If transistor Q10 turns off, lamp DS1 receives a small current to keep it warm through R45. Since a warm lamp has a higher resistance than a cold lamp, when Q1 turns on the current surge is not as great.

e. Voltage Filtering Components. Voltage filtering components (L9 through L11 and C21 through C25) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-57. Cable Control Comparator 1A12A3, Circuit Theory

(fig. 8-25)

Cable control comparator 1A12A3 contains integrated circuits designated Al through All. These circuits are shown functionally in figure 8-25. Figure 8-25 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The complete functional description of cable control comparator 1A12A3 is provided in paragraph 1-12. Electrical operation of discrete piece parts is provided in a through h below. a. Flip-flops. The J and K inputs of flip-flops A7A and A7B are maintained at logic one by connection to the +5-volt supply voltage through resistors R1 and R15.

b. Positive Pulse Generator. When 1PP is logic zero (ground) diode CR1 is forward biased and the emitter of transistor Q1 is at logic zero (approximately +0.7 volt). Voltage division in resistor R3 and diode CR6 provides the +1.4 volt at the base of QI. Capacitor C4 filters this voltage. Transistor Q1 is reverse biased under this condition. Transistor Q3 has -1.4 volt at the base which is provided by a voltage divider consisting of resistor R9 and diode CR7. The voltage is filtered by capacitor C5. With transistor Q1 off, -12 volts through resistor R4 forward biases Q3.

Current flow from + 12 volts through resistor R5, Q3 and resistor R4 to -12 volts produces voltage drops that make the voltage at the collector of Q3 negative. Diode CR5 clamps this voltage at -0.7 volt. This is the low voltage output of the positive pulse generator. When 1PP is high, diode CR1 is reverse biased. Transistor Q1 is forward biased by the positive voltage through resistor R2 and its emitter is at approximately +2 volts. With Q1 on, current flow from +q12 volts through R2, Q1 and R4 to -12 volts produces voltage drops that make the voltage at the collector of Q1 positive. This voltage is clamped at +0.7 volt by diode CR2. This is the voltage at the emitter of Q3, therefore, Q3 is reverse biased. With Q3 off, current flow from +12 volt through R5, diode CR3 and Zener diode CR4 to ground drops the voltage at the collector of Q3 to +5 volts. This voltage is determined by the clamping action of diode CR3 and Zener diode CR4. Zener diode CR4 is protected against current surges by capacitor C1. Resistor R6 provides additional current flow through Zener diode CR4 to assure that the diode is operating at its specified current rating to assure the specified Zener voltage rating. The + 5-volt output signal is coupled to integrator A8 through diode CR12B and resistor R7.

c. Negative Pulse Generator. When 1NP is logic one (approximately +3.5 volts), diode CR8 is reverse biased, and Q2 is forward biased by +12 volts through R10. Current flow from -12 volts through R11, Q2 and R10 to +12 volts makes the voltage at the collector of Q2 positive which is clamped at -0.7 volt by diode CR11. This is the low voltage output of the negative pulse generator. When 1NP is logic zero (ground), diode CR8 is forward biased, the emitter of transistor Q2 is at +0.7 volt and Q2 is reverse biased. With Q2 off, current flow from -12 volts through resistor R11, diode CR9 and Zener diode CR10 drops the voltage at the collector of Q2 to -5 volts. This voltage is determined by the clamping action of diode CR9 and Zener diode CR10. The functions of resistor R12 and capacitor C6 are the same as for resistor R6 and capacitor C1 (c above). The -5-volt output signal is coupled to differential integrator A8 through diode CR12A and resistor C13.

d. Differential Integrator. The differential integrator is composed of capacitors C2, C3, C7, C8, 09, and resistor R14 and differential amplifier A8. Capacitor C2 is a high frequency bypass. Capacitor C3 provides bandwidth limiting to prevent oscillation. Capacitors C7 and C8 are supply voltage decouplers.

Resistor R14 and capacitor C9 form a long-time constant signal feedback path. The feedback signal maintains the output signal and bridges over intervals when the positive and negative pulse inputs are both absent. Resistor R8 is an isolating resistor to couple the signal to test point E14.

e. Positive/Negative Clamp Detector. Resistors R22 and R25 form a voltage divider which provides +0.75 volt as the reference voltage for the positive clamp detector. Similarly resistors R26 and R27 provide -1v for the negative clamp detector. Resistors R21, R23, and R24 form a voltage divider that couples the signal output of A8 into the clamp detectors. The tap-off point at the center arm of resistor R23 is connected to the inputs of both clamp detectors and is bypassed by capacitor C15.

f. Strobe Clock Generator and 48-Channel Baud Generator. Resistors R16 and R17 connect the supply voltage into pin 3 of strobe clock generator A5. Variable resistor R17 and capacitor C10 set the time constant which determines the time duration of the negative pulse output signal. Capacitor C11 is a supply voltage filter. The functions of capacitors C12 and C13 and resistors R18 and R19 at 48-channel baud generator A1 are similar to the functions of corresponding parts at A5.

g. Lamp Driver. The -6-volt supply voltage through resistor R28 speeds up transitions from high (logic one) to low (logic zero) at the input of A10C. Resistor R29 provides a current to keep lamp DS1 warm when the output of A4A is high. When the output of A4A returns to low, the current surge through A4A is not as great due to the lamp warming current.

h. Voltage Filtering Components. Voltage filtering components (L1 through L4 and C17 through C24) limit the coupling of switching transients and other stray signals to the power supply circuits. The +6-volt supply for A8 is derived internally by dividing the -12-volt supply voltage. This is accomplished by resistor R20 and Zener diode CR13. This voltage is filtered by capacitor C14.

1-58. Cable Digital Processor 1A12A4 Circuit Theory

(fig. 826)

Cable digital processor 1A12A4 contains integrated circuits designated Al through A15. These circuits are shown functionally in figure 8-26. Figure 8-26 also specifies each integrated circuit

type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The complete functional description of cable digital processor 1A12A4 is provided in paragraph 1-13. Electrical operation of discrete piece parts is provided in a through e below.

a. Flip-Flops. The J and K inputs of flip-flops A7A and A7B are maintained at logic one by connection to the +5v supply voltage through resistor R5.

b. Data Level Converter. Resistors R1, R2 and R3 are voltage dividing resistors that also provide impedance matching for the TRPCM output signal. The logic zero output is 0 volt to 0.5 volt at 15.5 ohms impedance. The logic one output is 1.5 volt at 22 ohms impedance.

c. Activity Detectors. Capacitor C2 at activity detector A14 filters the supply voltage. Resistor R4 and capacitor C1 determine the time constant for the reset voltage at pin 13. This determines the on time of the output signal. Capacitor C4 and C3 and resistor R6 perform the same function for Al.

d. Dummy Detector and Strobe Placement Integrator Slicer. Resistor R12 and capacitor C7 form a high frequency filter to reduce noise and transient pulses in the signal. Capacitor C6 limits the bandwidth to prevent oscillation. The supply voltage (+6 volts) at pin 6 is derived by dividing the +12 volts through resistor R14 and Zener diode CR2. Capacitors C15 and C16 are supply voltage filters. When the input to A13 at E29 goes positive, the output at pin 5 goes negative with a steep slope (rate of change). When the input goes negative, the output goes positive but with a lesser slope. When the input signal consists of all logic ones (the condition when there are no mismatches), the output of A13 remains at logic one (high). When the input signals are mixed logic ones and zeros, the net output is logic zero (low) because the amplitude of negative going output changes is greater than the amplitude of positive going output changes. The rate of change of output voltage is determined by the time constant of R13 and C5 and the voltage across R13, or the difference in voltage between E29 and pin 2 of A13. This produces the difference in rate of change of output voltage for logic one and logic zero inputs. The voltage at pin 1 is determined by voltage division of the +12-volt supply through resistors R9 and R10. This voltage is filtered by C14. Resistor R11 matches R13 to keep impedance of both input circuits equal. Resistor R15 isolates the output of A13 from the input of A15. A15 is a differential voltage comparator with zero volts reference input at pin 4. R16 is an isolating resistor and C17 filters the +12-volt supply voltage. When the input signal goes 5 millivolt above the reference voltage, the output goes positive (logic one). When the input signal goes 5 millivolt below the reference voltage, the output goes negative (logic zero). Reset diode CR1 is reverse biased when the output at A12D is logic one, and conducts to discharge C5 when the output at A12D is logic zero.

e. Voltage Filtering Components. Voltage filtering components (L1 through L3 and C8 through C13) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-59. AF Amplifier 1A12A5 Circuit Theory

(fig. 8-27)

The complete functional description of af amplifier 1A12A5 is provided in paragraph 1-14. Electrical operation of discrete piece parts is provided in a through e below.

a. The incoming cable extracted order wire signal CCEXOW is developed across R1, and is amplified by Q1. Dc bias is provided by R1, R2, R4, and R5. The gain of the amplifier is determined by the ratio of R3 to R4 and the low frequency cutoff is, determined by C5, R4 and R5. **Diodes CR5 and CR6 with capacitor C19 limit excessively high ring signals introduced into the from cable signal by the external multiplexer,** The amplified output signal is delivered to the power amplifier Q2, Q3, through resistor R6 and capacitors C6 and C7 which form an audio low pass filter. The filter cutoff frequency is approximately 2 kHz. Transistors Q2 and Q3 are a power amplifier which provide current gain but no voltage gain; the circuit operates essentially as an emitter follower. Resistors R10 and capacitor C9 provide output coupling to the load with R10 setting the output impedance at 100 ohms. When the signal at the base of Q2 goes positive, current through Q2 increases and the emitter voltage rises. Q2 functions essentially as a high impedance emitter follower but the current increase also causes a drop in voltage at the junction of collector load resistors R8 and R9. The signal voltage tapped off at this point increases the forward bias of Q3. Q3 is connected as a common emitter amplifier with R7 as emitter load resistor but it functions as a current switch and provides a much greater increase in current than the increase of current in Q2.

b. The level detector is comprised of C10, CR1, CR2, C11, R11 and R12. Diodes CR1 and CR2

provide voltage doubling of the rectified cable receive order wire signal CCROW. The detected voltage is used for system monitoring.

c. The transmit order wire signal CCOWIN is developed across R13 and R14, and amplified by Q4. The gain of this amplifier is determined by the ratio of R15 to R16. The low frequency cutoff is determined by C12, R16, and R17. Dc bias is determined by R14, R16, and R17. The amplified output signal is coupled to power amplifier Q5 and QC through low pass filter network C14, R18, and C13. This network has a cutoff frequency of approximately 2 kHz. Stages Q5 and Q6 are connected as a power amplifier as described in a above. The output signal is coupled through resistor R22 and capacitor C16 to the load.

d. The level detector network C17, CR3, CR4, C18, R23 and R24 functions the same as the level detector network for the receive amplifier discussed in b above.

e. Voltage filtering components (L1, L2, and C1 through C4) limit the coupling of switching transients and other stray signals to the power supply circuits.

NOTE

Alarm monitor 1A12A6 contains integrated circuits designated Al through A9. These circuits are shown functionally in figure 8-28. Figure 8-28 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set.

1-60. Alarm Monitor 1A12A6 Circuit Theory

(fig. 8-28)

The complete functional description of alarm monitor 1A12A6 is provided in paragraph 1-15. Electrical operation of discrete piece parts is provided in a through e below.

a. Lamp Driver.

(1) The lamp driver circuits conduct 40 ma to operate the 28 vdc lamps with standard logic ,inputs. Each circuit is a simple npn transistor inverter with a series 150 ohms collector current limiting resistor (required to limit the cold lamp surge when turning on the lamp). The lamp driver acts as an inverter. When the input is a standard logic "one," the transistor is saturated and the lamp driver provides maximum current (.040 ma.). When the input is a logic zero, the transistor is cut off and the output is open (equal to lamp supply voltage).

(2) There are two types of lamp driver circuits used in the alarm monitor: the first type consists of a transistor with a base pullup resistor and collector current limiting resistor. The base pullup resistor is needed because the inverters associated with these drivers do not have the capability of supplying enough base current in the logic one state. The drivers mentioned above are (Q2, R3, R4), (Q4, R7, R8), (Q8, R20, R21), (Q10, R26, CR6, R24, CR7, CR8, R25) and (Q11, R27, R28). The lamp driver stage Q10 has more circuit components than the other circuits. Since the inverter that drives Q10 also supplies an internal signal to other logic gates, the network (CR6, R24, CR7, CR8 and R25) supplies the current to assure turn on and turnoff for Q10, depending on the output of inverter A3E.

(3) The second type of lamp driver has a series resistor in the base circuit. The resistor serves to: limit base current into the transistor and lessen the loading on the logic gate that controls the driver. The logic gates associated with these drivers have a transistor-logic output network and thus need no pullup resistors. The drivers of this type are: Q1, R1, R2; Q3, R5, R6; and Q9, R22, R23.

b. Relay Driver. Relay driver Q7, which generates the bypass order wire 1 BPOW signal, has the cathode of CR4 connected to its output, with the anode returned to ground. Diode CR4 is a 27-volt Zener diode which provides protection against normal transient voltages generated by the relay. The components associated with the circuit are: CR2, R16, CR3, R17, C2, Q7, CR4 and R18. The components (R16, R17, CR2 and CR3) are used to convert the logic input signal into a base turn on, turnoff signal. Capacitor C2 prevents the relay from following a transient (false) alarm input. Resistor R18 is a current limiting resistor. When the input signal to Q7 is logic one (high), CR2 is reverse biased. Electron flow from ground through C2, CR3 and R16 to +15 volts charges C2 and turns on Q7. When the input signal changes to logic zero (low), CR2 is forward biased. Electron flow is then from the cathode side of CR2 to the positive voltage and also from negative voltage and through R17 to C2, and from ground through Q7 emitter and base to CR3. This delays the turnoff of C2. With C2 discharged, the negative voltage through R17 has two paths, through CR3 and through C2 to ground. As soon as C2 is discharged Q7 turns off.

C2 continues to charge with negative polarity on the side connected to the base of Q7. When the input goes high, this reverse voltage on C2 must be discharged before it can be recharged with positive polarity. Thus turning on Q7, which occurs after a failure has been corrected, is a slow turn off, which occurs when the failure is detected, is also delayed. This allows Q2 to maintain an on or off condition with interruptions in either state.

c. Integrator Driver. The integrator driver QS, Q6 consists of the following components: R10, R15, CR5, R11, R12, C1, R13, R14. The input network (R10, R11, R12, R15, and C1) is comprised of a level converter and integrator for the driver circuit. The output of the integrator drives the base of Q5 which, in turn, controls transistor Q6. Resistor R14 provides current limiting to transistor Q6. There is no inversion of an input signal and a logic one input will become +28 volts at the output; a logic zero input will become zero volt. The output major alarm summary signal (OMARY) is integrated to prevent a false input from triggering this major alarm output. When the input signal (from A3D) is high, electron flow from -6 volts through R11, CR5 and R15 and R10 produces a positive voltage at the junction of CR5 and R11 because most of the voltage is dropped across R11. C1 charges to this positive voltage and turns on Q5. Resistor R14 is a current limiter. With Q5 on at saturation, Q6 has zero volts at the base and is off. When the input changes to low (ground), the positive charging voltage is removed from C2 and it discharges. When the voltage at the cathode side of CR5 goes negative (as C1 discharges), Q5 is reverse biased and turns off. The positive voltage through R13 then turns on Q6 and the output signal major alarm summary (OMARY) is logic zero.

d. Cable Traffic Detector.

(1) The cable traffic detector consists of four sections: cable traffic amplifier A5, 2304 kHz crystal with slicer bias and dc tracking network Q13A and Q13B, slicer comparator AC, and transistor integrator Q12. The cable traffic input signal XCPCM to the traffic detector is ac coupled to the input of high gain amplifier A5. Amplifier A5 drives crystal Y1 which resonates at 2304 kHz (nominal pcm cable component); the two transistors, Q13A and Q13B, provide bias (Q13B) and dc tracking with temperature (Q13A). The components used in the bias network are: R37, C13, Q13B, R39, C14 and R38. The parts used to attain dc temperature tracking are: R33, C9, Q13A, R34, R35, R36 and C10.

(2) The output of the dc temperature tracking circuit is added to the crystal output. This composite signal is fed to the noninverting input pin 2 of the comparator A6 while the Q13B bias is applied to the inverting input pin 3. The output of the comparator will be low for small amounts of cable traffic, due to the 10 percent offset supplied by R34 and R36 (in the dc tracking network). When the traffic is normal ,the comparator output will be switching and turn on the transistor integrator (R32, Q12 and C8). The integrator will allow small gaps in the pcm cable signal to go undetected by the alarm gating circuits.

(3) Cable traffic amplifier A5 is a high gain video amplifier. The supply voltage at pin 9 is derived by dividing the +12 volts supply through resistor R29 and Zener diode CR9. This voltage is filtered by capacitor C6. It is also the collector voltage for Q13. Capacitor C17 determines the low frequency cutoff and C18 determines the high frequency cutoff. Capacitor C5 and resistor R30 form a high pass filter. Dc blocking capacitor C7 isolates the high pass filter so that dc voltage at pin 1 of A5 is not changed. The cable traffic signal from cable digital regenerator 1A12A2 is amplified by A5 and the output signal is connected to crystal filter Y1 and to Q13A and Q13B. Crystal filter Y1 offers a low impedance to a very narrow frequency band centered at 2304 kHz and a high impedance outside the passband. Thus the signal at the output side of Y1 is the pcm signal minus most of the noise and transients. Q13A and Q13B are emitter followers which pass the pcm signal to the inputs of A6 but in the process they generate an average dc bias from the signal. Q13A has a high frequency cutoff at the input comprised of R33 and C9. Q13B has a similar input circuit, R37 and C13, but it has a higher cutoff frequency and thus Q13B passes more high frequencies than Q13A. The emitter load resistance of Q13A is R34 and R36. Since the output is coupled to A6 through isolating resistors R35 and R31, only 90 percent of the output signal of Q13A is used. The emitter load resistance of Q13B is R39. Capacitor C10 and C14 become charged to the average dc level of the input signal and determine the dc level about which the pcm signal varies. The dc level of the signal at E13 is lower than the dc signal at E14 because the output taken from Q13A is only 90 percent at the available signal. The pcm signal at E13 is greater than at E14 because of the signal coupled through Y1. This is the condition that exists when the pcm (cable traffic) signal is

present. The voltage at E13 then alternately exceeds and falls below the voltage at E14 and the output (pin 7) of A6 switches from high to low at the pcm rate. This signal coupled through isolating resistor R32 alternately turns Q12 on and off. When Q12 is off, C8 charges to a plus voltage and when Q12 is on, it discharges through Q12. Thus, when the pcm (cable traffic) signal is present, Q12 switches on and off and prevents C8 from holding a charge (logic one). The source of the charging voltage for C8 is in A3E. When the pcm signal is absent, the signal inputs to A6 at E13 and E14 are determined by the noise and transients, but no switching takes place. C8 can then charge up until its output is logic one (high).

e. Voltage Filtering Components. Voltage filtering components (L1 through L3, C3, C4, C11, C12, and C15, C16) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-61. Amplifier-Detector 1A12A7 Circuit Theory

(fig. 829)

The complete functional description of amplifier-detector 1A12A7 is provided in paragraph 1-16. Electrical operation of discrete piece parts is provided in a through i below.

a. Agc Slicer and Buffer Amplifier. The age slicer is a dual transistor (Q4) emitter follower which reduces the amplitude of the reshaped pcm signal 1RSPCM-1 to approximately the same amplitude as the pcm/order wire signal FRPCM. It operates as a differential amplifier. Q4A conducts only when its base is more positive than the dc bias at the base of Q4B; when this occurs, Q4B is cut off. Thus the signal is sliced or rectified because Q4A conducts only on the positive polarity of the pcm signal. The gain is controlled by the dc level at the base of Q4B, which is derived from the 1RSPCM-1 signal as modified by a feedback signal. This is explained in d, e, and f below. The output signal from emitter load resistor R20 is coupled through a low pass filter, L1 and C8, which eliminates frequencies above 50 kHz. The signal is then amplified in emitter follower buffer amplifier Q5. Resistor R21 and R22 determine the dc bias for Q5, and R22 is also the emitter load resistor. The output signal is coupled to the radio simulation network.

b. Radio Simulation Network. The first section of the radio simulation network, C9, R23 and. R24 provides for simulation of the low frequency phase shift characteristics of the radio receiver and for part of the attenuation. The signal is connected to the attenuation network, R25, R26 and R27 through capacitor C11. C11 provides some high frequency attenuation but it provides more low frequency than is desired. To compensate for this, part of the signal (from R24) is coupled through low pass filter, C10 and R30.

c. *Subtractor*. Amplifier A1 is a type MC1531G integrated circuit (fig. 8-18) which operates as a unity gain differential amplifier. The input signal at pin 1 is the pcm signal. The input signal at pin 2 (inverting input) is the pcm plus order wire signal. This signal (FRPCM) comes through low pass filter, L2, C23 and R45 which eliminates frequencies above 50 kHz. The two pcm signals are as nearly equal as the circuits can make them. The result is that the output signal is the order wire signal plus some residual pcm because the two pcm signals cancel (or the pcm at input pin 1 is subtracted from the pcm input at pin 2). The output signal (order wire plus residual pcm) is fed back through capacitor C3 and resistor R6 to the primary of transformer T1. It is also connected to the inverting input (pin 2) through resistor R31. Since the signal here is the pcm plus order wire and the two order wire signals are equal, the order wire signal has no effect but the residual pcm signal provides negative feedback. Operating voltages are supplied to pin 1 through voltage divider resistors R28 and R29 and to pin 2 through R33 and Zener diode CR2. Capacitor C14 and C15 filter the supply voltages.

d. Buffer. The reshaped pcm signal (1RSPCM-1) is passed through a low pass filter composed of L7, R2, R3 and C1 with a cutoff frequency of approximately 50 kHz. This passes the low frequency components of the pcm signal which is coupled through buffer amplifier Q1 to pin 3-5 of transformer T1 with no loss in signal. Q1 is an emitter follower; dc bias is determined by R3 and R4 and R4 is also the emitter load resistor. The output signal is coupled through capacitor C2 and isolating resistor R5 to the secondary of transformer T1.

e. Product Detector. The pcm signal inserted at the transformer center tap and the feedback residual pcm from the primary of transformer T1 are out of phase in the secondary; cancellation by an amount equal to the feedback pcm occurs. The resulting signal (reduced pcm plus order wire) is rectified and filtered by C4, C5, R7, R8 and R9 and applied as positive dc pulses to the basis of

Q2A and Q2B. Each half of the secondary of transformer T1 works into a half wave rectifier. Since their input signals are out of phase, the output pulses at Q2A and Q2B alternate.

f. Differential Amplifier. The differential amplifier operates as a class B push-pull amplifier. Resistors R10, R11 and R13 set the dc bias level for Q2 stages. The voltage is filtered by C6. Resistors R12, R14, R16, R17 and R18 set the dc bias level for Q3. Resistors R12, R14, R15 and R19 are collector load resistors. When the signal at the base of Q2B goes more positive, the collector voltage goes negative and drives the base of Q3B negative. Conduction through Q3B increases and changes capacitor C7. When the signal at the base of Q2A goes more positive, the collector voltage goes negative and drives the base of Q3A negative. The emitter of Q3A and Q3B are then driven negative to reduce the charging current into capacitor C7.

g. AF Amplifier. The order wire plus residual pcm output signal from subtractor Al is developed across level adjustment potentiometer R34 and coupled to the base of audio amplifier Q6. Transistor Q6 is a common emitter amplifier; dc bias is determined by R36, R37 and R34. Resistor R37 is bypassed for ac by C16; R36 provides a small amount of degenerative feedback. Resistor R35 is the collector load resistor. The stage provides a gain of approximately 100. The output signal is coupled through low pass filter C17, C18 and R38. Transistors Q7 and Q8 are a power amplifier which provide current gain but no voltage gain; the circuit operates essentially as an emitter follower. When the signal at the base of Q7 goes positive, current flow through emitter load resistor R39 increases and the emitter voltage increases. Increased current flow in Q7 causes the voltage drop across the collector load, R41 and R40 to increase. This negative-going voltage, topped off at the junction of R41 and R40, increases current flow in Q8. This is the main source of signal current flow. The output signal is coupled through R42 and C20. R42 provides an output impedance of 100 ohms.

h. Order Wire Signal Detector. The order wire signal detector, comprised of C21, CR3, CR4, C22, R43 and R44, is a voltage doubler-rectifier circuit used to monitor the peak amplitude of the radio recovered order wire RROW.

i. Voltage Filtering Components. Voltage filtering components (L3 through L6 and C24 through C31) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-62. Radio Digital Regenerator 1A12A8 Circuit Theory

(fig. 8-30)

Radio digital regenerator 1A12A8 contains integrated circuits designated A1 through A7. These circuits are shown functionally in figure 830. Figure 8-30 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The complete functional description of radio digital regenerator 1A12A8 is provided in paragraph 1-17. Electrical operation of discrete piece parts is provided in a through i below.

a. Differential Amplifier. The differential amplifier consists of a matched pair of npn transistors, Q1A and QIB, connected in a common-emitter configuration with resistors R2, R3 and R4 in the emitter circuit. Resistor R1 is the 51-ohm termination for the pcm/orderwire input signal FRPCM. The collector of Q1B will have about a 4-volt (peak-peak) swing for a 1-volt peak-peak) input signal at base of QIA. The base of QIB is at ground, so the collector voltage never goes negative. R5 and CR1 are the collector load impedance.

b. Linear Buffer 1. Linear buffer 1 consists of a pair of complementary transistors (npn and pnp) connected as emitter followers; Q2 conducts on the positive half cycle of the input signal and Q3 conducts on the negative half. When Q2 conducts, capacitor C1 charges through diode CR2 and capacitor C2. When Q3 conducts, capacitor C1 discharges through diode CR3 and capacitor C4. Thus Q2, and Q3 are low impedance sources which rapidly charge and discharge capacitor C1 and couple the FRPCM signal into the peak detectors. To understand the purpose of CR1, assume that it is removed and that the bases of Q2 and Q3 are connected together. The average dc voltage at the emitters of Q2 and Q3 is the + 6volt dc, so the ac signal at the bases is swinging positive and negative above and below this value. When it is +5.3 volts or less (0.7 volt negative with respect to +6 volts), Q3 is on; when it is +6.7 volts or higher (0.7 volt positive with respect to +6 volts), Q2 is on. This condition leaves a spread of 1.4 volt of the input signal over which both Q2 and Q3 are off. Insertion of diode CR1 reduces this spread to 0.7 volt, so Q3 conducts when the input signal is +5.65 volts or less and Q2 conducts when the input signal is +6.35 volts or higher.

c. Peak Detectors. The FRPCM signal is rectified by diodes CR2 and CR3. The rectified voltage is developed across load resistors R6 and R7

and filtered by C2 and C4. C3 provides additional high frequency filtering. Under operation, C2 has an average positive voltage (E15) and C3 has an average negative voltage (E16). These voltages permit current to flow through C1 only on peaks of the signal voltage applied to Q2 and Q3. The algebraic sum of the voltages at E15 and E16 is present at E18. This voltage (E18) is always the dc average of the positive and negative peaks of the FRPCM signal.

d. Linear Buffers 2 and 3. Linear buffer 2 consists of npn and pnp emitter followers in series. R8 and R10 determine dc bias and R10 is the emitter load resistor. The pnp and npn transistors provide temperature compensation and cancellation of offsets, that is, the base to emitter voltage drop (positive to negative) of Q4A is canceled by an opposite voltage change at the base/emitter junction of Q5A. Thus the voltage at the base of Q4A always equals the voltage at the emitter of Q5A. The circuit of linear buffer 3 is the same. The output signals are coupled through isolating resistors R13 and R14.

e. Voltage Comparator. Voltage comparator A4 receives the FRPCM signal at pin 3 (E19) and the dc reference signal developed from the FRPCM signal at pin 4 (E20). When the input signal at pin 3 goes more than 0.5 millivolt positive with respect to the signal at pin 4, the output goes to logic one. When the input signal at pin 3 goes more than 0.5 millivolt negative with respect to the signal at pin 4, the output goes to logic zero. Capacitor C5 is a supply voltage filter.

f. Transition Detectors. Transition detector Q6 and Q7 is the same in circuit and operation as transition detector Q8 and Q9. The pcm signal output of A3B is coupled through C7 and R16 to the base of Q6. When the pcm signal is positive (logic one), Q6 conducts and charges C6. When the pcm signal is negative, C7 discharges through CR4 and Q6 is cut off. The positive voltage developed by C6 at the emitter of Q6 is coupled to the base of Q7 through R19 and turns on Q7. The output of Q7 is then logic zero. When there is no pcm signal, Q6 does not turn on and C6 discharges through R18 and through a parallel path, R19 and Q7. Transistor Q7 then turns off and the output signal is logic one. Resistor R20 is the collector load resistor of Q7. Resistor R17 is a current limiting resistor that prevents excessive current if Q6 turns on when C6 is discharged. Resistors R15 and R16 determine the turn on level for Q6.

g. Loss of Traffic Detector. The FRPCM signal is connected to the inverting input of Q7 (pin 4) through isolating resistor R22. The reference input is derived from + 12 volt supply voltage and voltage divider resistor R23 and R24. The operation is the same as that described for voltage comparator A4. Logic one and logic zero are generated at the output in step with logic zeros and logic ones at the input.

h. Squelch Audio and Inhibit Clock Detectors. Resistors R38 and R40 divide the +12 volt-supply voltage to provide the reference voltage for A5. This voltage is filtered by C16. The signal input voltage receiver agc switched RAGC-SW is coupled through isolating resistor R37 and filtered by C13. Capacitor C15 is a supply voltage filter. The operation of A5 is the same as that described for voltage comparator A4. When the agc bias voltage is greater than the reference voltage, the output is logic zero; when it is less than the reference voltage, the output is logic one. Resistor R41 provides inverse feedback from the output to the reference input. The effect of the feedback is to make the reference voltage slightly more positive when the output is logic one and slightly more negative when the output is logic zero. In either case, it slightly increases the difference between signal and reference voltages and prevents noise and hash from causing false transitions at the output. Resistor R42 supplies current from the negative supply voltage to speed up transitions to the logic zero level. A6 is the same in circuit and operation as A5, except that the agc bias is connected to the inverting input and the reference voltage to the noninverting input. So the output of A6 is logic one when the agc bias is greater than the reference voltage and logic zero when it is less than the reference voltage.

i. Voltage Filtering Components. Voltage filtering components (L1 through L4 and C17 through C24) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-63. Radio Control Comparator 1A12A9 Circuit Theory

(fig. 8-31)

Radio control comparator 1A12A9 contains integrated circuits designated A1 through A13. These circuits are shown functionally in figure 8-31. Figure 8-31 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The circuits of 1A12A9 that are comprised of

discrete components are similar to corresponding circuits of cable control comparator 1A12A3 and the explanation of circuit operation is the same (para 1-57). The complete functional description of radio control comparator 1A12A9 is provided in paragraph 1-18.

1-64. Control Processor 1A12A10 and 1A12A12 Circuit Theory

(fig. 8-32)

The control processor contains integrated circuits designated A1 through A18. These circuits are shown functionally in figure 8-32. Figure 8-32 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The complete functional description of control processor 1A12A10 and 1A12A12 is provided in paragraph 1-19. Electrical operation of discrete piece parts is provided in a through d below.

a. Activity Detector. Resistor R1 and capacitor C3 determine the time constant of the reset voltage at pin 13 of activity detector A15. Capacitor C4 filters the supply voltage.

b. Lamp DS1. Resistor R2 provides a current to keep lamp DS1 warm when the output of A17B is high. When the output of A4A returns to low, the current surge through A4A is not as great due to lamp warming current.

c. Resistors. Resistors R3, R4 and R5 connect a fixed logic one (+5 volts) to the associated logic circuits.

d. Voltage Filtering Components. Voltage filtering components (L1, C1, C2) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-65. Pulse Decoder 1A12A11 Circuit Theory

(fig. 8-33)

The pulse decoder has two framing control circuits (PCM-1 and PCM-2) which are identical; therefore only the PCM-1 framing control circuit is described. Pulse decoder 1A12A11 contains integrated circuits designated A1 through A11. These circuits are shown functionally in figure 8-33. Figure 8-33 also specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. This complete functional description of pulse decoder 1A12A11 is provided in paragraph 1-20. Electrical operation of discrete piece parts is provided in a through d below. a. Input Clamp Circuit. Resistor R1 and diodes CR1 and CR2 comprise a clamp circuit to limit the logic one voltage of the match/mismatch PCM-1 signal OMM (1) applied to terminal 3 from control processor 1A12A10. When signal OMM (1) is a logic one, the input voltage is typically 3 volts or more and diode CR1 is forward biased; Zener diode CR2 is reverse biased (but conducting). The voltage at E4 is higher than -6 volts by the sum of the voltage drops of CR1 and CR2 and equals +2.2 volts. When signal OMM (1) is a zero, the input voltage is nearly ground and the diodes are nonconducting. The voltage drop across resistor R1 is very small compared to the voltage drop across resistors R4 and R5 and, therefore, E4 is also nearly at ground. Resistor R20 and diodes CR8 and CR9 comprise a similar clamp circuit, except that the input (+5 volts) is fixed. This circuit provides a voltage at E16 equal to the voltage at E4 when OMM (1) is logic one. Thus, the voltage at the top of potentiometers R2 and R3 is the logic one level. The setting of each of these potentiometers determines the threshold probability of the associated integrator circuit.

b. Sense and Search Integrator Circuits.

(1) The PCM-1 framing control sense integrator consists of resistors R4 and R6, capacitors C1 and C3, and operational amplifier A1. Search integrator A3 is a similar circuit and functions in the same manner. Capacitor C1 limits the high frequency response of the amplifier, reducing sensitivity to noise and eliminating any tendency to oscillate. The high gain of the amplifier and the feedback (capacitor C3 from output pin 5 of A1 to inverting input pin 2 of A1) make the voltage difference between the inverting and noninverting inputs of the amplifier (pins 2 and 1, respectively) nearly zero and, therefore, the current at these inputs nearly zero. Thus, the voltage applied to pin 2 of A1 is nearly the same as the bias voltage at test point J2 produced by potentiometer R2, and the currents through R4 and C3 are nearly the same (assuming that diode CR5 is non-conducting). As a result, the current charging or discharging capacitor C3 is proportional to the difference between the voltages at E4 and J2. Since the voltage at pin 2 of Al is nearly constant, the rate of change of the voltage acr6ss capacitor C3 is also the rate of change of the output voltage at test point J1, and this rate is also proportional to the input voltage difference. (2) The integrator input voltage difference

may be positive or negative. When the voltage at E4 is higher than the voltage at J2, the output voltage at J1 goes down; for the reverse case, the output voltage goes up. The output voltage has a range of +5 volts maximum and -5 volts minimum.

(3) Sense integrator A1 input circuit includes diode CR5 which couples search mode signal 1SM (1) back to the input of the integrator. When 1SM (1) is logic zero (low), diode CR5 is reverse biased, and there is no current flow. When 1SM (1) is logic one (high), current flows back to the integrator input (pin 2), and because of the low source impedance of sense search mode flip-flop A6A and the low-impedance path through diode CR5, the output of the integrator (pin 5) is rapidly reset to a low voltage (typically -4 or -5 volts) regardless of the OMM (1) input signal.

(4) Search integrator A3 has a clamp circuit to limit the output voltage below +4 volts. The clamp circuit is comprised of transistor Q1, diodes CR3 and CR4, and resistor R9. The clamp limit voltage is determined by the bias voltage obtained from voltage divider R8, R10, R14. When the output voltage of amplifier A3 goes slightly above the bias voltage (nominally -4 volts), transistor Q1 is turned on and collector current flows through diode CR3 back to the inverting input of the amplifier. This current cancels the current through resistor R5 and prevents the output voltage of the amplifier from going higher. When the output of the amplifier is lower than the clamp limit voltage, the base-emitter junction of transistor Q1 is reverse biased. Diode CR4 shunts this junction and limits the reverse voltage, thus preventing a breakdown of the junction. Resistor R9 limits the current drawn from the voltage divider. Excessive current could alter the bias voltage at test point J5. Diode CR3 is reverse biased when the amplifier output is low, thus preventing conduction through the collector-base junction of Q1.

c. Search and Sense Decision Circuits.

(1) The search mode, sense mode, and the sync loss decision circuits (A2, A4, and A5, respectively) operate as voltage comparators that produce a logic one voltage output when the voltage at the noninverting input (pin 3) exceeds the voltage at the inverting input (pin 4) and, conversely, a zero output voltage when the noninverting input is less than the inverting input. One of the inputs is a variable voltage from the associated integrator circuit, the other input is a fixed bias voltage developed by a voltage divider circuit.

(2) Voltage divider R15 and R16 provides +4 volts bias for A2. Voltage divider R17 and R18 provides -4 volts bias for A4. Voltage divider R8, R10 and R14 provides a bias voltage for A5 of 02 to +4 volts, depending on the setting of R10.

d. Common PCM-1 and PCM-2 Circuits. The PCM-2 framing control circuits operate in the same way as described above for the PCM-1 framing control circuit. Both circuits, in addition, share dc power circuits. Both circuits obtain dc power. through LC decoupling filters. Each filter circuit, (L1, C9, C10), (L2, C11, C12), (L3, C13, C14) and (L4, C16, C17) limits the coupling of switching transients and other stray signal components from the circuits on the board to the power distribution system. At high frequencies, the capacitance of C9 is considerably less than nominal, but capacitor C10, being a different type, maintains a higher capacitance and thus, adequate filtering. Two voltage regulator circuits (transistors Q3 and Q4, and associated components) generates +6 VR (volts, regulated) and -6VR from the + 12- and -12-volt supplies. The -6-volt regulator circuit is an emitter follower with R41 for emitter load resistor and a fixed dc bias as the base provided by Zener diode CR13. CR13 regulates at -6.2 volts and has the required operating current supplied through R40. The regulated output voltage is -6.2 volts plus the base emitter voltage drop of Q3 or -5.5 volts. The emitter voltage follows the voltage at the base, that is, remains constant regardless of changes in load current (within operating limits). The output voltage is filtered by C15. Resistors R38 and R39 provide a voltage drop of about 6 volts, so a transistor with lower power and voltage ratings can be used. The +6-volt regulator is the same as the -6-volt circuit except for polarity reversals.

1-66. Radio Digital Processor 1A12A13 Circuit Theory

(fig. 8-34)

Radio digital processor 1A12A13 contains integrated circuits designated A1 through A7. These circuits are shown functionally in figure 8-34. Figure 8-34 specifies each integrated circuit type. Figure 8-18 provides a circuit diagram for each type of integrated circuit used in the radio set. The complete functional description of radio digital processor 1A12A13 is provided in paragraph 1-21. Electrical operation of discrete piece parts is provided in a through d below.

a. Cable Output Amplifier. Transistor Q1 has a fixed dc bias, determined by voltage divider L1, L2 and CR1, at the emitter. The primary of transformer T1 is the collector load impedance. Resistor R3 is a current-limiter to protect Q1; R4 and CR2 clamp out inductive current when the signal changes from logic one to logic zero. When the output signal at A4C is logic one, transistor Q1 turns on and provides a current pulse through the primary of T1. This pulse is inductively coupled into both sections of the secondary. Positive-going transition of the input signal is speeded up by the +5-volt source through resistor R39 and capacitor C1. Capacitor C changes with negative polarity on the side connected to the base of Q1. On negative-going input signal transitions, the negative change on C1. speeds up switching time of Q1.

b. Output Circuit. The cable dc current path is shown in figure 8-23 which illustrates the complete current path through the digital data modem. The diodes CR8 through CR15 provide protection against breakdown voltages in excess of 1300 volts. The cable current is set for a nominal 38 milliamperes. The cable simulation networks are 1/4-mile line sections which can be patched on-line for proper termination of the cable. These are selected to provide a 1-mile cable section for the remote cable repeater. Capacitor C4 provides signal ground for pcm.

c. Traffic Detector. The traffic detector circuit consists of transistor stages Q1 through Q4. The traffic signal from cable output amplifier Q1 is applied to traffic detector amplifier Q2, Q3 via transformer T1. The output of Z3 controls transistor switch Q4 in the traffic detector circuit and also transistor switch Q5 in the indicator circuit. When a traffic signal is detected Q4 and Q5 are turned on. With Q4 and Q5 turned on, the ONOR output is low and DS1 is off (normal condition). When a traffic signal is not detected, Q4 and Q5 are turned off. With Q4 and Q5 turned off, the ONOR output is high and DS1 is on (alarm condition). Positive pulses at the secondary (pins 5 and 6) of transformer T1 are applied through current-limiting resistor R26 to the base of Q2. Q2 turns on and develops a negative-going voltage pulse across collector load impedance R27, R28 and R29. Part of this signal is connected to the base of Q3, which then develops a positive-going voltage pulse across collector impedance R34. The positive-going output signal of Q3 is coupled through current-limiting resistors R32 and R33 into the bases of Q4 and Q5. Q4 and Q5 turn on and signals ONOR and 1RPFAIL are logic zero. Lamp DS1 is lighted. Diodes CR3, CR4, CR6 and CR7 are connected from base to emitter at their respective transistors. They protect the base/emitter junction against excessive reverse voltage. Resistors R31 and R35 speed up turn off time of Q4 and Q5. Resistor R36 keeps lamp DS1 warm during off time. CR5 and R30 limit current .(to external relay 1A12A15A2TB1K1) for logic one (Q4 off).

d. Voltage Filtering Components. Voltage filtering components (L1, L5, L6, L7 and C2 and C3 and C14, 15, 16, and 17) limit the coupling of switching transients and other stray signals to the power supply circuits.

1-67. Order Wire Assembly 1A13 Circuit Theory

Order wire assembly 1A13 provides party line communication on a single order wire channel by amplifying and interconnecting signals between the local handset, remote telephone, the radio equipment, and through order wire (multiplex equipment). The internal order wire connections are such that sidetone is only provided for the local handset. The order wire assembly also provides central alarm monitoring circuits, an input to a speaker monitor, in-band, signalling at 1.6 kHz, a 1.1-kHz test tone, and order wire fault detection circuits. Five boards (1A13A1 through 1A13A5) plug into the order wire chassis assembly (1A13A7) to provide the functions mentioned above. The interconnections between the five boards and chassis mounted components of the order wire assembly are shown in figure 8-35.. The following paragraphs describe each board in reference designation order (1A13A1, 1A13A2,-etc). The descriptions are at the circuit level and are based on the schematic diagram of the associated board.

1-68. Board No. 1 1A13A1 Circuit Theory

(fig. 8-36)

Board No. 1 provides the order wire fault detection circuits. The circuits consist of a 4.02-kHz oscillator circuit, monitor circuit, MODULE TEST selector switch, and TEST TONE switch. The MODULE TEST selector switch (1A13A1S1) connects a test input signal (4.02 kHz or ground) to the orderwire circuit under test. The output of the order wire circuit under test is connected

through the MODULE TEST selector switch to the monitor circuit. The TEST TONE switch (1A13A1S3) is used to control the 1.1-kHz oscillator circuit on board No. 2 (1A13A2). When depressed, the TEST TONE switch turns on the 1.1-kHz,oscillator and the 1.1-kHz test tone signal is routed to the order wire circuits. The 4.02-kHz oscillator and monitor circuits on board No. 1 are described in a and b below.

a. 4.02-kHz Oscillator Circuit. The 4.02-kHz oscillator circuit generates a test signal for amplifier circuits on board No. 3 through 5 (1A13A3 through 1A13A5), peak limiter circuits on board No. 5 (1A13A5), and the speaker amplifier circuit on board No. 2 (1A13A2). The 4.02-kHz oscillator circuit is comprised of transistor circuit Q1, tuned circuit Z1, and output amplifier A1. Output amplifier A1 is a buffer stage which isolates the oscillator output. The 4.02-kHz output of amplifier Al is applied to S1C-1 and S1E-1 of the MODULE TEST selector switch and to transformer 1A13A1T1. The transformer inverts the 4.02-kHz output for application to S1D-1 of the MODULE TEST selector switch. The two 4.02-kHz signals are applied to S1C-1 and S1D-1 because two inputs are required to test the amplifier circuits on board No. 3 through 5 and the peak limiter circuits on board No. 5. The 4.02-kHz signal applied to S1E-1 is used to test the 4.02-kHz oscillator and monitoring circuits. With the MODULE TEST elector switch set to position 1, the 4.02- kHz test signal is routed through S1E-1 and S1E-5 to the monitoring circuit (transistor circuit Q2, 1C A2, and switch assembly S2). An analysis of the 4.02-kHz oscillator circuit follows:

(1) Transistor circuit Q1 and tuned circuit Z1 form a modified Colpitts oscillator. Tuned circuit Z1 is a parallel tank circuit with a frequency of 4.02 kHz. When power is initially applied, the tank circuit oscillates and the 4.02- kHz signal is coupled from pin 2 of the tank circuit to the emitter of Q1. The amplified signal developed at the collector of Q1 is applied to the tank circuit and sustains oscillation because the initial loop gain is greater than unity. Resistors R1 and R2 provide the bias at the base of Q1 and resistors R3 and R5 are bias resistors at the emitter of Q1. Potentiometer R4, in the emitter bias circuit provides a means of adjusting the signal level into amplifier Al.

(2) Two 4.02-kHz oscillator output signals are coupled to amplifier Al which provides level control. One 4.02-kHz oscillator output is coupled through capacitor C2 and voltage divider R8, R9 to the inverting input of A1 and the other 4.02- kHz oscillator output is coupled through capacitor C1 and voltage divider R6, R7 to the noninverting input of Al. This configuration (inverting and noninverting inputs) provides minimum distortion. C3 and C4 are stabilizing capacitors. Resistor R10 provides a negative feedback path to stabilize the voltage gain. A zero dc offset voltage is obtained by supplying --∑-volt bias through R11. Capacitor C5 blocks dc from the output circuit. Resistors R12 and R13 are impedance matching resistors in the output circuit. A diagram of amplifier Al (integrated circuit CA3031) is provided in figure 8-18 (1).

b. Monitor Circuit. The monitor circuit determines the status of the order wire circuit under test. If the circuit under test is operating properly, the MODULE TEST indicator (DS1) is extinguished. If the circuit under test is not operating properly, the MODULE TEST indicator lights red. The monitor circuit is comprised of emitter follower Q2, tuned circuit (4.02 kHz) Z2, amplifier A2, and switch assembly S2. The monitor circuit receives 4.02-kHz amplifier outputs via SIB of the MODULE TEST selector switch. The .6-kHz oscillator, 1.1-kHz oscillator, or alternating 1.1/1.6-kHz alarm signals are applied to the monitor circuit through S1A of the MODULE TEST selector switch.

(1) The 4.02 kHz test signal is applied through voltage divider network R16 and R17 through S1B of the MODULE TEST selector switch. Potentiometer R17 is used to adjust the sensitivity of the 4.02-kHz monitor circuit. The 4.02-kHz test signal is coupled to the base of emitter follower Q2 through closed contacts of switch S2 and capacitor C8. Emitter follower Q2 provides a low input impedance to tuned tank circuit Z2. Resistor R19 stabilizes the input impedance at the base of Q2 and resistor R20 establishes the bias at the emitter of A2. Tuned tank circuit Z2 has a very narrow bandwidth and provides a peaked output at 4.02 kHz. The output of the tuned tanked circuit is applied to amplifier A2 through capacitor C9. A diagram of amplifier A2 (integrated circuit CA3035) is provided in figure 8-18 .

(2) Amplifier A2 provides an output across resistor R25 which is applied to pin 6 of switch assembly S2. Switch assembly S2 includes the MODULE TEST indicator lamp and a lamp driver. When the 4.02-kHz test signal is amplified and properly detected, the output at pin 7 of amplifier A2 is approximately 0 volt causing the MODULE TEST indicator lamp to remain extin-

guished. If the 4.02-kHz test signal is not amplified and properly detected, the output of amplifier A2 is approximately +10 volts causing the MODULE TEST indicator lamp to light red. Resistor R18 and diode CR1 provide the voltage necessary to operate MODULE TEST indicator DS1.

(3) The 1.6-kHz oscillator, 1.1-kHz oscillator, or 1.1/1.6-kHz alternating alarm signal is applied to three stage amplifier A2 through S1A, resistors R33 and R21, and capacitor C9. If the test signal applied is of the proper amplitude, amplifier A2 will provide an output that causes the MODULE TEST indicator to remain extinguished. The positive signal output from the first stage of amplifier A2 is coupled through C10 and is detected by diodes CR2 and CR3. Capacitor C11 filters the detected signal. Resistor R22 is a feedback resistor for the first stage and resistors R23 and R24 are input resistors for the second and third stages of amplifier A2. Resistor R25 provides positive bias to operate the MODULE TEST indicator DS1 under zero output conditions. Capacitors C6 and C7 are decoupling capacitors for the +12v and -6v supplies. Resistors R14, R15, and R26 through R32 are voltage dividing resistors to provide proper monitoring levels.

1-69. Board No. 2 1A13A2 Circuit Theory

(fig. 8-37)

Board No. 2 contains the central alarm monitor, the 1.1-kHz test tone oscillator, and the speaker amplifier circuits. The following (a through c below) describe each circuit on board No. 2.

a. Central Alarm Monitor Circuit. The central alarm monitor circuit monitors the alarm input signals from the receiver (RCVR ALM), transmitter (XMTR ALM), power amplifier (PA ALM), and the digital data modem (PCM SUM ALM). If an alarm condition is present at any of the inputs, the central alarm monitor circuit will cause the CNTRL ALARM indicator on the transmitter meter panel to change from green to red and the 1.1/1.6-kHz audible alarm to sound. The alarm inputs are applied to two OR gates. OR gate A controls the 1.1/1.6-kHz audible alarm. OR gate B controls the CNTRL ALARM indicator on the transmitter meter panel.

(1) With ground applied to any of the alarm inputs, OR gate A (diodes CR6-CR9, resistors R18-R21, and capacitors C5-C8) detects an alarm condition and controls the audible alarm circuits. Assume that ground is applied to pin 6 (PCM SUM ALM) causing capacitor C5 to discharge through resistor R18. The negative pulse developed across R18 is coupled through diode CR6 to the cathode of silicon controlled switch Q3 causing Q3 to operate. With 7Q3 operating, a ground return is connected to the emitters of multivibrator transistors Q1 and Q2 permitting the multivibrator to operate. R4 and C2 determine one time constant of the multivibrator and R3 and C1 determine the other time constant. R2 and R5 are collector bias resistors of the multivibrator. When pin 4 of Q3 is connected to +12v through pins E and A and R6, the current to turn on Q3 is from +12v through R1 and R7 to ground, CR1 is used as a bias diode and capacitor C23 is used as a filter. With the multivibrator operating, the 1.1-kHz and 1.6-kHz oscillators are alternately turned on and off. The multivibrator output at the collector of Q2 is applied to the emitter of Q7 (part of 1.1-kHz oscillator circuit) through diode CR10. When Q1 conducts, its collector voltage is low and triggers the 1.1-kHz oscillator into oscillation. When Q1 is not conducting, its collector voltage is high and the 1.1-kHz oscillator cannot oscillate because a high voltage is applied through CR10 to the emitter of Q7. The multivibrator output at the collector of Q2 is applied to the 1.6-kHz oscillator circuit on board No. 5 and alternately turns the oscillator on and off. The alternating 1.1/1.6-kHz oscillator outputs are applied via external circuits: and pin M to emitter followers Q4 and Q5. Resistors R8 through R12 are used to bias emitter followers Q4 and Q5. The output of Q5 is applied to speaker amplifier A2 through resistors R13, R33, and R34. Capacitor C15 couples the signal to amplifier A2. C16 is a high frequency bypass. Stabilization of the amplifier is accomplished with C18 and C19. The output is connected by C20, C21 and R36 to speaker amplifier-monitor. The output of Q4 is applied to the remote signal/alarm through the hybrid transformer mounted on the order wire assembly chassis. The 1.1/1.6-kHz audible alarm signal can be removed by depressing the RESET pushbutton on the transmitter meter panel. This removes the path through Q3 causing Q3 and the multivibrator to turn off.

(2) Speaker amplifier A2 receives additional order wire inputs through pin 8, speaker volume control No. 1 input. The signals are amplified for application to the speaker on the transmitter meter panel. A circuit diagram of amplifier A2 (integrated circuit MC1554G) is provided in figure 8-18).

(3) With ground applied to any of the alarm inputs, OR gate B (diodes CR2-CR5 and resistors R14-R17) detects the summary alarm condition and causes the CNTRL ALARM indicator on the

transmitter meter panel to change from green to red. Assume that ground is applied to pin 6 (PCM SUM ALM) causing diode CR2 to conduct. With CR2 conducting, transistor switch Q6 is turned off. For this condition, the operating voltage for the green lamp CNTRL ALM-NORMAL is removed from pin P, and the ground return for the red lamp CNTRL ALM-ALM is applied to pin N (through CR2)..

b. 1.1-kHz Oscillator Circuit. The 1.1-kHz oscillator circuit generates the 1.1-kHz signal which is used for test tone and part of the audible alarm signal (1.1/1.6 kHz). The oscillator circuit is comprised of transistor circuit Q7, 1-1kHz tuned circuit Z1, and amplifier A1. Transistor circuit Q7 and 1.1-kHz tuned circuit Z1 form a modified Colpitts oscillator. Resistors R22 and R33 are a voltage divider and develop the bias on the base of Q7. R24, R25 and R26 are the Q7 emitter resistors and provide dc bias and ac impedance. Potentiometer R25 controls and ac level into amplifier A1. The oscillating frequency is determined by the 1.1-kHz tuned circuit. The oscillator turn on signal is coupled through diode CR10 from the multivibrator circuit (Q1 and Q2), the MODULE TEST switch on board No. 1, or the TEST TONE switch on board No. 1. When the oscillator is turned on, the 1.1-kHz output of Z1 is fed back to the emitter circuit of Q7. The amplified signal developed at the collector of Q7 sustains oscillation. 1.1-kHz oscillator output signals are applied to operational amplifier A1 via capacitors C9 and C10 and R27 and R24. R28 and R30 are input loading resistors for amplifier A1. R31 forms the feedback path which determines the amplifier gain and R32 is a bias-load resistor. The A1 output is coupled through resistor R35. C13 and C14 are stabilizing capacitors preventing high frequency oscillations. Amplifier A1 is a general purpose operational amplifier which provides minimum distortion and isolates the oscillator from the output circuits. A circuit diagram of amplifier A1 (integrated circuit CA3031) is provided in figure 8-18 (1).

c. Filtering Components. C11, C12, and C17 are filter capacitors for the power supply circuits. C3 and C4 are spike suppression capacitors for high frequency.

1-70. Board No. 3 1A13A3 Circuit Theory

(fig. 8-38)

Board No. 3 contains the pcm alarm circuit and amplifier circuits A1 and A2. Each circuit is described in the following paragraphs.

NOTE

Amplifiers A1 and A2 are integrated circuits (type MC1533G). A circuit diagram is provided for these circuits in figure 8-18 (1).

a. PCM Alarm Circuit. The pcm alarm circuit (relay K1) connects either the recovered order wire signal (pins N and S) or the order wire (PCM Bypass) (pin D) to the order wire circuits. For normal conditions, a ground return is present at pin H causing relay K1 to be energized. With K1 energized, the recovered order wire signal is coupled to the order wire circuits by transformer T1, resistors R9 and R10, and contacts 4 and 6 of relay K1. When a pcm alarm condition occurs, the ground return is removed from pin H, and relay K1 becomes deenergized. R11 is a dropping resistor in the relay coil circuit. With K1 deenergized, the order wire (PCM bypass) signal (pin d) is applied to the order wire circuits via contacts 8 and 6 of relay K1. Since the order wire signal is part of the receiver traffic signal, order wire communication is maintained when a pcm failure occurs.

b. Amplifier A1. Amplifier A1 amplifies order wire signals for application to the through order wire transmit terminals (pins 11 and 12). Order wire signals (recovered order wire, or 4.02-kHz order wire test signal) or the order wire (PCM bypass) signals are applied to the noninverting input (pin 2) of amplifier A1 via capacitor C2. C3 and R4 are stabilization components. Resistor R2 provides symmetrical loading to the noninverting input of A1. Order wire amplifier No. 3 input signals are applied to the inverting input (pin 1) of amplifier A1 via capacitor C1. Amplifier A1 has an input impedance of approximately 1 Meg and an output impedance of approximately 100 ohms. The amplifier gain is approximately 100 and is determined by resistor R1 (10 k) and resistor R3 (1 Meg). Capacitors C4 and C5 provide stabilization. The output (pin 5) is coupled to the through orderwire transmit terminals via capacitor C6, resistor R5, 3 kHz low pass filter FL1, and transformer T1. Filter FL 1 sharply attenuates signals above 3 kHz, consequently, the 4.02-kHz test signal cannot appear at the through order wire transmit terminals. The 4.02-kHz test signal is routed to order wire amplifier No. 3 monitor circuits through pin E. Resistors R6, R7, and R8 provide an impedance match between the filter and transformer T1.

c. Amplifier A2. Amplifier A2 amplifies order wire amplifier No. 2 input application to the order

wire hybrid terminal (pin 8). Order wire amplifier No. 2 inputs (pin 1) are applied to the inverting input (pin 1) of amplifier A2 via capacitor C7 and resistor R12. The noninverting input (pin 2) receives order wire amplifier No. 2 inputs (pin 9) through capacitor C8. Resistors R14 and R12 determine the gain of A2. R13 provides a symmetrical input into the noninverting input. Capacitors C12 and C13 provide stabilization. The output of A2 is applied to filter FL2 via C14 and R16. R17, R18 and R19 provide an output T pad for filter FL2. R20 couples the output signal to the remote signal/alarm circuits.

d. Filtering Components. C9 and C10 an filter components for the power supply circuits.

1-71. Board No. 4 1A13A4 Circuit Theory

(fig. 8-39)

Board No. 4 contains amplifier circuits and the 1.6-kHz monitor circuit. Each circuit is described in the following paragraphs.

NOTE

Amplifier A1 and A2 are type MC1533G integrated circuits and amplifiers A3 and A4 are type CA3035 integrated circuits. A circuit diagram for each of these circuits is provided in figure 8-18(1).

a. Amplifier Circuits. Amplifiers A1 and A2 amplify signals for application to the orderwire amplifier 6 monitor circuit and order wire amplifier 4 monitor circuit. Through order wire receive or 4.02-kHz test signals are applied to the inverting input (pin 1) of amplifier A1 through pins 6 and H, transformer T1, resistors R13 and R7, and capacitor C1. The 4.02-kHz test signal is applied via pin F, resistor R7, and capacitor C1. Order wire amplifier 4 inputs are applied to the noninverting input (pin 2) of amplifier A1 via pin M and capacitor C2. The amplifier provides a gain of approximately 100. Circuit operation and component function is the same as described in paragraph 1-70 for amplifier A1 on board lA13A13. The output (pin 5) of amplifier A1 is coupled through capacitor C8 and resistor R5, appears across potentiometer R6, and is applied through pin 1 to order wire amplifier No. 2. The output of A1 is also applied to the inverting input (pin 1) of amplifier A2 via coupling capacitor C9. Also the 4.02-kHz test signal is applied to the inverting input of A2 via pin E, resistors R6, R8, R9, and capacitor C9. Order wire amplifier e input signals are applied to the noninverting input (across R10) of amplifier A2 via pin N and coupling capacitor C10. Amplifier A2 provides a gain of 100 and operates the same as amplifier 1A13A3A1 (para 1-70). The output of amplifier A2 is coupled through capacitor C14 and 3-kHz low pass filter FL1 to the handset receive terminal (pin L). Filter FL1 sharply attenuates signals above 3 kHz, consequently, the 4.02 kHz test signal is not applied to the handset receive. Resistor R14 matches the output impedance of the amplifier to the filter circuit. Resistors R15-R17 form an impedance matching network in the output of filter FL1. The output of amplifier A2 is also applied to the speaker amplifier volume control No. 2 through resistor R18 and pin 12 and to the 1.6-kHz monitor through resistor R20.

b. 1.6-kFHz Monitor Circuit. The 1.6-kHz monitor circuit detects the order wire amplifier 6 input (1.6-kHz ringing signal). The circuit is comprised of tuned circuit Z1, amplifiers A3 and A4, a level discriminator circuit, and relay K1. When the 1.6-kHz ringing signal is detected relay K1 becomes energized causing the 1.6-kHz ringing signal to be applied to the speaker volume control No. 1 through pin 13. Also, the RING indicator on the meter panel changes from green to amber.

(1) A 1.6-kHz signal at the output of amplifier A2 is passed by means of voltage dividing resistors R20 through R23 through the 1.6-kHz tuned circuit and capacitor C16 to amplifier A3. A3 is comprised of three amplifier stages. Pin 1 is the input and pin 3 is the output of the first stage of A3. The first stage is a frequency reject circuit in that a level will appear at pin 3 only when a 1.6-kHz signal is present. R27 provides negative feedback for gain stabilization. Pin 3 is connected to the input (pin 4) of the second stage through resistor R26 and capacitor C15. The output of the second stage is pin 5. (The third stage of amplifier A3 is not used.) The output of the first and second stages are coupled to the level discriminator circuit (diodes CR1 through CR5 and resistor R28) through capacitor C17 and C18.

(2) The output of the level discriminator circuit is applied to the input (pin 1) of amplifier A4 through filter network R29, R30, and C19. Amplifier A4 is the same type of circuit as amplifier A3, however, the third stage of A4 is, used (input-pin 6, output-pin 7). Resistors R32 and R31 are input resistors for the second and third stages. When no signal or a signal other than 1.6 kHz + 40 Hz is applied to amplifier 3, the amplitude-phase detector circuit causes the output of A4 to be high (+ 12v). For this condition, relay K1 is deenergized. When the ringing signal (1.6 kHz ±

40 Hz) is applied to amplifier A3, the level of discriminator causes the output of A4 to be low (0 volt). For this ,condition, relay K1 is energized causing the RING indicator on the transmitter meter panel to change from green to amber and ringing tone to be applied to the speaker. Diode CR6 protects against transient voltages when relay K1 is deenergized.

(3) Capacitors C3 and C4 are used to decouple the power supply inputs to board No. 4. Resistor R8 provides the proper output level from A2 for monitoring purposes. Resistor R19 couples the 1.6-kHz tone to the speaker volume control No. 1 when relay K1 is energized.

1-72. Board No. 5 l A13A5 Circuit Theory

(fig. 8-40)

Board No. 5 contains the 1.6-kHz oscillator circuit, peak limiter circuits, and amplifier circuits. Each circuit is described in a and b below.

NOTE

Amplifiers A1 through A5 and voltage regulator VR1 on board 1A13A5 are integrated circuits: A1 (type CA3031), A2 and A3 (type CA3001), A4 and A5 (type MC1533G), and VR1 (type MC1560G). A circuit diagram of each circuit is provided in figure 8-18 (1).

a. *1.6-kHz Oscillator Circuit.* The 1.6-kHz oscillator generates a 1.6-kHz signal which is used for ringing and also for part of the 1.6-kHz/1.1-kHz alarm signal. The circuit is comprised of transistor circuit Q1, and 1.6-kHz tuned circuit Z1, and amplifier A1. Transistor circuit Q1 and 1.6-kHz tuned circuit Z1 form a modified Colpitts oscillator circuit. The oscillator control signal is coupled to the emitter of Q1 via diode CR1 and pin C. The oscillator can be turned on by the RING switch on the meter panel, the MODULE: TEST selector switch on board No. 1 (1A13A1) or the central alarm circuits on board No. 2 (1A13A2). The 1.6-kHz oscillator output is applied to amplifier A1 via capacitors C1 and C2. Amplifier A1 is a general purpose operational amplifier which provides minimum distortion and isolates the oscillator from the output circuits. The 1.6-kHz oscillator and amplifier circuit and component function is identical with that of the 4.02-kHz oscillator described in paragraph 1-68*a.*

b. Peak Limiters and Amplifier Circuits. Linear amplifier A2 and A3 are used as peak limiter circuits. The purpose of the peak limiter circuits is to prevent the input signals from exceeding a predetermined level. Peak limiting is accomplished by utilizing the diode characteristic of the linear amplifier. Above a predetermined value the output of the amplifier follows the limiting action of the silicon diode. Voltage regulator VR1 provides a regulated supply voltage for the peak limiter circuits. Handset transmit input test tone 1.1 kHz, or the 4.02-kHz input are applied to peak limiter A (amplifier A2) through capacitor C7 and resistor network R19 and R24. The proper handset level is obtained through voltage divider network R16 and R17. Resistors R14 and R15 provide proper input levels for the 4.02-kHz and 1.1-kHz signals. Resistor R23 minimizes input offset voltage and R25 sets the operating point of amplifier A2 to provide the proper peak limiting. Minimum output offset voltage is obtained with R26. The output of peak limiter A is coupled through capacitor C6 and resistor R27 to potentiometer R28. Order wire hybrid input, ring 1.6 kHz, or the 4.02-kHz input are applied to peak limiter B (amplifier A3) through resistor divider networks R29 through R33. These inputs are coupled to peak limiter B through capacitor C9 and resistors R34 and R37. Operation and component function for peak limiter B is identical to that for peak limiter A above. The + 6 volts required for the peak limiters is established in VR1 by resistors R35 and R36. Resistor R38 is a current limiting resistor and capacitor C10 reduces output noise. The 6 volt output of VR1 is filtered by capacitor C11 and is applied to peak limiters A and B through blocking diode CR2. The output of peak limiter A appears across potentiometer R28 and is coupled to amplifier A5 (pin 1) through capacitor C13. Peal limiter A output is also applied to order wire amplifier No. 2 through pin F. The output of peak limiter B appears across potentiometer R43 and is coupled to amplifier A5 (pin 2) through capacitor C14 and to orderwire amplifier No. 6 through pin 6. Amplifier A5 provides a gain of 100. Operation and component function of amplifier A5 is identical to amplifier 1A13A3A1 (para 1-70*b*). The output of amplifier A5 appears across potentiometer R50 and is coupled to amplifier A4 (pin 1) through capacitor C21 and to order wire amplifier No. 3 through pin 15. Order wire amplifier No. 5 inputs are supplied to amplifier A4 (pin 2) through capacitor C22. Amplifier A4 provides a gain of 100 and is identical to amplifier A5. The output of A4 is applied to the transmitter's order wire circuits via capacitor C26, impedance matching resistor R6, 3-kHz low pass filter FL1, transformer T1, and output pins 13 and 14

Filter FL1 sharply attenuates signals above 3 kHz, consequently, the 4.02-kHz test signal is not applied to the transmitter's order wire circuits. Transistor circuit Q2 is used as a sidetone amplifier and is connected between the transmit and receive elements of the local handset. The handset transmit input is applied to the base of Q2 via pin R and capacitor C8. The output of Q2 (emitter follower configuration) is applied to the handset receive (sidetone) through resistor R22 and pin S. Resistors R20 and R21 provide the proper bias for transistor Q2. Dc power is supplied to the local handset microphone through dropping resistor R18.

1-73. Frequency Synthesizer 1A14/2A21 Circuit Theory

The frequency synthesizer provides an RF output freuqnecy in the range of 284.375 MHz to 303.125 MHz. Seven modules (Al through A7) and a dual power supply (A8) plug into connectors in the main chassis (A10). Power connections and remote indicator connections are made at the rear of the main chassis. The main chassis also contains thumb wheel switches for frequency selection, power and operational indicator lamps, and integrated circuit, and a relay circuit. Figure 8-41 illustrates the chassis mounted components and the module connections. The circuit descriptions for frequency synthesizer 1A14 modules are given in paragraphs 1-74 through 1-81 and are arranged in reference designation sequence (1A14A1, 1A14A2, etc). The descriptions also apply to frequency synthesizer 2A21 used in the receiver, except the reference designations are prefixed with 2A21 instead of lA14 and the word "receiver" is used instead of "transmitter."

a. Thumbwheel Switches. Four thumbwheel switches: Si-I (SI-II dummy), S1-III, S1-IV and S1-V (fig. 8-41A) provide +5 vdc return (ground) connections to the switch gate inputs of the variable frequency divider modules 1A14A4 in accordance with their settings; the contact configurations for each thumbwheel switch setting are indicated below. An X indicates the switch closed position which applied a +5 vdc return (ground) line to the associated switch gated input.

b. Indicator- Lamps. Two power indicator lamps and six operational indicator lamps are provided: the power lamps indicate presence of the +28- volt and +5-volt power from the dual power supply 1A14A8. Operational indicator lamps are provided on plug-in modules 1A14A1 through 1A14A6. A lighted (red) lamp indicates a failure in the associated plug-in module.

c. Integrated Circuit Z1. Integrated circuit Z1 (type 933) provides a diode distribution network for the +5-volt lamp test signal. Pressing TEST pushbutton S2 applies 5 volts dc to this network which, in turn distributes it to the individual operational indicator lamp bias circuits.

S1-I and S1-II (DUMMY)

Con	1000- and 100-MHz Thumbwheel switch settings						
tact	44	45	46	47	48	49	50
B	.....	.....	X	.....	.....	X	X
C	.....	X	.....	.....	X	.....	X

S1-Ill

Con	10-MHz thumbwheel switch settings									
tact	0	1	2	3	4	5	6	7	8	9
A	X	.....	.....	...	...	...	X	X	X	X
B	X	X	.....	...	...	...	...	X	X	X
C	X	X	X	...	...	...	...	...	X	X
D	X	X	X	X	...	...	...	...	...	X
E	X	X	X	X	X					

S1 -IV OR S1-V

Con	1-MHz or 0.1-MHz thumbwheel switch settings									
tact	0	1	2	3	4	5	6	7	8	9
1	.....	X	.....	X	...	X	...	X	...	X
2	....	....	X	X	...	...	X	X		
4	....	....	....	...	X	X	X	X		
8	....	....	....	...	...	...	...	...	X	X

d. Relay Circuit. Relay K1 is controlled by application of power to the crystal oven in standard rf oscillator 1A14A7. Relay K1 is shown in the deenergized position; this position indicates that the crystal oven has reached its operating temperature. When the crystal oven is not at its operating temperature, 28 volts dc is applied to the relay coil from pins 4 and 6 of plug XA7. This energizes the relay KL and provides an open circuit at pins A3, B3, to a remote indicator (SYNTH OVEN indicator on transmitter meter panel).

1-74. RF Oscillator 1A14A1 Circuit Theory

(fig. 8-42)

a. Power (28 volts dc) from the dual power supply 1A14A8 is applied through pins 1 and 5 of connector P1.

The +28 volts dc is applied to terminal E12 on board A3 and to the input of voltage regulator VR1. The voltage VR1 produces +20 volts +1 percent which is applied to the vco (Y1), board A2, and board A4 through RF feed throughs FL1, FL2, and FL3 respectively. The RF feed throughs filter RF currents which might adversely affect the circuit operation.

b. The 283.375- to 303.125-MHz RF output frequency generated by the vco (Y1) is determined by the vco bias voltage produced in the AF phase error detector 1A14A3 and applied through coaxial connector P1-A3 and terminal El. The vco bias voltage varies between 4.5 and 16.0 volts dc. The RF output is applied to board A4 through terminal E18 and to board A2 through terminal E3 and resistor R8.

c. The 284.375- to 303.125-MHz RF signal applied to board A4 is routed to the base of transistor Q4 (buffer amplifier) through the isolating network consisting of resistors R19, R20, and R21 and coupling capacitor C14. The level of this signal is correctly set by selecting the value of R20 during final tests. The nominal value of R20 is 270 ohms. The amplified RF signal is routed from the collector of Q4 (buffer. amplifier) to the base of transistor Q5 (buffer amplifier) where it is amplified to its required level (20 milliwatts).. The output of Q5 is developed across autotransformer T2 and coupled through capacitor C19 to the isolating network consisting of resistors R29, R31, and R32. The RF output (high) signal to the main chassis is developed across R32 and routed through terminals E21 and E22 and coaxial connector P1-A1. The nominal RF output into a 50-ohm load is 20 milliwatts. The sinusoidal RF signal frequency is between 284.3750 and 303.1250 MHz. Part of the RF output developed by Q5 (buffer amplifier) is rectified by diode CR3 and filtered by capacitor C20 to supply the meter current which is routed to the transmitter meter switch through the frequency synthesizer main chassis and transmitter cabinet. The nominal meter current is 25 microamperes for 20 milliwatts into 50 ohms. The value of resistor R33 is also determined during final tests; its nominal value is 53.6K ohms.

d. The RF signal applied to board A2 is routed to the base of transistor ,Q1 (digital amplifier) through resistor R8, transformer T1, and capacitor C8. Transformer T1 and capacitor C7 comprise a bandpass filter so that signals outside the 284.375- to 303.125-MHz range are excluded. The signal is amplified by Q1 (digital amplifier) and applied to the base of dual purpose amplifier Q2 (digital amplifier) through capacitor C4. An emitter output, RF output (low), is developed across resistor R12 and routed through capacitor C10, terminal E7 and E8, and coaxial connector P1-A2 to the' electronic frequency converter 1A14A2. The nominal sinusoidal RF output from the emitter is 1 milliwatt (225 millivolts rms into 50 ohms). The collector signal of Q2 (digital amplifier) is rectified by lamp detector diode CR1 and filtered by capacitor C6. Resistor R7 provides the operational indicator lamp bias at terminal E6 which is applied to terminal 13 on board A3.

e. With the vco (Y1) and digital amplifier (Q1, Q2) on board Al operating properly, lamp bias voltage applied to terminal E13 is negative, keeping lamp driver Q3 on board A3 nonconducting. Likewise, the transistor in lamp assembly DS1 is nonconducting. Bias diode CR2 is a temperature- compensating diode cluster which varies the base voltage on lamp driver Q3 in accordance with the voltage variations between the base emitter junctions of the lamp assembly transistor and lamp driver Q3 caused by temperature variations. For example, if the temperature decreases, the base voltage of lamp driver Q3 could become positive and lamp driver Q3 may then conduct, which could cause the transistor in assembly DS1 to conduct, and light the failure indicator lamp DS1 (red); bias diode CR2 temperature regulates the base voltage of lamp driver Q3. If the RF output signal from board A2 is decreased, the bias on lamp driver Q3 becomes positive and it conducts, causing the transistor in assembly DS1 to conduct and light the failure indicator lamp DS1 (red). When the TEST pushbutton in the main chassis is pressed, a 5-volt lamp test signal is applied via pin P1-4, terminal E16, and resistor R16, to the base of transistor in assembly DS1, causing it to conduct and light the failure indicator lamp (red).

1-75. Electronic Frequency Converter 1A14A2 Circuit Theory

(figs. 8-43 and 8-44)

a. The RF output (low) signal from rf oscillator 1A14A1 is applied to board 1A14A2A1 (fig. 8-43) through coaxial connector P1-A1, terminals E7 and E8, capacitor C2, and steering diodes CR1 and CR2 to a high speed divide-by-two circuit consisting of transistors Q1, Q2, and Q3. The divide-by-two circuit operates as an a stable multivibrator. The free-running frequency of the a stable multivibrator is locked to the first subharmonic of

the RF input frequency. The switching is performed by Q1 and Q2; transistor Q3 provides a constant current input to the emitters of the switching transistors Q1 and Q2. The output frequency from the divide-by-two circuit Q1 through Q3 is amplified through RF amplifiers Q4 and Q5. Diode CR3 provides temperature compensation for the base-emitter junction of RF amplifier Q4. The output from RF amplifier Q5 is coupled through capacitor C17 to the local oscillator input port (terminal 3) of mixer Z1. A 128- MHz signal from board 1A14A2A2 is applied to the signal' input port (terminal 1) of Z1 through terminal E4 and resistor R22. The value of R22 is selected at final test to provide a minimum IF output level. The nominal value of R22 is 390 ohms. The mixer output is an- intermediate frequency in the range from 14.1875 to 23.5625 MHz. The mixer output is amplified through video amplifiers Q6 and Q7 and routed through transformer T2 to coaxial connector P1-A2 (IF output).

b. The signal in the secondary of transformer T2 is monitored to provide lamp bias. The signal is rectified by bias code CR6; the resultant negative voltage keeps lamp driver Q8 nonconducting which holds the transistor in assembly DS1 non- conducting, causing the failure lamp DS1 to be extinguished. When the if output signal amplitude falls below 1.8 volt peak-to-peak, the positive bias causes lamp driver Q8 to conduct and the transistor in lamps assembly DS1 conducts, lighting the failure indicator lamp DS1 (red). Pressing the TEST pushbutton on the frequency synthesizer main chassis applies a 5-volt lamp test signal via pin P1-3, terminal E9, and resistor R33, to the base of lamp driver Q8 which overrides the negative voltage causing it to conduct. With lamp driver Q8 conducting, the transistor in the lamp assembly also conducts, causing the failure lamp DS1 to light red.

c. Regulator diode CR5 and resistor R17 reduce the 28 volt power input to a regulated 6.2 volts for the divide-by-two circuit Q1 through Q3, RF amplifiers Q4 and Q5 and lamp driver Q8.

d. The 8-MHz signal from the standard RF oscillator 1A14A7 is applied to board 1A14A2A2 (fig. 8-44) through coaxial connector P1-A4, terminals El and E2, an isolation pad consisting of resistors, R1, R3, and R16, and capacitor C1 to the base of multiply by two Q1. The output from multiply by two Q1 is doubled to 16 MHz and doubled again in the second stage multiply by two Q2 to 32 MHz which is applied to multiply-by-four stage Q3 producing a final output signal of 128 MHz. The 128-MHz output from is then applied through emitter follower Q4 and capacitor C23 to the signal input part mixer Z1 on board 1A14A2A1. The 128 MHz output is developed across resistor R15. Rf is filtered from the +28 volt-input by RF choke L5 and RF bypass capacitors C11, C16, and C17.

1-76. AF Phase Error Detector 1A14A3

Circuit Theory

(fig. 845)

a. The 1.5625-kHz reference signal from fixed frequency divider 1A14A6 is applied through pins P1-2 and P1-3 terminals E9 and E10, and resistor R17 to transformer T1. Diode CR7 prevents spurious signals from being applied to transformer T1. The 1.5625-kHz reference signal consists of 1-microsecond positive-going pulses which cause transistor Q4 (sawtooth generator) to conduct and discharge capacitor C9. The voltage across C9 is the fundamental sawtooth waveform. A constant current generator charges C9; it comprises transistor Q3 (sawtooth generator), resistors R5, R6, and R7, capacitor C4, and temperature-compensating diode CR3. The Value of R7 is selected at final test to correctly set the peak amplitude! of the 'sawtooth. The threshold voltage from which C9 starts charging is the voltage developed across capacitor C8 which is deter- mined by the 2° and 21 correction code input signals from the fixed frequency divider which are applied through pins P1-6 and P1-16, terminals E8 and E7, and resistors R12 and R11 to digital to analog converter Q9 and Q8, respectively. The voltage developed across C8 is determined by the voltage divider consisting of diodes CR4, CR5, CR6 and resistors R13 through R16. Diode CR4 provides temperature compensation. The voltage developed across C8 is the voltage across CR4 and R13; these form a part of the voltage divider. The parallel combination of resistor R14 and R15 in series with diode CR5, and resistor R16 in series with diode CR6 form the other part of the voltage divider. When both transistors Q8 and Q9 of digital to analog converter stage are nonconducting (20 and 21 are both logic zeroes), current flows through the three parallel parts of the voltage divider and through CR4 and R13 and is maximum. When 20 is a logic one level, Q9 (digital to analog converter) is conducting and CR6 is reverse biased. For this condition, no current flows from R16 into R13, causing the voltage across CR4 and R13 to be reduced. When 2' is a

logic one level, Q8 digital to analog converter is conducting and CR5 is reversed biased. For this condition, no current flows from R15 and R13, causing the voltage across CR4 and R13 to be further reduced. The lowest voltage is developed across CR4 and R13 when both transistors Q8 and Q9 of digital to analog converter are conducting (21 and 20 are both a one level; then, the only path for current is through R14. 'Since R16 is twice R15, the voltage change with transistor Q9 (digital to analog converter) conducting is half the voltage change when transistor Q8 (digital to analog converter) conducts. The correction code can be 00, 01, 10 or 11; a logic zero corresponds to zero volt (transistor nonconducting); a logic one corresponds to 5 volts (transistor conducting). The maximum, sawtooth starting voltage corresponds to an input code of 00; its gets progressively lower from 01 to 10 and is minimum for code 11. Varying the starting voltage of the sawtooth waveform step changes the vco bias voltage. The vco bias voltage is applied to the RF oscillator 1A14A1. This results in a faster return to the phase-locked condition or faster frequency capture. The voltage developed across C8 and C9 is applied to the input of buffer stage Q5 and Q6 which buffers the composite "step" level and sawtooth signal to the input of the sample and hold circuit.

b. The sample and hold stage consists of transistor Q7, which gates the composite signal, and capacitor C14, which stores (or holds) the gated voltage level. Transistor Q7 is a dual-emitter gate which has a low resistance bi-directional conduction path between the two emitters when a positive voltage is applied between the collector and base. The gate is "opened" by the divide-by-N pulses which are applied through pins P1-13 and P1-14, terminals Ell and E12, and resistor R19 to transformer T2. Diode CR8 prevents spurious signals from being applied to T2. During normal phase-locked operation, the divide-by-N and the 1.5625-kHz reference are both the same frequency, therefore, the gate will open at the same ramp point of the sawtooth, thus keeping the charge on C14 constant and the vco bias voltage steady for a given frequency setting. Capacitor C14 charges or discharges through Q7 to the incoming sawtooth voltage while the gate is open and stores the voltage. Transistors Q10 and Q11 are a unity gain buffer amplifier and Q12 and Q13 function as a complementary pair de amplifier. The resulting vco bias voltage is filtered by the network consisting of resistors R28 through R31 capacitors C12, C13, C16, and C17. This network is a parallel-Tee filter with maximum rejection at 1.5C25 kHz. The output (vco bias) is coupled to the vco in 1A14A1 through terminals E14 and E15 and coaxial connector P1-A1. The range of dc control is set at final test by selecting the value of resistor R32. The nominal value of resistor R32 is 470 k ohms.

c. The sawtooth waveform at the output of buffer Q5 and Q6 produces a bias for ac detector Q1. The positive sawtooth signal keeps ac detector Q1 conducting which keeps the transistor in the DS1 assembly nonconducting, causing the failure lamp DS1 to be extinguished. If the sawtooth signal is not present, the base of ac detector Q1 becomes zero and is turned off. This will cause the transistor in assembly DS1 to conduct and light the failure indicator DS1 lamp red. Pressing the TEST pushbutton on the frequency synthesizer main chassis applies a 5-volt lamp test signal to pin P1-8, to terminal E1 through resistor R3, and to the base of the transistor in DS1 which lights the failure lamp.

d. Diodes CR2 and CR10 and transistor Q2 form a voltage regulator which converts the +28-volt input to +20 volts. The +20 volts is applied to the transistor circuits. Only the transistors in the lamp circuits operate directly from the 28-volt supply in order to isolate the vco bias voltage from any spurious variations.

1-77. Variable Frequency Divider No. 1 1A14A4 Circuit Theory (fig. 8-46)

NOTE

Variable frequency divider No. 1 contains integrated circuits designated Z1 through Z18. Integrated circuit types MC932, .949, 950, 963, 9002, and MSC6847L are used. These circuits are shown functionally in figure 8-46. A circuit diagram for each of these circuits is provided in figure 8-18.

a. Variable frequency divider No. 1 contains two printed wiring boards Al and A2 which provide the following circuits: clamp circuit CR1, driver Q1, divide-by-two circuit Z1, two 0.1-MHz and 1-MHz cascaded divide-by-ten counter registers, control flip-flops AND gates. The IF output frequency from 1A14A2 is applied to divided-BY two Z1, through clamp circuit diode CR1 and

driver Q1. The output from terminal 11 of divide-by-two circuit Z1 is applied to input inverter Z2 with the final inverted output from Z2 applied to the first stage (Z6) of the divide by-ten counter registers. The output pulses from input inverter Z2B are the clock pulses for the cascaded divide-by-ten counter registers. The registers count down the clock pulses until the reset enable signal from 1A14A5 is received and the registers contain the unique number (1-MHz register contains 0100-decimal 4, 0.1-MHz register contains 0110-decimal 6). After the unique number count, the initialize, inhibit, and preload sequence (3 counts) takes place. During the initialize, inhibit, and preload periods, the clock pulses are prevented from being counted. The 0.1 and 1-MHz register stages are set to all "ones" during the initialize period. During the preload period, the count (all "ones") in the counter registers is modified in accordance with the 1 and 0.1-MHz thumbwheel switch settings. After the preload period, the clock pulses are no longer inhibited and the count (determined by thumbwheel switch settings) in the registers is decremented by the incoming clock pulses. The counter registers countdown through zero until the reset enable signal is received from 1A14A5 and the unique number again appears in the registers. The cycle then repeats as described above.

b. The 0.1 and 1-MHz divide-by-ten counter registers on board A2 are binary coded decimal (BCD) counters. The 0.1-MHz divide-by-ten counter register is comprised of integrated circuits Z6 (least significant bit) Z8, Z10, and Z12 (most significant bit). The 1-MHz divide-BY ten counter register is comprised of integrated circuits Z13 (least significant bit) Z15, Z17, and Z18 (most significant bit). The registers are cascaded: the clock pulses are applied to the first stage Z6 of the 0.1-MHz register; the output stage Z12 of the 0.1-MHz register triggers the first stage Z13 of the 1-MHz register; the output stage Z18 of the 1-MHz register is inverted through count inverter Z14C and the output (count): is applied to the first stage of the 10-MHz register in variable frequency divider No. 2 1A14A5. The 0.1 and the 1-MHz divide-by-ten counter registers in 1A14A4 count down in accordance with the following chart. It should be noted the chart lists the state of each register stage for 99 through 90. For 89 through 00 the standard binary logic regression applies.

1-MHz divide-by-ten register stages				0.1-MHz divide-by-ten register stages				Decimal equiva-lent
Z18	Z17	Z15	Z13	Z12	Z10	Z8	Z6	
0	0	0	0	0	0	0	0	00
1	0	0	1	1	0	0	1	99
1	0	0	1	1	0	0	0	98
1	0	0	1	0	1	1	1	97
1	0	0	1	0	1	1	0	96
1	0	0	1	0	1	0	1	95
1	0	0	1	0	1	0	0	94
1	0	0	1	0	0	1	1	93
1	0	0	1	0	0	1	0	92
1	0	0	1	0	0	0	1	91
1	0	0	1	0	0	0	0	90
0	0	0	0	0	0	0	0	00

c. The following is a description of the divide by-ten registers (BCD down counters). As stated previously, the output from stage Z12 of the 0.1 MHz divide-by-ten counter register triggers the firs .stage Z13 of the 1.0-MHz divide-by-ten counter registers. Assume that integrated circuits Z13, Z15, Z17, and Z18 are all reset (0000). The first negative-going transition from Z12 sets Z13 and Z18 (1001). To set a flip-flop type 950 pin 4 must be at a 0-volt level; to reset the flip-flop, pin 10 must be at a 0-volt level. If the count is 0000, only 13, Z17, Z18 are conditioned to be set; however, since Z15 does not change, no transition will be applied to Z17. The second negative-going transition from Z12 resets Z13 (1000). At this time, the input to pin 9 of NAND gate Z11B is a low (0 volt) level and pin 8 is a high (5 volt) level; this now satisfies the two "ones" requirement of NAND gate Z16D, since pins Z16D-12 and 13 are both high. The third negative-going transition from Z12 sets Z13, Z15, and Z17 and resets Z18 (0111). The fourth negative-going transition from Z12 resets Z13 (0110). The fifth negative-going transition from Z12 sets Z13 and resets Z15 (0101). The sixth negative-going transition from Z12 sets Z13 and Z15 and reset Z17 (0100). The eighth negative going transition from Z12 resets Z13 (0010). The ninth negative-going transition from Z12 sets Z13 and resets Z15 (0001). The tenth negative-going transition from Z12 resets Z13 (0000).

d. Variable frequency divider No. 1 : 1A14A4 divides the IF output frequency from 1A14A2 by 200 (one divide-by-two flip-flop, and two divide by-ten counter registers). Timing for the divide by-200 operation is shown in figure 1-30.(1). The: clock pulses from Z1 are the IF output frequency from 1A14A2 divided by two. The waveform at

pin 3 (set output) of each register stage is shown from time T_0 through T_{000} (T is the period of the clock pulse). Pin 11 of Z12 is also shown since the negative-going transition of this output causes Z12 (input stage of the second divide-by-ten counter) to trigger. The width of the count signal at pin 8 of output inverter Z14C is equal to 20 periods of the incoming clock pulses (40 periods of the IF output frequency from 1A14A2). The repetition rate of the count signal at Z14C-8 is equal to 100 periods of the clock pulses (200 periods of the IF output frequency from 1A14A2). The time from T_0 to T_{20} is the width of the county pulse applied to variable frequency divider No. 2 (1A14A5). Z13, pin 11 provides the output reset signal which is used in 1A14A5 to control the width of the divide-by-N output signal.

e. The registers in 1A14A5 contain the most significant bits and will reach their unique number before the registers in 1A14A4 have reached their unique number. When the registers in 1A14A5 count down to the two most significant digits of the unique number, the reset enable signal is decoded in 1A14A5 and is applied to 1A14A4. The rest enable signal is applied as a low (O volt) level to NAND gate Z14A in 1A14A4. It is inverted to high (5 volts) level and applied as one input to NAND gates Z3A and Z3B. As shown in figure 1-30 ®. At time T35 the count in registers Z18 (most significant bit), Z17, Z15, Z13, Z12, Z10, Z8, and Z6 (least significant bit) is 01100100. Since control gate Z3 has been provided by the reset enable signal from 1A14A5, this count, which is the unique number (decimal 64), will be decoded by gates Z3A, Z3B and provide a logic zero level to Z5-4. The following positive going transition from Z1-11 will set Z5, causing gate Z2A to produce a zero level initialize signal. The initialize signal sets all register states to all "ones" and is sent to 1A14A5. The next count applied to Z6 by Z2B is inhibited by the one level applied to pin ten of Z6 by the output of NAND gate Z4B. However, the count transition from Z2B is applied to flip-flop Z7 which sets it. The inhibit signal becomes a zero level that is applied to pin 3 of NAND gate Z4B. The next count transition applied to Z6 from gate Z2B is therefore, also inhibited, but it resets flip-flop Z5 and produces a zero level output from NAND gate Z2C which is inverted by gate Z2D to produce a one level preload signal. The preload signal is applied to the switch gates in this module and in 1A14A5 causing the thumbwheel switch settings; to be gated into the registers. This is illustrated in figure 1-30 ,, where the assumption is made that the 1 and 0.1-MHz thumbwheel switch sections on the main chassis are each set at position 5. With the switches in this position, the 4 and 1 inputs to the switch gates Z9B, Z16B and Z4C, Z9D are a zero level (grounded through the switch sections). The 8 and 2 inputs are not grounded and are a one level (5 volts); these input levels are inverted in their associated gates and set the state of associated flip-flops, for this example, the count becomes 01010101. The next incoming clock pulse will reset control flip-flop Z7 and remove the inhibit signal on gate Z4B. Starting with the next clock pulse from Z2B stage Z6 will start counting down. This operation continues until all the register stages again reach zero.

f. The start of the count down for stage Z6 can be delayed by one clock period depending upon the setting of the least significant bit (1) of the 0.1MHz switch. The timing associated with this operation is shown in figure 1-31. As Z6-11 goes to a logic one state at time 35, it raises Z3B-10 to logic one forcing Z5-4 to a logic zero. This conditions Z5 to be set on the next clock pulse. Therefore, the next clock pulse (time 36) from Z2B-6 sets Z5-3 to a one. Since Z5-11 is zero, Z4B-4 is also zero. For this condition, stage Z6 is stopped from counting and Z6-3 remains a logic one. Z7-3 is forced to a one on the next clock pulse. This places a one on Z4C-9. The next clock pulse from Z2B-6 raises Z5-11 to a one causing Z4B-4 to also be a logic one. This imposes the following levels on Z4C; pin 10 is one, pin 9 is one. The output at Z4C-8 now depends on whether a one or a zero condition is programmed in on Z4C-11 from the least significant bit (1) from the 0.1-MHz thumbwheel switch. If a logic one is programmed in, Z4C-8 will go to a zero allowing Z6-3 to switch off (logic zero) at the next clock pulse. If a zero is programmed in, Z4C-8 will go to a one, thereby keeping Z6-3 at a high level when the next clock pulse occurs, and not changing state until the following clock pulse (T_{04}). The effect of the delay is to change the total count by the addition of two counts.

g. The count output pulses at output pin 11 of flip-flop Z18 are monitored by a lamp bias circuit. A negative voltage is developed at the base of the transistor in lamp assembly DS1 by diodes CR2 and CR3 which keeps the transistor nonconducting and the failure lamp extinguished. The negative bias voltage is produced by capacitor C11 discharging through diode CR3 and charging capaci

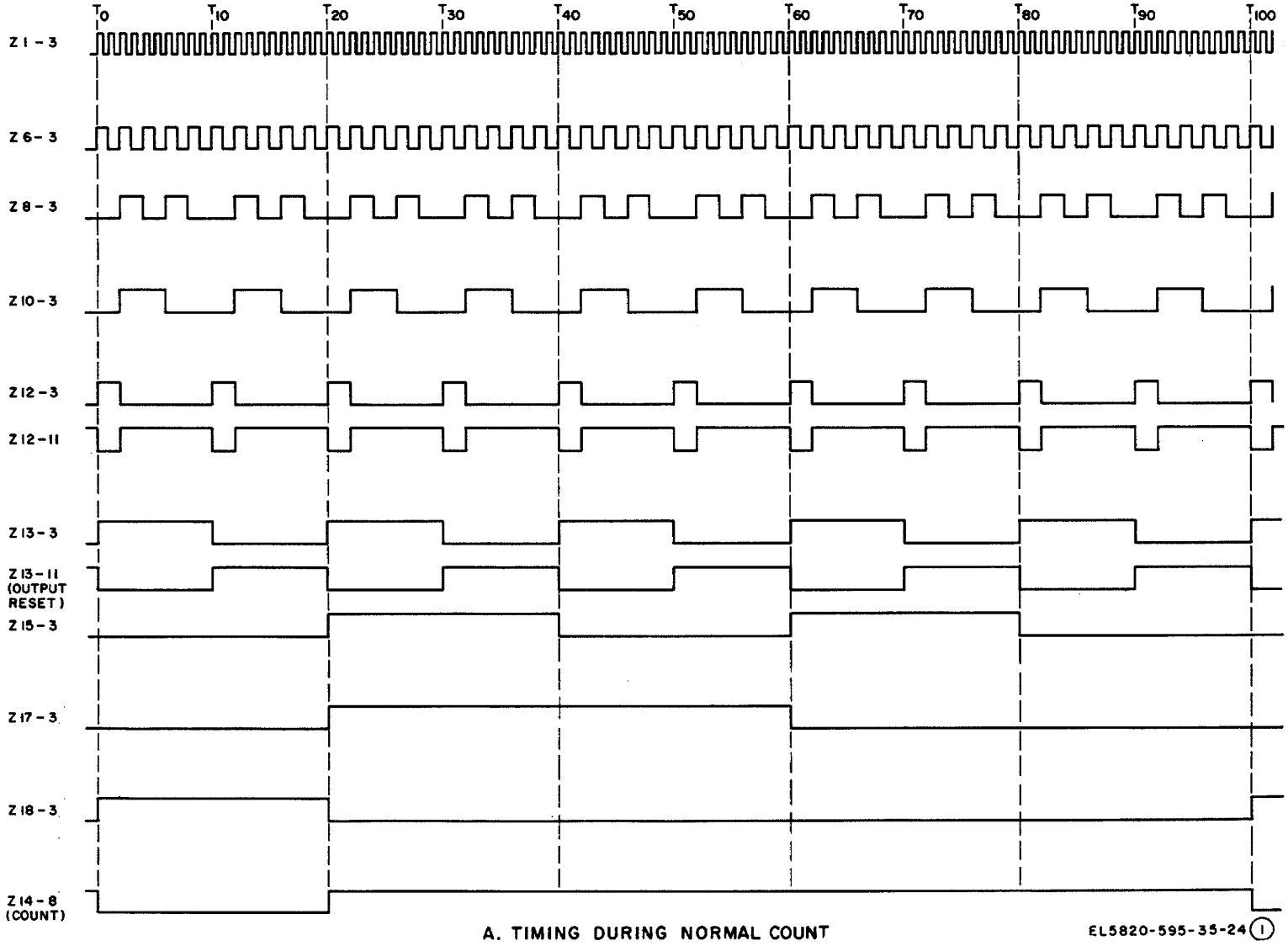


Figure 1-30 (1) . Variable frequency divider No. 1, 1A14A4, timing diagram (part 1 of 2).

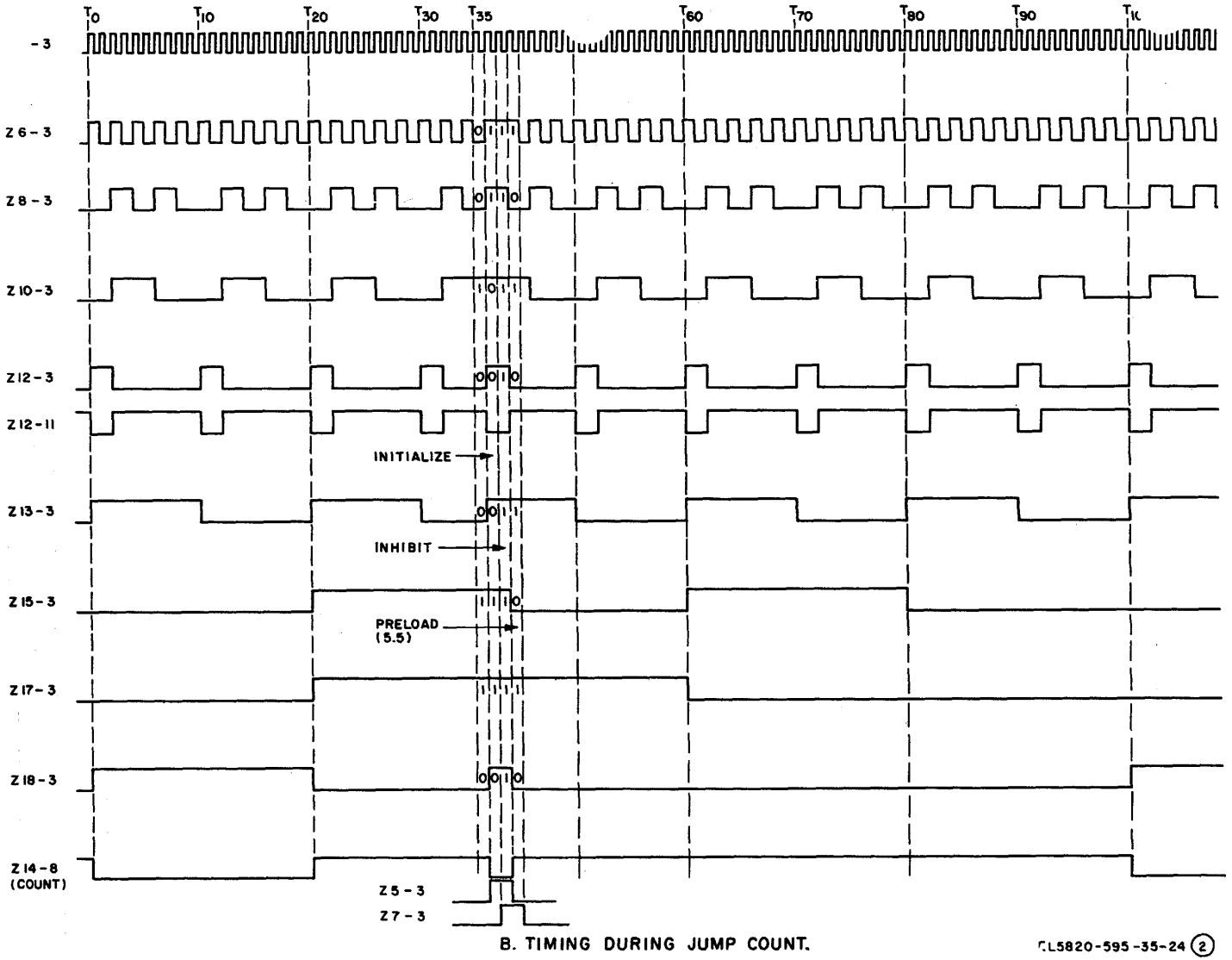


Figure 1-30.. Variable frequency divider No. 1, 1A14A4, timing diagram (part 2 of 2).

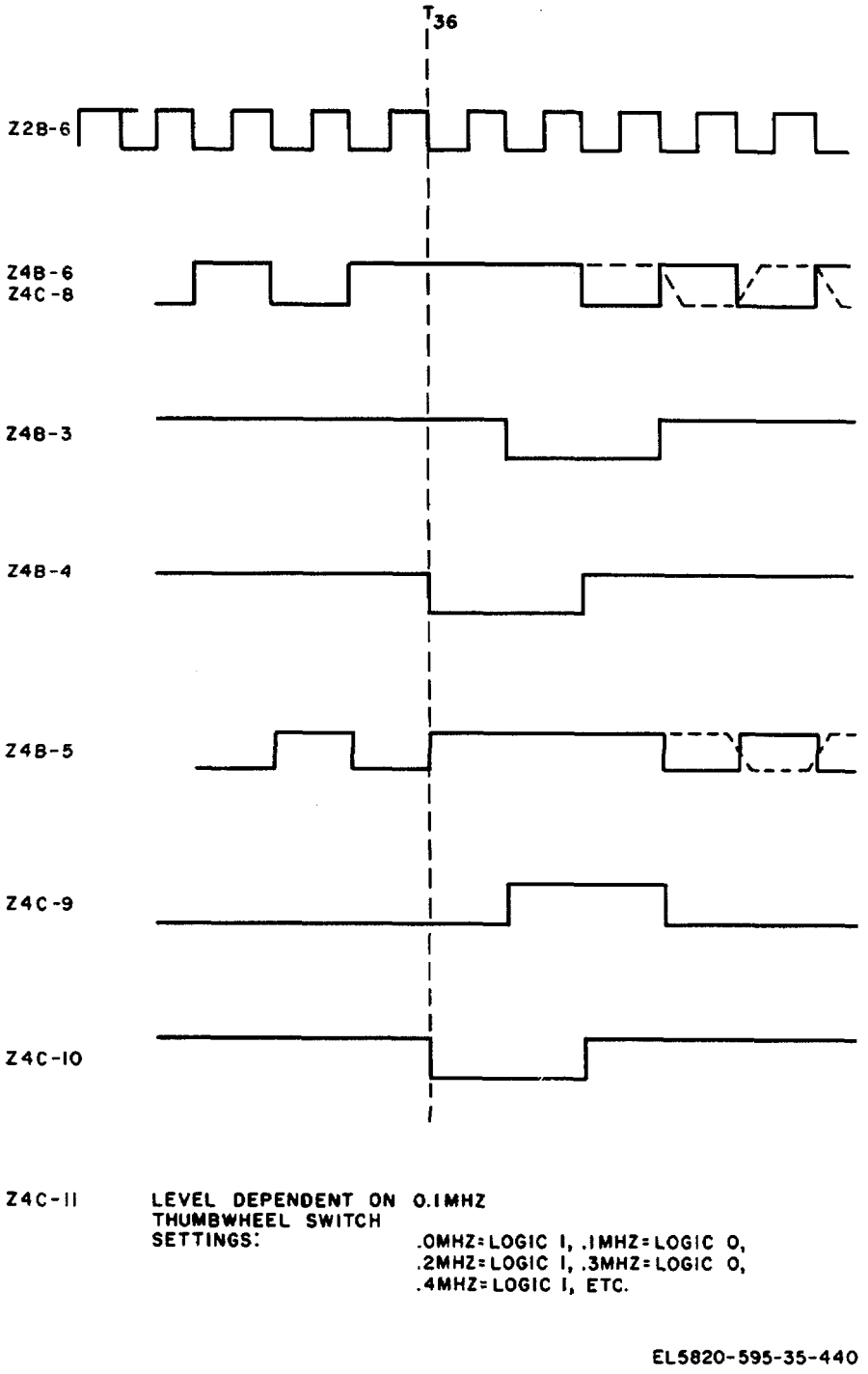


Figure 1-31. 0.1-MHz thumbwheel switch, timing diagram.

tor C12 in a negative direction with respect to ground (+5V RET). If the count signal is not present, the base of the transistor in lamp assembly DS1 becomes positive through resistor R12 and the transistor conducts, lighting the failure indicator lamp DS1 red. Pressing the TEST pushbutton on the main chassis applies a +5-volt lamp test signal to pin P1-1, terminal E19, and resistor R13 to the base of transistor in DS1, lighting the lamp red.

1-78. Variable Frequency Divider No. 2 1A14A5 Circuit Theory
(fig. 8-47)

NOTE
Variable frequency divider No. 2 contains integrated circuits designated Z1 through Z10 and Z12 through Z14. Integrated circuit types MC932, 946 and 950 are used. These circuits are shown functionally in figure 8-47. A circuit diagram for each of these circuits is shown in figure 8-18 (2).

a. Variable frequency divider No. 2 contains one printed wiring board Al which provides the following circuits: 10-MHz divide-by-ten counter registers Z2 through Z6, 100/1000-MHz divide by-eight ripple through counter registers Z7 through Z9, an output register Z10, and switch and control gates. The count signal from variable frequency divider No. 2 1A14A4 is applied to the divide-by-ten counter registers Z2 through Z6. The output from the divide-by-ten counter registers Z2 triggers the divide-by-eight counter registers. The output (divide-by-N pulses) from stage Z10 of the divide-by-eight registers is applied through output inverter stage Z18 to fixed frequency divider 1A14A6 and to af phase error detector 1A14A3. If the count in the 1A14A5, registers was not programmed by the thumbwheel switch settings (10 MHz, 100 MHz, and 1000 MHz) and the control logic in variable frequency divider No. 2 1A14A4, they would divide the count pulses by 80 (10 X 8). Both variable frequency dividers 1A14A4 and 1A14A5 would divide the IF output frequency from 1A14A2 by 16,000 (200 X 80) if they were not programmed. The registers in 1A14A5 count down the count pulses from 1A14A4 until the registers contain the unique number (divide-by-eight register contains 111-decimal 7 and divide-by-ten register contains 11110-decimal 4). The binary to decimal relationships are described later in this paragraph. Once the registers contain the unique numbers, the reset enable signal is applied to 1A14A4 to produce the initialize, inhibit, and preload sequence (3 counts). The initialize signal from 1A14A4 insures that registers are at the required count for setting in a number from the thumbwheel switches. The inhibit signal from 1A14A4 prevents the divide-by-eight register from accumulating a false count. The preload signal modifies the count (111111110) in the registers in accordance with the 10100-, 1000-MHz thumbwheel switch settings. The modified count in the registers reduces the time between the divide-by-N output pulses. -After the preload period, the count (determined by thumbwheel switch settings) in the registers is decremented by the incoming count pulses from 1A1A4. The registers count down through zero until the unique number appears again in the registers. The cycle then repeats as described above.

b. The 10-MHz divide-by-ten register stages Z2 through Z6 operate as a Johnson counter (shift register). The 100/1000-MHz divide-by-eight ripple-through register stages Z7 through Z9 operates as a standard three-stage nonsynchronous binary counter. These register stages count down in accordance with the following chart. It should be noted the chart lists the state of each register stage for 79 through 70. For 69 through 00 the standard binary logic regression applies.

c. The following describes the operation of the divide-by-ten register (Johnson Counter). The count pulses from 1A14A4 are applied to the divide-by-ten register. It is assumed that register stages Z2 through Z6 are reset (00000). The first negative-going count transition sets register stage Z2 (00001). To set a flip-flop type 950, pin 4 must be at a low (0 volt) level; to reset the flip-flops, pin 10 must be at a low (0 volt) level. When the registers state is 00000, only Z2 is conditioned by Z6 to be set; stages Z3 through ZC are conditioned to be reset, but, since they are already reset, their status is not changed. After Z2 has been set its outputs condition Z3 to be set. The second incoming negative-going count transition sets Z3 (00011); the third negative-going count sets Z4 (00111); the fourth negative-going count sets Z5 (01111); and the fifth negative-going count sets Z6 (11111). Setting Z6 primes the

10011000-MHz divide-by-eight register stages				10-MHz divide-by-ten register stages (Johnson counter)				Decimal equiva-lent
Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	
0	0	0	0	0	0	0	0	00
1	1	1	0	0	0	0	1	79
1	1	1	0	0	0	1	1	78
1	1	1	0	0	1	1	1	77
1	1	1	0	1	1	1	1	76
1	1	1	1	1	1	1	1	75
1	1	1	1	1	1	1	0	74
1	1	1	1	1	1	0	0	78
1	1	1	1	1	0	0	0	72
1	1	1	1	0	0	0	0	71
1	1	1	0	0	0	0	0	70
0	0	0	0	0	0	0	0	00

reset input pin 10 of stage Z2. The next five negative-going counts will advance the one through the reset side of register stages Z2 through Z6 and eventually return the registers to 00000.

d. The -10-MHz divide-by-ten counter Z2 through Z6 is a Johnson counter or shift register. Stages Z6, Z5, Z4, Z3, and Z2 are programmed by the A, B, C, D, and E inputs respectively from the 10-MHz thumbwheel switch. The divide-by-eight ripple-through counter Z7 through Z9 is a three stage nonsynchronous binary counter. Stages Z8 and Z7 are programmed by the B and C inputs respectively from the 100/10000-MHz thumbwheel switch. Stage Z9 (most significant bit) is not programmed; the programmed input (reset) is connected permanently to logic 1 (+5 vdc). Because the reset input to Z9 is permanently connected to a logic one, the lowest number that can be programmed into the divide-by-eight register is decimal 4 or 100 binary.

e. If the count was not programmed by the control logic in variable frequency divider No. 1 1A14A4 and the thumbwheel settings, the registers in 1A14A5 would divide the count pulses from 1A14A4 by 80 as illustrated in figure 8-48. The count pulses are shown across the top of the diagram from time T_0 through T_{8000} (T is the period of the clock pulses applied to the registers in 1A14A4). Note that the repetition rate of the count pulses is equal to 100 periods of the clock pulses. The waveform at pin 3 (set output) of each register stage is shown from time T_0 through T_{8000} Immediately preceding time. To all register stages Z2 through Z10 are zero; at To the negative-going count transition sets Z2 which, in turn, sets Z7 through Z10. When Z10 is set the divide-by-N output pulse starts. When Z2 is set it conditions Z10 to be reset, and, when the output reset signal from variable frequency divider No. 1 1A14A4 is applied to Z10 (40 time periods at the incoming IF frequency; time T), Z10 is reset and terminates the divide-BY N pulse. The count continues (assuming registers are not programmed) through time T_{8000} and the cycle is repeated.

f. The following describes how the count in the 1A14A5 registers is modified by the control signals from variable frequency divider No. 1 1A14A4 and the 10-, 100 and 1000-MHz thumbwheel switch settings. The timing for the modified (jump) count is shown in figure 1-32. The count pulses are shown across the top of the diagram. The count from time T_o until T_{000}, is the same as described in the previous paragraph. At time T_{000}, the count in registers Z9 through Z2 is 11111110 which is the unique count (decimal 74). For this condition, the inputs to reset enable gate Z1A and diode CR3 are all at a high (5 volts) level. Gate Z1A produces a low (0 volt) level which is the reset enable signal applied to variable frequency divider No. 1 1A14A4. Variable frequency divider No. 1 will produce the initialize signal (a low (0 volt) level) which resets Z2 and sets Z3 through Z6 and Z9. One clock pulse later, variable frequency divider No. I 1A14A4 will produce the inhibit signal (a low (0 volt) level) which is inverted by gate Z14C and prevents Z7 from being reset when Z2 changes state. The next clock pulse causes variable frequency divider No.1 1A14A4 to produce the preload signal (a high, 5,-volt level) which is applied to the switch, gates. The thumbwheel switch settings are gated into the registers. This is illustrated in figure 1-32 where it is assumed that the 1000-, 100-, and 10MHz thumbwheel switch sections are set at 45 and 6 respectively. The 1000 and 100-MHz setting of 45 preloads decimal number 5 (binary 101) into stages Z9, Z8, and Z7. The 10-MHz setting of 6 preloads decimal number 6 (01111) into Johnson counter stages Z6, Z5, Z4, Z3, and Z2. With the 1000 and 100-MHz switches in these positions, signal B' is a high (5 volts) level and signal A is a low (0 volt) level (grounded through the switch section). With the 10-MHz switch set at 6, signal A is a low (0 volt) level (grounded through the switch section) and signals B, C, D, and E are at a high (5 volts) level. The preload signal sets the count into register stage Z9 through Z2; the registers assume the state 10101111. Assuming that the 1 and 0.1-MHz thumbwheel switches are both set to 5, causing the registers in 1A14A4 to contain decimal 55, the count is jumped from time T_{540} to time T_{5655}. The clock pulses applied to the registers in 1A14A4 and the count pulses applied to the register in 1A14A5 will now decrement the count until all registers are zero producing the divide-by-N pulses from output inverter Z1B in 1A14A5. The width of these pulses is determined by the conditioning of pin 10 of Z10 from Z2-11, thereby allowing it to be reset by the output reset signal from 1A14A4.

g. The divide-by-N pulses are monitored at the output register Z10 to provide lamp bias. These

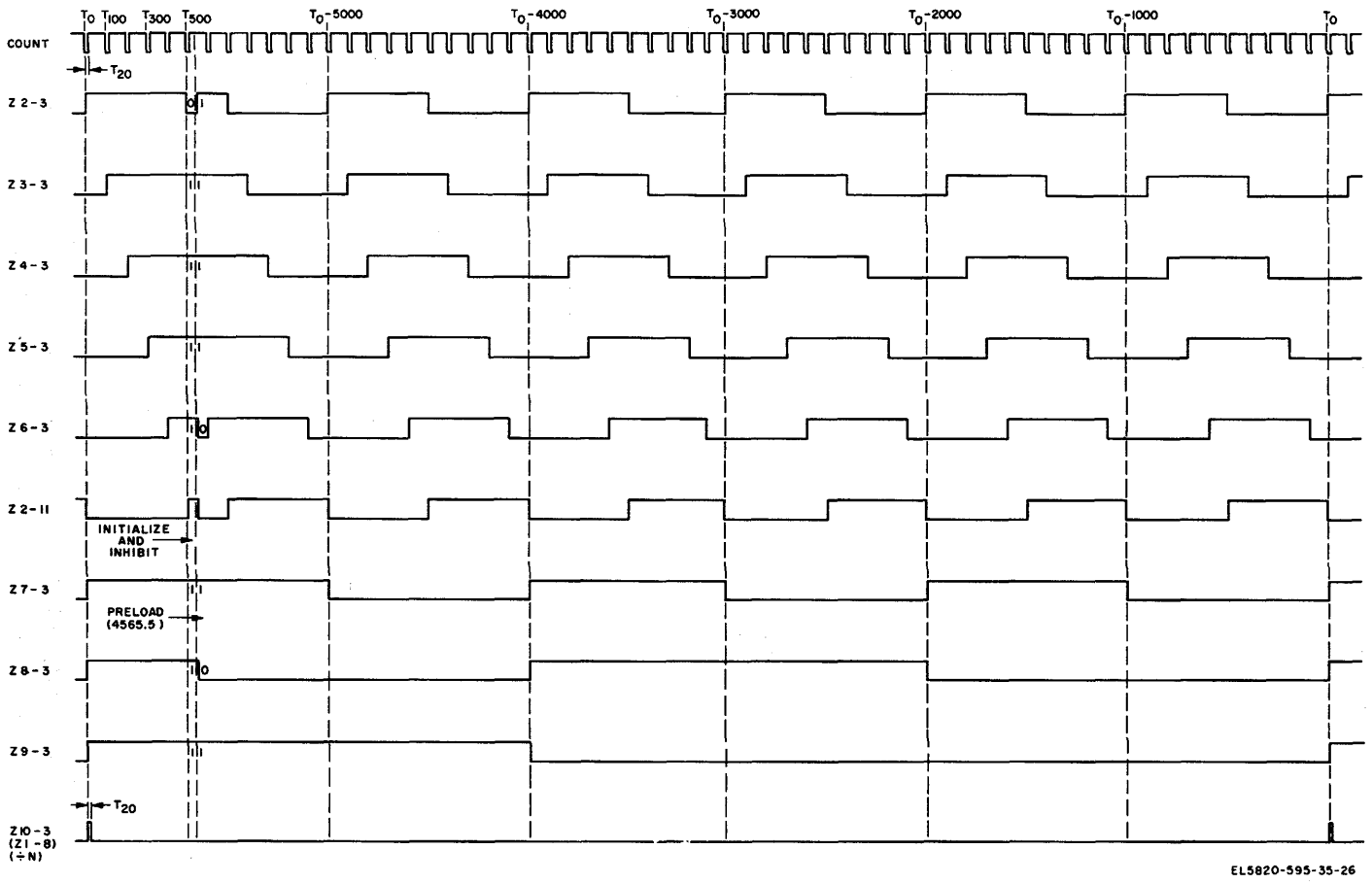


Figure 1-32. Variable frequency divider No. 2, 1A14A5, timing # with jump count.

pulses develop a positive voltage through diode CR1 keeping lamp driver Q1 conducting. With lamp driver Q1 conducting, the transistor in lamp assembly DS1 is held nonconducting. When the divide-by-N signal is not present, lamp driver Q1 becomes nonconducting and the transistor in DS1 conducts, lighting the failure indicator DS1 lamp red. Pressing the TEST pushbutton on the main chassis applies a 5-volt lamp test signal through terminal E23 and resistor R12 to the base of the transistor in DS1, causing the failure lamp DS1 to light red.

1-79. Fixed Frequency Divider 1A14A6 Circuit Theory (fig. 8-49)

NOTE

Fixed frequency divider 1A14A6 contains integrated circuits designated Z1 through Z24. Integrated circuit types MC932, 946, 950, and 9002 are used.

These circuits are shown functionally on figure 8-49. Circuit diagrams for each of these circuits is shown on figure 8-18 *a.* The 8-MHz sinusoidal signal from the standard RF oscillator' (1A14A7) is applied through pins P1-8 and P1-6 and terminals E1 and E2 to transformer T1 on board 1A14A6A2. Clamp diode CR2 across the secondary of transformer T1 clamps the signal which is then applied to divider Z1 through inverter Z15D. Divider stages Z1 through Z10 divide the incoming 8 MHz signal by 1024, each stage provides divide-by-two. The slip-flops, type 950, are set or reset from the previous circuit by a negative-going transition at pins 5 and 6; it is set when pin 4 is a low (0 volt) level and reset when pin 10 is a low (0 volt) level. The 7.8125 kHz output from Z10 is divided by five divider stages Z11 through Z13 (total divide 5120 by stages Z1 through Z13) to produce the 1.5625kHz reference signal. Figure 1-33 illustrates the countdown in stages Z1 through Z15. A, figure 1-33, shows. the timing for stages Z1 through Z5; B, figure 1-33 shows the timing for stages Z5 through Z10; and C, figure 1-33 shows the timing for stages Z10 through Z15. The pulse width of the 1.5625-kHz output of Z13 is changed to a 1 microsecond pulse width by output register Z14. The output frequency of Z14 is still 1.5625-kHz since only the pulse duration has been changed. The 1.5625-kHz signal is then routed through inverter Z24A to. the AF phase error detector 1A14A3 and to board 1A14A6A1.

b. The 1.5625-kHz reference signal is applied through pin P1-4 and terminal E20 to input gate Z16A and counter gate Z18A. The divide-by-N signal is applied through pin P1-7 and terminal E21 to input gate Z16B and counter gate Z18B. Both signals are illustrated on A, figure 1-34. Two timing conditions are shown in A, figure 1-34; both are phase-locked loop conditions. The waveforms on the left side of A, figure 1-34 show the leading edges of the 1.5625-kHz reference and divide-by-N (tN) pulses occurring at the same time. The waveforms on the right side of A, figure 1-34 show a slight time lag between the 1.5625kHz reference and the --N pulses, corresponding to a different RF output frequency from the RF oscillator (1A14A1). In either case, the repetition rate of the divide-by-N pulses is 1.5625 kHz. The two incoming signals (1.5625-kHz reference and divide-by-N pulses) alternately set and reset flipflop Z17 with their pulse trailing edges. As shown in A, figure 1-34, the output of counter gates Z18A and Z18B are unchanged by the input signals. However, when the divide-by-N signal is interrupted (or its frequency is not exactly 1.5625 kHz) as illustrated in B, figure 1-34, the next 1.5625-kHz reference pulse sets flip-flop Z17 which remains set; the next pulse develops as output from counter gate Z18A which triggers flip-flop Z19. Each succeeding pulse triggers flipflop Z19 which then begins the counting in flipflops Z20 through Z23 as shown in figure 1-35. The output from flip-flop Z22 becomes the 20 correction code that is applied to the AF phase error detector 1A14A3, the output from flip-flop Z23 becomes the 21 correction code. These signals will only change after a significant change in either input. When the 1.5625-kHz signal is interrupted, the output of the AF phase error detector 1A14A3, the RF voltage controlled oscillator 1A14A1, the electronic frequency converter 1A14A2, and variable frequency dividers No. 1 and No. 2 1A14A4 and 1A14A5 are all affected; the overall frequency synthesizer operation for this case is considered nonoperating.

c. When the 1.5625-kHz and divide-by-N signals are phase-locked, the input and output of flip-flop Z19 are unchanged and no signals are applied to inverter Z24B. In this state, alarm driver Q2 is nonconducting and the collector voltage is 3.5 volts dc (normal condition). This voltage is applied to alarm monitor 1A5 in the transmitter cabinet as the phase-lock alarm through the main chassis. If the two signals are not in proper phase, flip-flop Z19 generates a square wave which biases alarm driver Q2, causing it to conduct

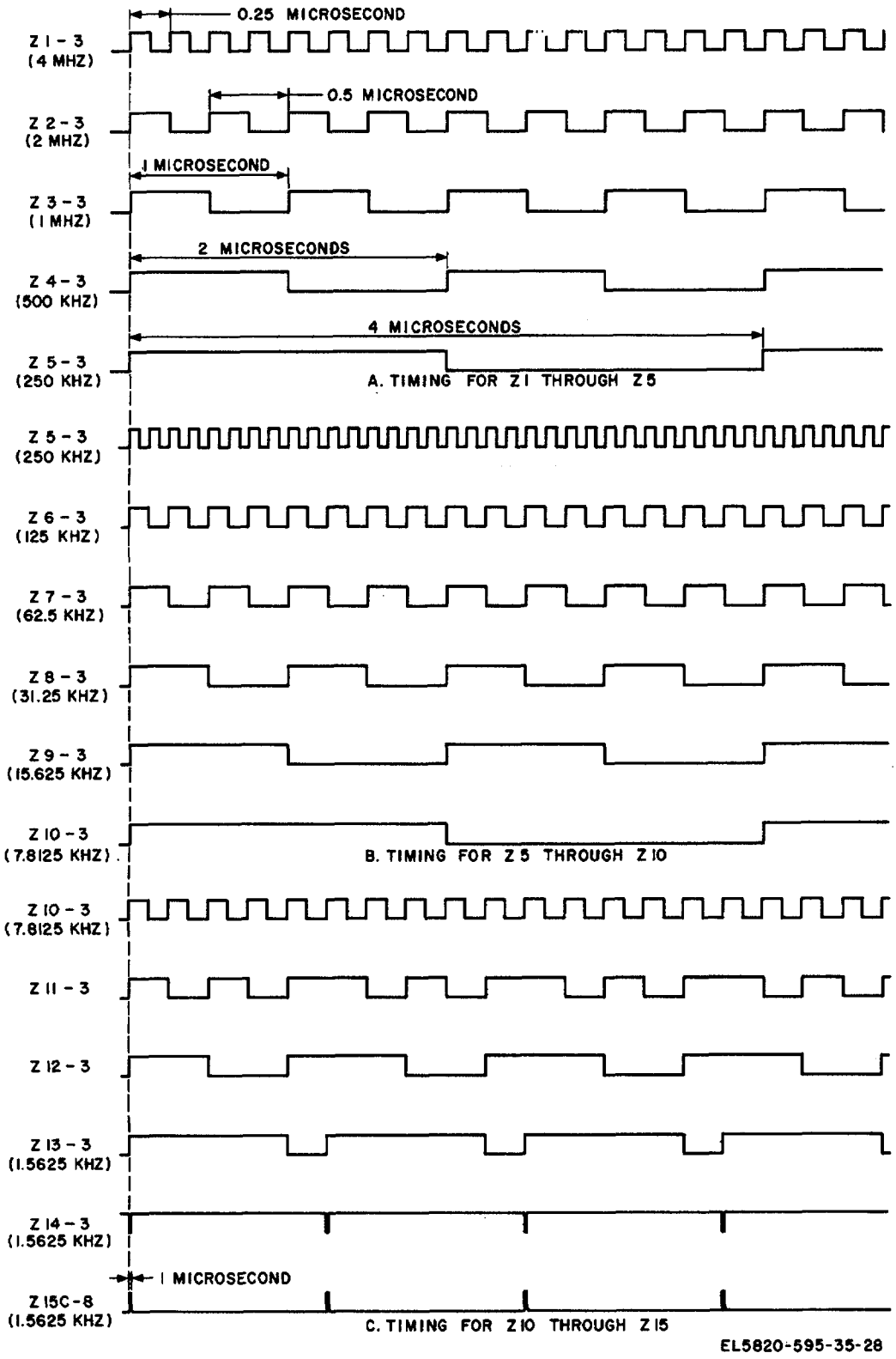


Figure 1-33. Fixed frequency divider, timing diagram.

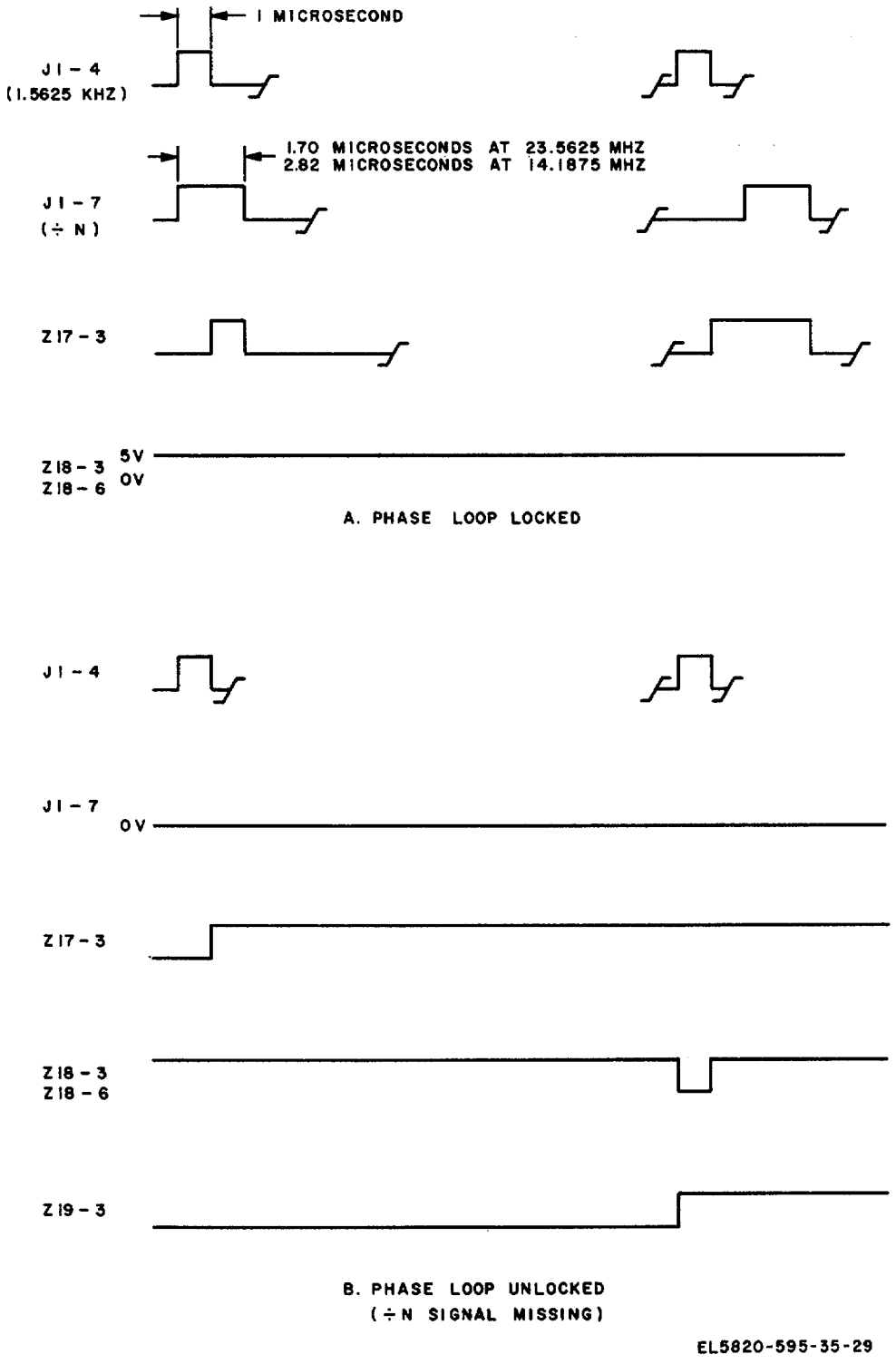


Figure 1-34. Fixed frequency divider phase detector, timing diagram.

and reduces the phase-lock alarm voltage to 0 volt (alarm condition). If the 1.5625-kHz signal is interrupted, flip-flop Z19 will not generate bias for alarm drive Q2 due to lack of signal; however, diode CR5 will bias alarm driver Q2 and change the phase-lock alarm voltage to 0 volt (alarm condition).

d. The 1.5625-kHz output from flip-flop Z13 is monitored to produce a lamp bias for lamp driver Q1 through diode CR3. Lamp driver Q1 is normally conducting, and the transistor in lamp assembly DS1 is nonconducting causing the failure lamp DS1 to be extinguished. When the 1.562,-kHz signal is interrupted lamp drive Q1 becomes nonconducting and drives the transistor in lamp assembly DS1 into conduction, lighting the failure lamp DS1 red. Pressing the TEST pushbutton on the main chassis applies a 5-volt lamp test signal through pin P1-9 terminal E12, and resistor R4 to the base of the transistor in lamp assembly DS1 to conduct and the failure lamp DS1 to light red.

1-80. Standard RF Oscillator 1A14A7
(fig. 841)

The standard RF oscillator 1A14A7 consists of a sealed module which contains a stable quartz crystal oscillator which is fully transistorized and uses integrated circuits and proportional oven control for maximum stability and reliability. The oscillator produces an 8.0-MHz sine wave signal with an RF output of 0.7 vrms ±2 db. It has a built-in oven with a temperature sensor which indicates when the oven is above 75°C. The temperature

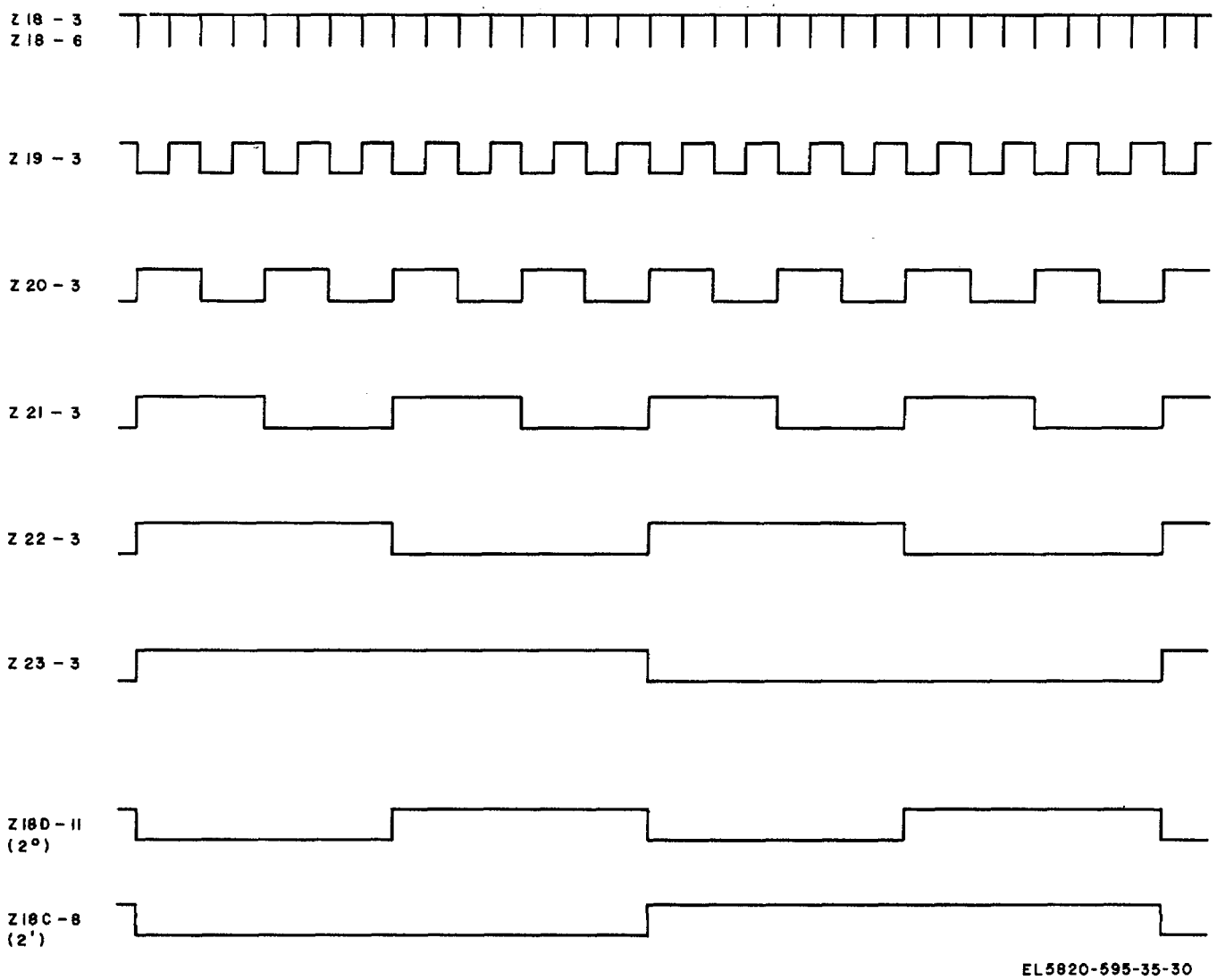


Figure 1-35. Fixed frequency divider phase detector, timing diagram with phase loop unlocked.

sensor contacts remain closed when the oven temperature is below 75° C. A frequency adjustment control is provided to compensate for aging and to allow the oscillator to be set within 5 x 10^{-8}.

1-81. Dual Power Supply 1A14A8B (fig. 8-41)

The dual power supply 1A14A8 consists of a sealed module which contains transistorized circuits that rectify 115 volts ac and produce two separate dc outputs: 28 volts and 5 'volts. The input ac voltage may vary from 103.5 to 126.5 volts and from 50 to 400 Hz and the dc outputs Will remain constant. The 28-volt output is rated for a full-load current of 450 milliamperes. The minimum full-load current for the 5-volt output is 750 milliamperes.

Section IV. FUNCTION OF RECEIVER

1-82. General

This section provides block diagram descriptions and circuit functions for the receiver. The areas covered are-block diagram description of the major signal flow, block diagram descriptions of assemblies and modules; and, circuit theory of modules at the schematic diagram level. Reference to circuits previously described in the transmitter section (sec. III) are made where applicable (i.e. frequency synthesizer 2A21 (receiver) is identical to frequency synthesizer 1A14 (transmitter). Modules common to the transmitter and receiver (i.e., AF-RF amplifier and alarm monitor) which have different functional descriptions are described in their respective transmitter and receiver block diagram descriptions.

1-83. Receiver Block Diagram Description

(fig. 8-50)

a The signals paths through the receiver, the functional relationships between the receiver modules. alarm, and signal level monitoring functions are illustrated in figure 8-50. The receiver is a dual diversity superheterodyne receiver providing diversity operation by means of two input circuits, channel A and channel B. This discussion will describe the signal path through the functional modules related with the operation of channel A only, since the signal path through channel B is identical to channel A with the exception of different module reference designations as indicated in figure 8-50.

b. An RF input signal in the frequency range of 4400 to 5000 MIHz from the directional coupler 4A5 is applied the input of preselector 2FL4 of channel A. Preselector 2FL4 is tuned to the specific receiver operating frequency within the 4400 to 5000 3Hz range. Filtered output signal from preselector 2FL4 is then applied to TDA 2A1 which amplifies the signal, provides isolation and improves the signal-to-noise ratio. The output of TDA 2A1 is applied to post selector 2FL6 which is tuned to the specific receiver operating frequency and suppresses the passage of the out of-band noise generated by TDA 2A1. The filtered output signal from post selector 2FL6 is applied to 4400 to 5000-MHz circulator 2HY1 which provides isolation between the previous modules and mixer preamplifier 2A4.

c. Mixer preamplifier 2A4 mixes the 4400 to 5000-MHz RF signal from 4400 to 5000-MHz circulator 2HY1 with the 4330 to 5070-MHz local oscillator signal from local oscillator filter 2FL8 which is 70-MHz above or below the 4.4 to 5.0GHz RF signal of channel A. The 4330 to 5070-MHz local oscillator signal' is developed in frequency mixer 2A6 by mixing the 220-MHz output signal from 220-MHz VCO 2A13 with the 4550 to 4850-MHz output signal from frequency multiplier group 2A7.

d. The 4550 to 4850-MHz input to frequency mixer 2A6 is produced by a series of modules starting with frequency synthesizer 2A21. The frequency synthesizer generates a highly stable frequency in the range of 284.375 to 303.125 MHz. The 284.375 to 303.125-MHz frequency synthesizer output is amplified and multiplied (X4) up to a 1137 to 1214-M3Hz signal by amplifier multiplier 2A8. The 1137 to 1213-MHz signal is applied through bandpass filter 2FL 10 and circulator 2HY3 to frequency multiplier group 2A7. The circulator provides isolation between the frequency multiplier modules. The frequency multiplier group multiplies (X4) the 1137 to 1213 MHz signal up to a 4550 to 4850-MHz signal for application to frequency mixer 2A6. A detailed description (using specific receiver frequencies) of the signal mixing process is provided in paragraph 1-84.

e. The 4330 to 5070-MHz local oscillator signal from frequency mixer 2A6 is then applied to local oscillator filter 2FL8 which is tuned to pass a

signal that is 70 MHz above or below the 4400 to 5000-MHz RF signal to channel A. The 70-MHz output signal from mixer preamplifier 2A4 is applied to 70-MHz IF filter 2A5 which allows passage of 70-MHz signal to IF amplifier 2A12. The amplified 70-MHz IF signal is then applied to combiner 2A16. An AGC output, porportional to the received RF signal level, is. also applied from the IF amplifier to antenna alignment indicator 4A7 via shelter connectors.

f. The combiner 2A16 monitors the level of channel A and B signals and either combines the signals or selects one of the signals, depending upon their relative magnitude, for application to demodulator 2A17. When the channel IF signal levels are within a predetermined level ratio (8 db) with respect to each other, the signals are combined and applied to demodulator 2A17. When the predetermined level ratio is exceeded, the combiner inhibits the weaker signal and only the stronger signal is applied to the demodulator 2A17. An age (automatic grain control) circuit in the combiner provides common age signals to the channel A and channel B IF amplifiers 2A12 and 2A15. An age cross-connection between the channel A and channel B IF amplifiers 2A12 and 2A15 provides common age operation for diversity operation. The age level after amplification in the combiner 2A16 is also applied to digital data modem 1A12 in the transmitter. The combiner also provides automatic phase control (ape) circuits for channel A and channel B. The ape A and B signals are fed back from the combiner to automatically control and synchronize the 220MHz vco signal associated with each channel. This results in frequency synchronization of the 70MHz IF signal for each receiver channel which is required for proper combining of the IF signals.

g. The 70-MHz combined or selected IF output signal from the combiner 2A16 is applied to demodulator 2A17 which converts the combined or selected IF signal to a PCM/order wire signal. This signal is then applied to low pass filter 2A18. For 12-channel operation, a 260-kHz low pass filter is provided; for 24-channel operation, a 680-kHz low pass filter is provided. After filtering, the signal is amplified by AF-RF amplifier 2A19 and the amplified signal (TRAFFIC)UTPUT) is applied to the digital data modem '1A12 in the transmitter.

h. Alarm monitor 2A20 controls the alarm indicators on the receiver meter panel. Alarm signals from various receiver modules are applied to the alarm monitor. Under normal operating conditions all alarm indicators are lighted green. When an alarm condition occurs, the alarm monitor causes the associated alarm indicator on the meter panel to light red. Also, when any one of the receiver alarm conditions occur, the alarm monitor provides a receiver summary alarm signal which is applied to the transmitter and causes the CNTRL ALARM indicator on the transmitter meter panel to light red.

i. The receiver provides metering circuits to monitor the signal level outputs of various receiver modules. The signal levels are applied to the meter selector switch 2A22S1 on the receiver meter panel and can be applied to the metering circuit by setting the meter selector switch 2A22S1 to the desired position. The meter panel also provides oven monitoring indicators for frequency synthesizer 2A21, TDA 2A1 and 2A2, and 220 MHz vco 2A13 and 2A14. The frequency synthesizer and 220-MHz vco indicators light white when the associated ovens are at the correct temperature. The TDA indicators normally cycle on (which) and off to indicate whether the TDA ovens are on or off.

j. Power supply 2A3 provides the dc supply voltages required to operate the receiver modules.

1-84. Receiver Frequency Mixing Process Block Diagram Description (fig. 1-36)

a. Since channels A and B process the receive signals identically, only the signal processing for channel A is illustrated in figure 1-36. Assume that the receiver is tuned to 4500 MHz as shown in A, figure 1-36. The frequency dial on preselector 2FL4 and post selector 2FL6 are set to 4500 MHz allowing the 4500-MHz RF input signal to enter mixer preamplifier 2A4. The thumbwheel switches on frequency synthesizer 2A21 are also set to 4500 MHz corresponding to a frequency synthesizer output of 290.625 MHz. The 290.625MHz output is multiplied by four up to 1162.5 MHz in amplifier-multiplier 2A8 and passed through 1137 to 1213-MHz bandpass filter 2FL 10 and 1137 to 1213-MHz circulator 2HY3 to frequency multiplier group 2A7. The frequency multiplier group multiplies the 1162.5-MHz signal by four up to 4650 MHz. Frequency mixer 2A6 mixes the 4650-MHz signal with the 220-MHz signal from 220 MHz vco 2A13 producing sum and difference frequencies 4430 and 4870 which are applied to local oscillator filter 2FL8. When the dial on the local oscillator filter 2FL8 is set for a

receiver frequency of 4500 MHz, the local oscillator filter is tuned to the difference frequency (4430 MHz) which is 70 MHz below the receiver frequency (4500 70 MHz = 4430 MHz). Therefore, the calibrated filter dial setting of 4500 MHz is 70 MHz above the frequency the local oscillator filter is tuned to. The 4430-MHz difference frequency is mixed with the 4500-MHz channel A RF input signal in mixer preamplifier 2A4 producing sum and difference frequencies (8930 MHz and 70 MHz). The 70-MHz difference frequency is amplified in mixer preamplifier 2A4 and passed to the channel A IF amplifier via 70 MHz IF filter 2A5.

b. Assume that the receiver operating frequency is set to 4800 MHz as shown in B, figure 1-36. The signal processing is similar to that described above for the 4500-MHz RF signal input. The frequency dials on preselector 2FL4, post selector 2FL6, local oscillator filter 2FL8, and frequency synthesizer 2A21 are all set to 4800 MHz. The 4800-MHz dial readout of frequency synthesizer 2A21 corresponds to a frequency synthesizer output frequency of 290.625 MHz, the same as the 4500-MHz dial setting. The 290.625MHz signal from frequency synthesizer 2A21 is again multiplied (X 16) to 4650 MHz, where it is mixed in frequency mixer 2A6 with the 220-MHz signal from 220 MHz vco 2A13 producing sum and difference frequencies of 4870 and 4430 MHz which are applied to local oscillator filter 2FL8. When the dial readout of the local oscillator filter is set for a receive operating frequency of 4800 MHz, the local oscillator filter is set to the sum frequency (4870 MHz) which is 70 MHz above the receiver operating frequency (4870 4800 MHz = 70 MHz). Therefore, the calibrated local oscillator filter dial setting at 4800 MHz is 70 MHz above the receiver operating frequency (4800 MHz) to which the local oscillator filter is tuned. The 4870-MHz signal passed by the local oscillator filter is mixed with the 4800-MHz channel A RF input signal in mixer preamplifier 2A4 producing sum and difference frequencies (9670 MHz and 70 MHz). The 70-MHz component of the mixed signal is amplified in the mixer preamplifier and passed to the channel A IF amplifier 2A12 via 70-MHz IF filter 2A5.

1-85. RF Input and Mixing Circuits Block Diagram Description (fig. 8-51)

The RF input and mixing circuits are shown in figure 8-51. Since identical circuits are used in 1-126 channel A and channel B, only the channel A circuits are described. -.

a. Preselector 2FL4. Preselector 2FL4 is a four-pole (four cavity) bandpass filter that is set to the incoming RF frequency in the 4.4 to 5.0 GHz band. The preselector is directly at the input to the receiver and passes only the desired RF signal to TDA-A 2A1. Each of the four tuning cavities is ganged to a single frequency adjust control dial with direct readout of the frequency to which the preselector is set. The bandwidth of the preselector is nominally 25 MHz with a maximum insertion loss of 0.65 db.

b. Tunnel Diode Amplifier A (TDA-A) 2A1. TDA-A 2A1 amplifies the RF signal (4.4 to 5.0 GHz) from preselector 2FL4 and provides a low noise figure for channel A. TDA-A consists of a tunnel diode assembly and an oven assembly. The oven maintains the tunnel diode assembly above a predetermined temperature. When the oven is on (heating), the TDA-A OVEN indicator on the meter panel lights white. The tunnel diode amplifier provides 21.5 + 1.5 db gain in the frequency range 4.4 to 5.0 GHz at a noise figure of 4.55 db maximum. The output of TDA-A is applied to post selector 2FL6.

c. Post Selector 2FL6. Post selector 2FL6 is a two-pole (two cavity) bandpass filter that is set to the incoming RF frequency in the 4.4 to 5.0-GHz band. In addition to passing the desired RF signal, the post selector inhibits out-of-band noise from the tunnel diode amplifier 2A1 thereby maintaining the correct noise figure for the receiver. Each of the tuning cavities is ganged to a single frequency adjust control with direct readout dial of the frequency to which the post selector is set. The bandwidth of the post selector is nominally 30 MHz with a maximum insertion loss of 0: 85 db. The output of post selector 2FL6 is applied to 4.4 to 5.0-GHz circulator 2HY1.

d. 4.4 to 5.0-GHz Circulator 2HY1. The 4.4to 5.0-GHz circulator 2HY1 provides an impedance match between post selector 2FL6 and mixer preamplifier 2A4. The 4.4to 5.0-GHz circulator 2HY1 also provides additional isolation between local oscillator filter 2FL8 and post selector 2FL6

e. Mixer Preamplifier 2A4. Mixer preamplifier 2A4 converts the channel A 4.4to 5.0-GHz RF input signal to the channel A 70-MHz IF signal. The conversion is made by mixing the RF input signal (4.4 to 5.0 GHz) with the local oscillator signal (4.33 to 5.07 GHz) which is 70 MHz above

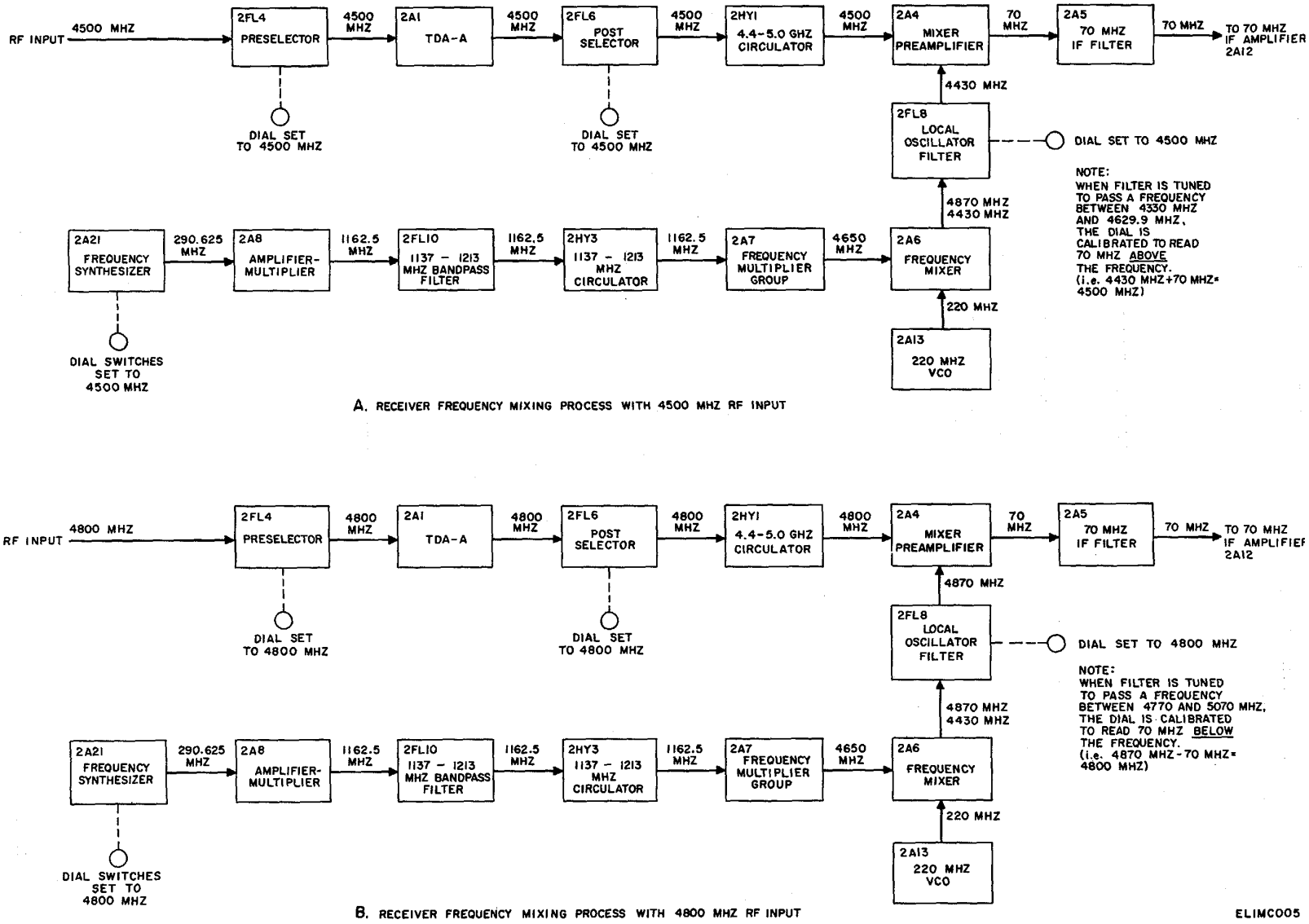


Figure 1-36. Receiver frequency mixing process, block diagram.

or below the receiver RF input frequency. The output of mixer preamplifier 2A4 is applied to 70-MHz IF filter 2A5.

(1) The mixer preamplifier consists of a coaxial balanced mixer 1A4Z1, and three preamplifier states Q1 through Q3. The RF input signal (4.4 to 5.0 GHz) is applied to-one input (J1 1.7 IN) of mixer 2A4Z1, and the local oscillator signal is applied to its second input (J2 LO IN)

(2) The RF input signal (4.4 to 5.0 GHz) is mixed with the local oscillator signal (4.33 to 5.07 GHz), which is 70 MHz above or below the RF signal, in mixer 2A4Z1. This produces sum and difference frequencies, one of which is the 70-MHz difference frequency. Only the 70-MHz IF frequency produced by mixing the two signals appears at the output of the mixer 2A4Z1 and is amplified by the preamplifier stages (Q1 through Q3).

(3) IF ADJ control in the input circuit of first preamplifier Q1 is a variable inductor (L3) that is adjusted to produce an IF bandpass response centered at 70 MHz by resonating with the sum of the mixer (2A4Z1) output capacitance and preamplifier Q1's input capacitance. Preamplifier Q1 is a fixed tuned, wide band low noise amplifier stage which determines the noise figure of the mixer preamplifier. Preamplifier Q2 is also a fixed tuned, wide band amplifier stage with variable gain capability (R12). Preamplifier Q3 is also a fixed tuned, wide band amplifier stage capable of supplying large signal levels linearly to its input.

(4) Capacitor C22 effectively matches the output impedance of preamplifier Q3 to the 75ohm input impedance of the 70-MHz IF filter.

(5) Potentiometers R22 and R23 provide proper metering of the crystal current in each of the diode in the mixer 2A4Z1.

f. 70-MHz IF Filter) 2A5. The 70-MHz IF filter 2A5 is a five-pole gaussian bandpass filter. For 12-channel operation, a filter with a bandwidth of 1.5 MHz is used and, for 24-channel operation, a filter with a 1.5-MHz bandwidth is used. The filter has a center frequency of 70 MHz and passes the 750-kHz or 1.5-MHz frequency band to IF amplifier 2A12. All other frequencies are inhibited. The 12-channel filter (750-kHz bandwidth) has an insertion loss of 5.5 db maximum. The 24-channel filter (1.5-MHz bandwidth) has an insertion loss of 7.5 db maximum.

1-86. Local Oscillator Circuits Block Diagram Description (fig. 8-52)

The channel A local oscillator circuits consist of 220 MHz vco 2A13, frequency mixer 2A6, and local oscillator filter 2F18. The channel B local oscillator circuits consist of 220 MHz vco 2A14, frequency mixer 2A9, and local oscillator filter 2F19. The local oscillator circuits which are common to both channels consist of frequency synthesizer 2A21, amplifier-multiplier 2A8, 1137 to 1213-MHz bandpass filter 2FL10, 1137 to 1213-MHz circulator 2HY3, and frequency multiplier group 2A7. The common local oscillator circuits are described first followed by a description of the local oscillator circuits which are provided separately for each channel.

a. Local Oscillator Circuits (Common to Both Channels). The local oscillator circuits (common to both channels) produce a 4550 to 4850-MHz output which is applied to channel A frequency mixer 2A6 and to channel B frequency mixer 2A9. The 4450 to 4850-MHz output is developed by multiplying the 284. 375 to 303.125-MHz output of frequency synthesizer 2A21 by sixteen. Frequency synthesizer 2A21 generates a highly stable frequency in the 284.375 to 303.125-MHz range which is adjustable in 6.250-kHz steps. Frequency synthesizer 2A21 is identical to frequency synthesizer 1A14 used in the transmitter. Refer to paragraph 1-27 for a block diagram description of the frequency synthesizer circuits. The 284.375 to 303.125-MHz output of frequency synthesizer 2A21 is applied to amplifier-multiplier 2A8.

(1) Amplifier-multiplier 2A8 is comprised of low level amplifier Q1, Q2 and 1st frequency multiplier (varactor diodes CR2 and CR3). The low level amplifier stage provides an 18-20 db gain and delivers 2 watts to drive the varactor diodes. The low level amplifier output is also applied through metering circuit (CR1) to the AMPL LEVEL test point (TP2) on the module front panel. The 1st frequency multiplier uses two varactor doubler circuits (CR2 and CR3) to accomplish a times 4 multiplication and maintain higher efficiency. The 1137.5 to 1212.5-MHz output of amplifier-multiplier 2A8 is at a power of 750 milliwatts (nominal) with spurious and related harmonic signals down 80 db. The 1137.5 to 212.5 MHz output is applied to 1137.5 to 1213-MHz bandpass filter 2 FL10.

(2) The 1137 to 1213-MHZ bandpass filter (2FL10) passes only the desired output frequency to 1137- to 1213-MHz circulator 2HY3. All other

frequencies are inhibited by 1137 to 1213-MHz bandpass filter 2FL10, thereby improving the spurious responses of the receiver. The 1137 to 1213-MHz circulator 2HY3 is used to isolate the output of 1137 to 1212-MHz bandpass filter 2FL10 from the input of frequency multiplier group 2A7. 1137.5 to 1213-MHz circulator 2HY3 also provides a detected sample of the 1137 to 1213-MHz signal to the meter selector switch on the receiver meter panel.

(3) Frequency multiplier group 2A7 is comprised of 2d frequency multiplier 2A7A1, 2275 to 2435-MHz circulator 2A7HY1, 3d frequency multiplier 2A7A2, and 4550 to 4850-MHz power divider 2A7HY2. The 2d frequency multiplier, 2A7A1, uses a tuned circuit, varactor diode doubler, and tuned cavity to multiply the frequency up to 2275 to 2425-MHz at 400 milliwatts (nominal). Circulator 2A7HY1 isolates 2d frequency multiplier 2A7A1 from 3d frequency multiplier 2A7A1 from 3d frequency multiplier 2A7A2 and also provides a detected sample of the 2d frequency multiplier's output signal (2275 to 2425 MHz) to the meter selector switch on the receive meter panel. The third frequency multiplier 2A7A2 uses a low pass filter, varactor diode doubler, and tuned cavity to multiply the frequency up to 4550 to 4850-MHz. The 4450 to 4859-MHz, 200 milliwatt output of the 3d frequency multiplier is applied to frequency mixers 2A6 and 2A9 through 4550 to 4850-MHz power divider 2HY2.

b. Channel A and Channel B Local Oscillator Circuits. Two identical 220 MHz vco's 2A13 and 2A14, two identical frequency mixers 2A6 and 2A9, and two identical local oscillator filters 2FL8 and 2FL2 are used in the dual diversity receiver as part of the local oscillator chain. Under normal operating conditions, both 220 MHz vco's are frequency synchronized (phase-locked) at a nominal frequency of 220 MHz. The output frequency of each 220 MHz vco is controlled by an apc signal (dc voltage) applied to its input from combiner 2A16. The apc signals compensate for phase and frequency differences between the IF signals of channel A and channel B. (Refer to the apc block diagram description, paragraph 1-91.) Since the channel A and channel B local oscillator circuits are identical, only the channel A circuits are described below.

(1) The 220 MHz vco 2A13 consists of 110 MHz vco 2A13Y1 and frequency multiplier 2A13A1. The 110 MHz vco is a sealed crystal oscillator which has a nominal frequency of 110 MHz. However, the actual output frequency depends upon the agc signal (dc voltage) applied to its input. from combiner 2A16. The direction and amount of frequency deviation around the nominal frequency is determined by the polarity and level of the apc signal. The FREQ. ADJ control allows the 10-MHz output to be corrected manually. The frequency controlled 110-MHz output is applied to frequency multiplier 2A13A1. The frequency multiplier consists of input amplifier Q1, frequency doubler Q2, Q3, and output amplifier Q4. The frequency doubler multiplies the frequency controlled 110-MHz signal up to 220 MHz. The input amplifier amplifies the low level signal from the 110 MHz vco and also provides isolation for the frequency doubler. The output amplifier amplifies the low level 220-MHz (frequency controlled) output of the frequency doubler for application to frequency mixer 2A6. The output amplifier also provides a 220-MHz signal (VCO-LOCK A), through an attenuator, to alarm monitor 2A20. The VCO LOCK (A) signal from 220 MHz vco 2A13 and the VCO LOCK (B) signal from 220 MHz vco 2A14 control the VCO LOCK indicator on the receiver meter panel. In addition, the 220-MHz output of amplifier Q4 is applied to a metering circuit where it is detected (mult osc metering signal) for application to the meter selector switch.

(2) Frequency mixer 2A6 consists of 220MHz bandpass filter 2A6FL1, crystal mixer 2A6Z1, and 4330to 5070-MHz circulator 2A6HY1. The 4500 to 4850-MHz signal from frequency multiplier group 2A7 is applied to one input of crystal mixer 2A6Z1. The frequency controlled 220-MHz signal from 220 MHz VCO 2A13 is applied to the other input of crystal mixer 2A6Z1. The two signals are mixed producing signals at the RF input frequency and frequencies which are ± 220 MHz from the RF input frequency. These signals are passed through 4330to 5070-MHz circulator 2A6HY1 to local oscillator filter 2FL8 where the correct frequency is selected. 4330to 5070-MHz circulator 2A6HY1 provides isolation between the crystal mixer 2A6Z1 and local oscillator filter 2FL8. The crystal current metering circuit provides proper metering for the crystal current in each of the diodes in the crystal mixer 2A6Z1. The metering circuit output is applied to the meter selector switch on the receiver meter panel.

(3) Local oscillator filter 2FL8 is a four-pole (4 cavity) RF bandpass filter. The local oscillator filter passes only the desired translated frequency

from frequency mixer 2A6. Each of the four tuning cavities is ganged to a single frequency adjust control dial with direct readout of the incoming RF frequency (frequency to which the receiver is set). However, the actual bandpass of the local oscillator filter is ± 70 MHz from the incoming RF frequency. (Refer to the receiver mixing process block diagram description given in paragraph 1-84.) The output of the local oscillator filters is applied to mixer preamplifier 2A4. In addition to passing the desired local oscillator signal (± 70 MHz from the incoming RF signal), the local oscillator filter 2FL8 inhibits all other signals resulting from the frequency mixing process in frequency mixer 2A6. The bandwidth of the local oscillator filter is nominally 25 MHz with a maximum insertion loss of 1.5 db. -

1-87. **IF Amplifiers 2A12 and 2A15 Block Diagram Description (fig. 8-53)**

Channel A and channel B IF amplifiers 2A12 and 2A15 are used to amplify the low level 70-MHz IF signals from 70-MHz IF filters 2A10. The amplifiers are identical except that the agc metering signal output from IF amplifier 2A15 is not used.
Each IF amplifier consists of four circuits: amplifier circuit, IF monitor circuit, agc circuit, and metering circuit.

a. Amplifier Circuit. The amplifier circuit is used to amplify the low level 70-MHz IF input signal from 70-MHz RF filter. The IF GAIN control is used in the input circuit of the amplifier stage, to set the 70-MHz IF gain of the IF amplifier. The 70-MHz IF signal is amplified by five cascaded amplifier stages Q1 through Q5 and attenuated by four diode attentuator circuits CR1 through CR4. The amplified 70-MHz IF signal from the fifth amplifier stage Q5 is then fed to buffer Q6. The overall gain of the five cascaded amplifier stages and four diode attenuator circuits is controlled by the age circuit. The buffer Q6 provides an impedance match between the output of the fifth amplifier stage Q5 and the input of the output amplifier Q7. The output amplifier Q7 provides a 70-MHz IF gain and is capable of delivering large linear signal levels to the output. The 70-MHz IF signal at the output of Q7 is applied to combiner 2A16. In addition to the 70-MHz IF signal is applied to the IF monitor circuit in IF amplifier 2A12.

b. IF Monitor Circuit. The IF monitor circuit detects the 70-MHz IF signal and applies a carrier (IF) out metering signal to the receiver meter selector switch for monitoring the output level of the 70-MHz IF signal. The IF monitor circuit also provides a age input signal to dc amplifier Q8 (part of age circuit), when the AGC SEL switch is in the DIV OFF position. The IF monitor circuit consists of peak diode detector CR5 and CR6 and voltage divider R32 and R37. The 70MHz IF signal is peak detected by the diode detector and a de voltage is developed across the voltage divider. The detected de voltage is applied to the age circuit through the AGC SEL switch.

c. AGC Circuit. The age circuit is used to control the overall gain of the amplifier circuit and to maintain each IF amplifier output at the same IF level ratio as at the IF amplifier input. (Refer to paragraph 1-90 for a detailed description. of the age function.) The age circuit consists of the AGC SEL switch, de amplifier Q8 and Q9, and emitter follower Q10. The AGC SEL switch is used to select the age mode and connects the proper inputs to the age circuit. When the AGC SEL switch is in the TEST position, the age circuit is disabled and maximum IF gain is obtained. In the DIV OFF position, the de output of the IF monitor circuit is applied to de amplifier Q8 and Q9. In the DIV ON position, the de amplifier is connected to an external detector in combiner 2A16 and the age circuits are cross-connected to the age circuits in IF amplifier 2A15. The dc amplifier Q8 and Q9 is used to amplify the dc voltage at its input to increase the gain of the age circuit. An age gain potentiometer is used in the output of the de amplifier to set the de gain of the age circuit. The output of the de amplifier is applied to emitter follower Q10. The output of the emitter follower is a de voltage which is inversely proportional to the age input to the de amplifier Q8 and Q9. The age input de voltage increases as the 70-MHz IF signal increases. This causes the age de output to decrease proportionally increasing the attenuation of the diode attenuator circuits CR1 through CR4 and decreasing the overall IF gain of the amplifier circuit. The age output is applied to each of four diode attenuator circuits. To illustrate, as the 70-MHz IF signal level increases, the age output decreases and the 70-MHz IF signal attenuation increases. This reduces the output level of the 70-MHz IF signal to the desired level. The age output of emitter follower Q10 is also applied to the metering circuit.

d. Metering Circuit. The metering circuit provides age signal level outputs to the meter selector

switch on the receiver meter panel and the antenna alignment indicator. Note that the age signal level output (age meter) is not used in IF amplifier 2A15. The metering circuit consists of voltage divider R43, R51, R52 and meter adjust circuit R46 through R48. The agc signal level outputs (age metering and ant. alignment indication) are developed across the voltage divider R43, R51 and R52. The reference (return lines) for the age signal level outputs are applied through meter adjust circuit R46-R48. The METER ZERO control is used to set the meter on the receiver meter panel to zero. To zero adjust the meter, the AGC SEL switch on IF amplifier 2A12 must be set to the TEST position.

1-88. Combiner 2A16 Block Diagram Description (fig. 8-54)

a. Combiner 1A16 receives the channel A and channel B if signals from IF amplifiers 2A12 and 2A15. Combiner 2A16 consists of two identical IF signal amplifier circuits, two identical squelch circuits, two identical ape circuits, an age circuit, and two identical channel A and channel B carrier IF alarm circuits. The squelch circuits monitor the two IF signals and control the output of each IF signal amplifier circuit. When the two IF signals are within a predetermined level ratio (approx. 8 db) with respect to one another, the squelch circuits enable the IF signal amplifier circuits for both channels and the two IF signals are amplified, combined, and sent to demodulator 2A17. When the ratio of the two IF signals exceeds 8 db, the squelch circuits inhibit the IF signal amplifier circuit of the weaker channel and only the stronger IF signal is amplified and sent to demodulator 2A17. The ape circuits monitor the phase and frequency of the channel A and channel B IF signals and phase-lock the two IF signals, when they are not in phase, by providing a APC-A and APC-B dc control voltage to the frequency of 220 MHz vco 2A13 and 2A14. The age circuit monitors the combined or selected IF signal and provides a agc-A and agc-B dc voltage proportional to the detected IF signal which controls the gain of each IF amplifier 2A12 and 2A15. The channel A carrier IF alarm circuit monitors the channel A IF signal and provides a channel A carrier IF alarm output to alarm monitor 2A20 when the channel A IF signal is 8 db below the channel B IF signal level. Similarly, the channel B carrier IF alarm circuit monitors the channel B IF signal and provides a channel B carrier IF alarm output when the channel B IF signal is 8 db below the channel A IF signal level.

b. The following description of combiner 2A16 is based on the circuits shown in figure 8-54.

(1) The squelch circuits in combiner 2A16 consist of channel A squelch detect circuit, channel B squelch detect circuit, and a balanced differential comparator. The channel A and channel B squelch detect circuits monitor the level of the IF signals in each receiver channel. The squelch detect circuits provide a positive or negative dc squelch voltage, depending on which IF signal (channel A or B) is greater, to the A and B inputs of the balanced differential comparator. In the balanced state, the differential comparator maintains a forward bias on each of the squelch diodes CR1 and CR11 located in the CHAN A and CHAN B IF signal amplifier circuits. The differential comparator becomes unbalanced when either the channel A or B squelch inputs exceed a predetermined positive voltage. A third de voltage, derived from the age, which represents the sum of the channel A and B IF signals, is applied to the C input of the balanced differential comparator. This dc voltage maintains the differential comparator output squelch voltages at their appropriate levels. When both channel A and B IF signals fall below a predetermined level, the C input to the differential comparator decreases and generates a channel A and B carrier alarm. The differential comparator remains in the balanced state and the IF signals are not squelched. When the channel A IF signal level exceeds the channel B IF signal level by 8 db or more, the channel A squelch detect de output voltage is positive and of sufficient magnitude to unbalance the differential comparator. This unbalance produces a back bias on the squelch diode in channel B IF signal amplifier circuit, causing the channel B IF signal to be squelched. The squelch diode in the channel A IF signal amplifier circuit remains forward biased. Therefore, a strong channel A IF signal causes the weaker channel B IF signal to be squelched. Similarly, when the channel B IF signal level exceeds the channel A IF signal level by 8 db or more, the channel B squelch detect circuit produces a positive de voltage that unbalances the differential comparator, causing the channel A IF signal to be squelched.

(2) The apc circuits in combiner 2A16 consist of the channel A ape circuit and the channel B ape circuit. The channel A ape circuit compares the phase of the channel A IF signal with the phase of the combined IF signal, and

similarly the channel B apc circuit compares the phase of the channel B IF signal with the phase of the combined IF signal. When the two IF signals are not in phase, the channel A apc circuit produces a dc voltage (APC-A) that causes the frequency of 220 MHz vco 2A13 to change in one direction, while the channel B apc circuit produces a dc voltage APC-B that causes the frequency of 220 MHz vco 2A14 to change in the opposite direction. Changing the frequency of 220 MHz vco 2A13 and 2A14, in this manner, compensates for the phase difference in the two IF signals. Refer to the receiver apc circuits block diagram description given in paragraph 1-91.

(3) The agc circuit in combiner 2A16 consists of a detector, dc emitter follower, and dc amplifier. The agc circuit produces a dc voltage (AGC-A and AGC-B) that controls the gain of IF amplifiers 2A12 and 2A15, as described in the receiver agc block diagram description (para 1-90). The agc circuit in combiner 2A16 also provides a dc voltage to the C input of the differential comparator as described in (1) above, and a dc voltage (agc-pcm) to digital data modem 1A12 in the transmitter. Each dc voltage is proportional to the combined IF signal level, but tends to remain constant when the receiver inputs are above a predetermined value called radio threshold. When the receiver input signals are below radio threshold, each dc voltage tends to change. One agc output (AGC-A and AGC-B) is the sum of the dc voltage developed in the detector and that supplied by the AUTO-AGC potentiometer. Hence, the AUTO-AGC potentiometer controls the combined IF signal level. The ALARM potentiometer controls the dc voltage fed to input C of the differential comparator, which in turn controls the dc voltage (AGC-PCM) that is supplied to digital data modem 1A12. The MAN-AGC ADJ potentiometer is used during receiver age gain alignment. The output of the voltage divider R60 and R61 is proportional to the combined IF signal and is fed to the receiver meter selector switch.

(4) The channel A carrier IF alarm circuit in combiner 2A16 consists of an amplifier, a time-delay network, and an emitter follower. The channel A carrier IF alarm circuit monitors the channel A IF signal and provides a channel A carrier IF alarm signal to alarm monitor 2A20 when the channel A IF signal is below a predetermined reference level for approximately 5 seconds.

(5) The channel B carrier IF alarm circuit in combiner 2A16 is identical to the channel A carrier IF alarm circuit and provides a channel B carrier IF alarm signal to alarm monitor 2A20 when the channel B IF signal is below the predetermined reference level for approximately 5 seconds.

1-89. Demodulator and Amplifier Circuits Block Diagram Description
(fig. 8-55)

The demodulator and amplifier circuits consist of demodulator 2A17, low pass filter 2A18 and AF-RF amplifier 2A19.

a. Demodulator 2A17. Demodulator 2A17 receives the combined or selected 70-MHz IF input signal from combiner 2A16 and converts the frequency deviations in the 70-MHz IF signal into the pcm/order wire signal. The demodulation consists of input amplifier Q1, limiter stages Q2 through Q5, discriminator driver Q6, Q7, frequency discriminator T1, CR3, CR4, and video output amplifier Q8, Q9.

(1) The 70-MHz IF signal from combiner 2A16 is applied through input amplifier Q1 to the first limiter stage Q2. The input amplifier Q1 matches the input impedance of the first limiter stage with the output impedance of. combiner 2A16.

(2) Four limiter stages Q2 through Q4 are provided to remove amplitude variations in the 70-MHz signal. Each limiter stage is operated as an overdriven common base amplifier to clip the positive and negative peaks of the 70-MHz IF signal. A LIM TUNING control is provided for tuning each limiter stage. The output of the fourth limiter stage is applied to discriminator driver Q6, Q7.

(3) The discriminator driver consists of emitter follower Q6 and common base amplifier Q7. The emitter follower Q6 is used to match the output impedance of the fourth limiter stage to the input impedance of the common base amplifier Q7. The output of the discriminator driver is applied to frequency discriminator T1, CR3, CR4.

(4) The frequency discriminator detects the frequency variations into the pcm/order wire signal. The DISCR PRIM control is used to tune the primary winding of the frequency discriminator transformer T1. The DISCR SEC control in nator transformer T1 is used to set the discriminator transformer T1 is used to set the discriminator crossover frequency. The pcm/order wire output is applied to low pass filter 2A18 through: video output amplifier stage Q8, Q9. The video output amplifier stage amplifies the signals and

isolates the frequency discriminator T1, CR3, CR4 from low pass filter 2A18.

b. 260-KHz Low Pass Filter 2A18. The 260 KHz low pass filter 2A18 is used during 12 channel operation and replaced with a 680-KHz low pass filter 2A27 during 24-channel operation. During 12 channel operation the 260-KHz low pass filter 2A18 allows passage of all frequencies below 260 KHz and applies them to the AF-RF amplifier 2A19. During 24-channel operation the 680 KHz low pass filter 2A27 allows passage of all frequencies below 680 KHz and applies them to the AF-RF amplifier 2A19.

c. AF-RF Amplifier 2A19. The AF-RF amplifier consists of two video amplifier stages Q1, Q2 and an emitter follower Q3. The pcm/order wire signal from 2A18 is applied to the first and second video amplifier stages Q1, Q2, through the TRAFFIC LEVEL ADJ control. The output of the AF-RF amplifier is adjusted to 1.0 volt peak-to-peak by the TRAFFIC LEV ADJ control. The pcm/order wire signal is amplified by the first and second video amplifier stages Q1, Q2 and applied to the output through emitter follower Q3. The emitter follower Q3 provides an impedance match between second video amplifier stage Q2 and the output. Emitter follower Q3 also provides negative feedback to first video amplifier Q1. The amount of negative feedback determines the overall gain and bandwidth of the AF-RF amplifier 2A19. The output of the AF-RF amplifier 2A19 is applied to digital data modem 1A12 in the transmitter as a traffic output signal and to alarm monitor 2A20 as a traffic monitor signal which is used to monitor the level of the traffic output of the receiver.

1-90. Receiver AGC Block Diagram Description (fig. 8-56)

a. The receiver agc circuits control receiver gain by monitoring the level of the channel A and channel B IF signals and varying the gain of IF amplifiers 2A12 and 2A15. When the detected IF signal is above a predetermined reference level (receiver threshold), the receiver agc circuits reduce the overall gain of IF amplifiers 2A12 and 2A15. When the channel A and/or channel B IF signal is below the predetermined reference level, the receiver agc circuits do not effectively reduce the gain of IF amplifiers 2A12 and 2A15. The receiver agc circuits provide three modes of operation; diversity off (DIV OFF), diversity on (DIV ON), and test (TEST). Manual controls are provided in the IF amplifiers to permit selection of the agc mode desired.

b. The receiver age circuits are contained in IF amplifier 2A12, IF amplifier 2A15, and combiner 2A16. The position of the AGC SEL switches on IF amplifiers 2A12 and 2A15 determine the receiver agc modes which are described below. The comber agc circuit also provides a dc voltage (AGC-PCM) to digital data modem 1A12 in the transmitter cabinet, which is described in the combiner 2A16 block diagram description of paragraph 1-88.

(1) When the AGC SEL switches on IF amplifiers 2A12 and 2A15 are in the DIV OFF position, the agc circuit in combiner 2A16 is bypassed and the agc circuits in IF amplifiers 2A12 and 2A15 operate independently. Because the age circuit in each IF amplifier is identical, only the agc circuit for the channel A IF signal is discussed. The channel A IF signal is monitored by the agc circuit in IF amplifier 2A12. When the channel A IF signal is above a predetermined reference level, the agc circuit detects the IF signal level and increases the attenuation of the diode attenuator circuits (CR1-CR4) by a proportionate amount. This is accomplished using a detector CR5, CR6 and a dc amplifier Q8, Q9 to produce a dc voltage which is inversely proportional to the amount the detected IF signal is above the predetermined reference level. The dc voltage is applied to a dc emitter follower Q10, which provides a negative feedback to the diode attenuator circuits CR1 through CR4 to reduce the gain of the IF signal.

(2) When the AGC SEL switches on IF amplifiers 2A12 and 2A15 are in the DIV ON position and the AUTO/MAN AGC switch on combiner 2A16 is in the MAN position, the AGC circuits in IF amplifiers 2A12 and 2A15 are cross-connected and the MAN AGC ADJ potentiometer in combiner 2A16 controls their operation. The position of the MAN AGC ADJ potentiometer control determines the level of dc voltage applied to the agc circuits in IF amplifiers 2A12 and 2A15, and therefore determines the gain of IF amplifiers 2A12 and 2A15.

(3) When the AGC SEL switches on IF amplifiers 2A12 and 2A15 are in the DIV ON position and the AG AUTO/MAN switch on combiner 2A16 is in the AUTO position, the age circuits in IF amplifiers 2A12 and 2A15 are cross-connected and the age circuit in combiner 2A16 controls their operation. The combined IF

signal in combiner 2A16 is detected by CR12, added to a dc bias set by the AUTO AGC ADJ potentiometer, and applied to the IF amplifier agc circuits through an emitter follower Q13. The level of the dc voltage from the emitter follower is Q13 proportional to the level of the detected IF signal plus the bias level set by the AUTO AGC ADJ potentiometer. Therefore, the amount of negative feedback applied to the diode attenuator circuits CR1 through CR4 in each of the IF amplifiers 2A12 and 2A115 is proportional to the level of the detected combined IF signal. The greater the IF amplifier input, the greater will be the detected combined IF signal. A larger detected IF signal will reduce the dc voltage applied to the diode attenuator circuits CR1 through CR4 increasing the negative feedback, thus increasing the attenuation and reducing the IF signal level.

(4) When the AGC SEL switches on IF amplifiers 2A12 and 2A15 are in the TEST position, the age circuits in IF amplifiers 2A12 and 2A15, and combiner 2A16 are bypassed and the IF gain of both IF amplifiers are at a maximum.

1-91. Receiver APC Block Diagram Description
(fig. 8-57)

a. The receiver ape circuit phase locks the channel A IF signal with the channel B IF signal in order to achieve the signal-to-noise improvements resulting from diversity combining. The relative phase of the two IF signals vary randomly as their respective carrier signals fluctuate (in amplitude and phase) due to the different tropospheric paths they travel. The receiver apc circuit detects the instantaneous phase differences in the two IF signals plus any frequency difference in the 220 MHz vco's 2A13 and 2A14 and compensates for any difference to maintain the two IF signals in a phase-locked condition.

b. The channel A apc loop consists of the channel A ape circuit in combiner 2A16 and 220 MHz vco 2A13. The channel A apc circuit in combiner 2A16 monitors the channel A IF signal and the combined IF signal. When the two IF signals are not in phase, the channel A apc circuit detects the instantaneous phase difference between the two IF signals. A dc control voltage (APC-A), developed by the instantaneous phase difference, is fed back to the voltage controlled oscillator 2A13Y1 in 220 MHz vco 2A13. This dc control voltage causes the 220-MHz frequency of 220 MHz vco 2A13 to change. The 220-MHz frequency change is transferred to a 70-MHz IF frequency change in channel A by frequency mixer 2A6, and mixer preamplifier 2A. The 70-MHz IF frequency change compensates for the instantaneous phase difference originally producing the change. The ape phase loop continually tracks and corrects for phase differences in the channel A and B IF signals, thus maintaining the channel A IF signal phase-locked to the channel B IF signal.

c. The channel B ape loop is identical to the channel A ape loop except for its signal path and xodule reference designations. The channel B ape circuit maintains the channel B IF signal phaselocked to the channel A IF signal.

1-92. Alarm Monitor 2A20 Block Diagram Description
(fig. 858)

a. Alarm monitor 2A20 receives monitor signals (traffic monitor, Channel A and B IF alarm, vco A and B, and synthesizer monitor) and controls associated alarm indicators on the receiver meter panel. Depending upon the signal level received, the associated indicator lights either green (normal indication) or red (alarm indication). The alarm monitor also contains a summary alarm circuit which is enabled when any one of the alarm conditions occur. The traffic monitor signal is received from AF-RF amplifier 2A19 and indicates the pcm and order wire signal level at the output of the receiver. Channel A and B carrier IF alarm and signals are received from combiner 2A16 and indicate the condition of the channel A and the channel B 70-MHz IF carrier signals. The vco A and B signals are received from oscillator-multipliers 2A13 and 2A14 respectively and indicate if the 220-MHz signals from frequency multipliers 2A13A1 and 2A14A1 are frequency locked. The synthesizer monitor alarm signal is received directly from frequency synthesizer 2A21 and indicates if the signals from variable frequency divider No. 2 2A21A5 and standard RF oscillator 2A21A7 are phase locked.

b. An identical alarm monitor module 1A5 is used in the transmitter, however, the jumper connections on the associated plate assembly connectors for each module (2A20 or 1A5) are different. The transmitter alarm monitor module is described in paragraph 1-34.

c. The TRAF, SYNTH LOCK, CARR (IF) A, CARR (IF) B, and VCO LOCK indicators on the receiver meter panel are controlled by Schmitt trigger circuits in alarm monitor 2A20. Each Schmitt trigger circuit causes an associated indicator

to light green (normal indication) or red (alarm indication). The input signals to the alarm monitor control the operation of an associated Schmitt trigger circuit.

(1) The traffic monitor signal is derived from AF-RF amplifier 2A19 and is applied to operational amplifier (integrated circuit) AR1 through a precision attenuator circuit. The operational amplifier output is detected by detector CR1 and CR2 and applied to the traffic meter through a potentiometer and to Schmitt trigger circuit Q5, Q6 through the emitter follower Q1. If the traffic monitor signal exceeds a predetermined level, the dc voltage developed by detector CR1, CR2 will cause transistor Q5 of the Schmitt trigger to turn on and transistor Q6 to turn off thus allowing amplifier Q7 to turn on. With Q7 turned on, a low impedance path to ground is provided for the normal traffic indicator lamp, and the TRAF indicator lights green. Since Q6 is turned off, a high impedance path to ground is provided for the alarm traffic indicator lamp causing the indicator lamp (red) to remain off. When the traffic monitor signal falls below the predetermined voltage, the dc voltage applied to the base of Q5 is not sufficient to keep Q5 conducting. With Q5 turned off, Q6 turns on and Q7 turns off. For this condition, a high impedance path to ground is applied to the normal traffic indicator lamp (TRAF) and a low impedance path to ground is applied to the alarm traffic indicator lamp. Consequently, the TRAF indication changes from green to red. Also with Q7 turned off, the Q7 output dc voltage is high enabling the OR gate which causes Q23 to turn on. With Q23 turned on, a receiver summary alarm indication is provided to the transmitter.

(2) Channel A and B carrier IF alarm signals are derived from the Channel A and B carrier IF alarm circuits in combiner 2A16. The synthesizer monitor signal is derived from frequency synthesizer 2A21. These monitor signals (de levels) are applied directly to the associated Schmitt trigger circuit Q14, Q15. Circuit operation is identical to that described above for the traffic monitor circuit. If the monitor signal exceeds a predetermined dc level, the associated indicator lights (SYNTH LOCK) green (normal indication). If the input is below the predetermined level, the associated indicator lights red (alarm indication) and, in addition, the summary alarm circuit is enabled.

(3) The 220-MHz vco-A and vco-B monitor signals are received from 220-MHz vco modules 2A13 and 2A14 respectively. If the vco-A and vco-B 220-MHz signals are at the same frequency, the receiver is in a phase-lock condition (difference frequency is zero). For the phase-lock condition, the mixer CR3, CR4 generates a de voltage which is blocked by dc blocking capacitor C9. When the receiver is out of phase-lock, a difference frequency exists. For the out-of-phase condition, the difference frequency (mixer output) is passed by dc blocking capacitor C9 and amplified by AR2. The amplified signal then is applied to detector CR9, CR10 and high pass filter C17, R39.

(a) The output of the high pass filter C17, R39 is applied to detector CR7, CR8 where the difference frequency is detected. The detected dc is applied to the meter on the receiver front panel when the meter selector switch is placed in the VCO FREQ DIFF position. As the difference frequency increases, the output of the high pass filter C17, R39 increases causing the VCO FREQ DIFF meter reading to increase.

(b) The dc output of detector CR9, CR10 is passed through emitter follower Q2 to time-delay circuit C21, R43. The time-delay circuit delays the application of dc voltage to Schmitt trigger Q8, Q9. The out of phase lock or difference frequency condition must exist for a minimum of 4 seconds before the delayed dc voltage at the base of Q8 increases to a level sufficient to turn Q8 on. Thus, momentary out of phase-lock conditions (for example, signal fading) will not produce an alarm condition. The operation of Schmitt trigger Q8, Q9 is similar to that previously described for monitor circuits except the alarm and normal outputs are reversed. The outputs of Schmitt trigger Q8, Q9 are reversed because it is the presence rather than the absence of a dc voltage at the Schmitt trigger input that results in an alarm condition.

(4) The summary alarm circuit is comprised of diode OR gate (CR12, CR13, CR15-CR17) and transistor Q23. Each of the normal outputs is connected to the OR gate. For normal operation, transistor Q23 is off (nonconducting). When any one of the alarm conditions occur, the OR gate switches Q23 on (conducting state) causing a receiver summary alarm condition.

1-93. Frequency Synthesizer 2A21 Block Diagram Description

Frequency Synthesizer 2A21 is identical to frequency synthesizer 1A14 used in the transmitter. Refer to paragraphs 1-27 through 1-33 for the block diagram description of the frequency synthesizer.

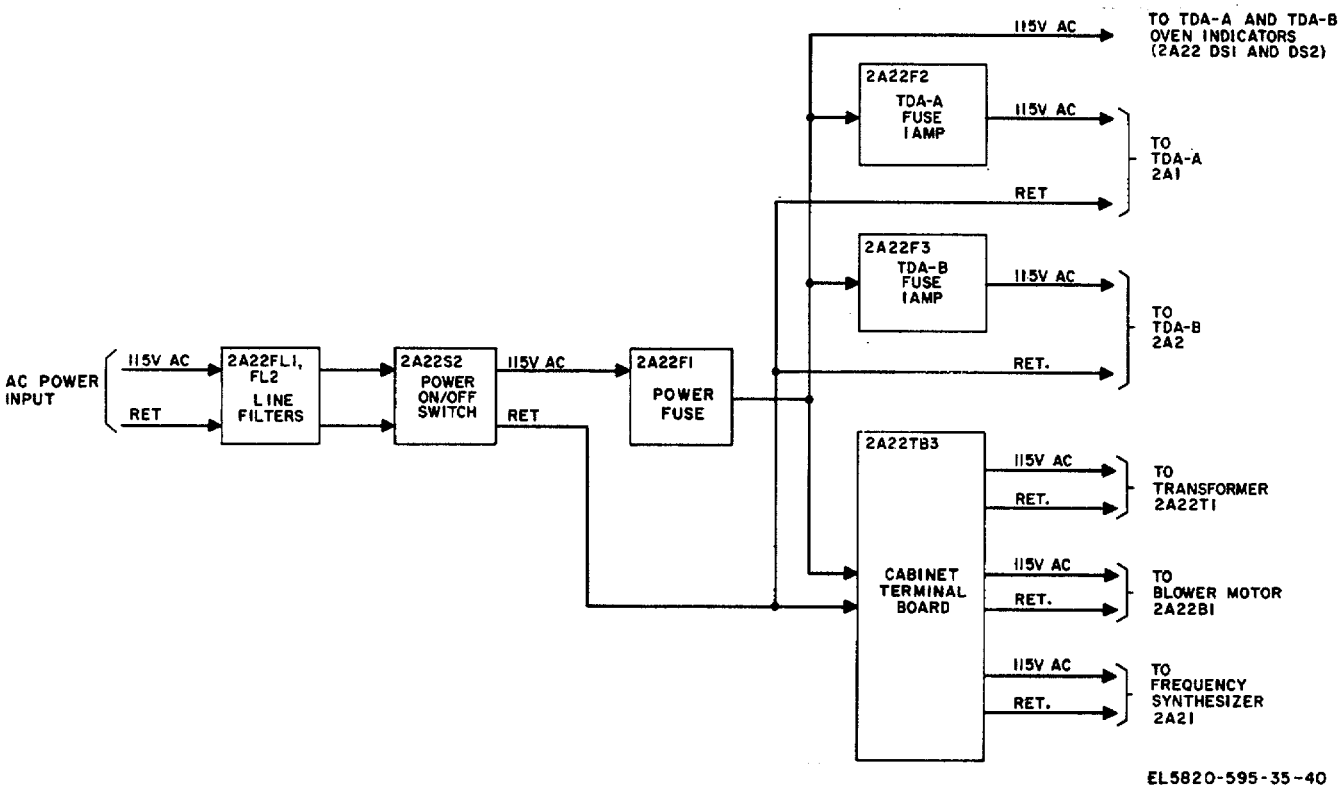


Figure 1-37. Receiver primary power distribution.

1-94. Primary Power Distribution
(fig. 1-37)

The 115 vac primary power is applied to the receiver through AC POWER INPUT connector 2A22J5. The 115 vac input passes through line filters 2A22FL1 and FL2 to POWER ON-OFF switch 2A22S2 on the receiver meter panel. When the POWER ON-OFF switch is set to the ON position, 115 vac passes through the 8 AMPS POWER fuse 2A22F1 and is distributed to transformer 2A22T1, TDS-A2a1, TDA-B2A2, cabinet blower motor 2A22B1, and frequency synthesizer 2A21.115 vac is also applied to the TDA-A and B indicators to provide the "press-to-test" function. Refer to the receiver interconnecting diagram (fig. 8-59) for detailed primary power connections.

1-95. Dc Power Distribution
(fig. 1-38)

The 115 vac input applied from terminal board 2A22TB3 to transformer 2A22T1 is transformed into four ac outputs (29 vac (w), 19 vac (x), 18 vac (y), and 30 vac (z)). Each output is applied to a voltage regulator in power supply 2A3. Four 15/28v regulators and one 12v regulator are utilized in power supply 2A3. A typical regulator is described in paragraph 1-38. The voltage regulators provide four regulated dc voltage outputs +28 vdc (w), +28 vdc (z), +15 vdc (x), -12 vdc (y) and four associated dc returns. The voltages are distributed to the modules in the receiver cabinet through plate assembly terminal board 2A24TB1 and cabinet terminal board 2A22TB2. The +28 vdc (w), 15 vdc (x), and -12 vdc (y) are supply voltages for the modules. The 28 vdc (z) output is used in oven control and alarm functions. Refer to the receiver interconnecting diagram (fig. 8-59) and power supply 2A3 interconnecting diagram (fig. W8-0) for detailed dc voltage connections.

1-96. Receiver Module Circuit Theory

The receiver module circuit theory descriptions are provided in paragraphs 1-97 through 1-112. Module circuit theory descriptions appear in sequential reference designation order and are given at the schematic diagram level. References to circuits previously described in the transmitter section (sec. III) are made where applicable (i.e. the receiver frequency synthesizer 2A21 is identical to the transmitter frequency synthesizer 1A14). Circuit theory descriptions and circuit diagrams

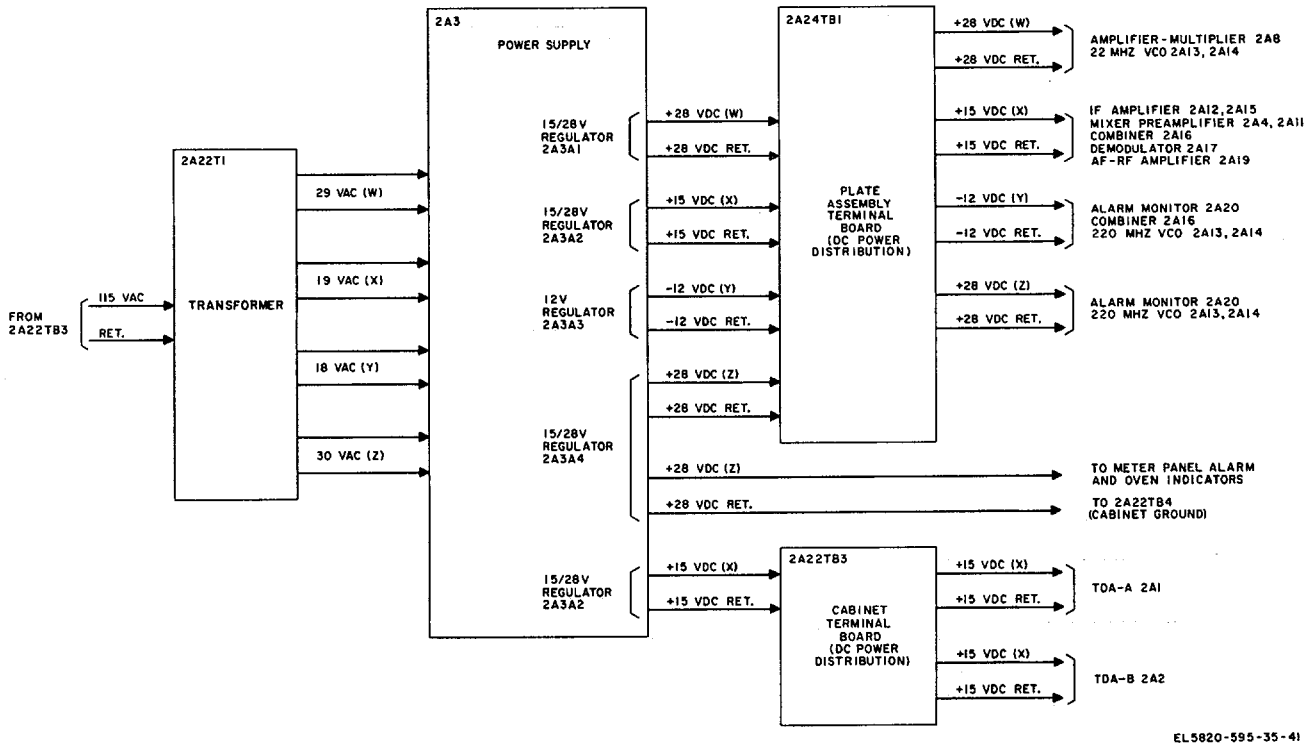


Figure 1-38. Receiver dc power distribution.

are not provided for the receiver nonrepairable modules (i.e. TDA's 2A1/2A2, preselectors 2FL4/2FL5, etc.). Theory coverage for the nonrepairable modules is limited to the block diagram descriptions. All module interconnections are shown in the receiver interconnecting diagram (fig. 8-59).

1-97. Power Supply 2A3 Circuit Theory

Power supply 2A3 contains the voltage regulator modules (2A3A1 through 2A3A4) which provide the dc supply and control voltages for the receiver. The power supply chassis 2A3A5 provides the following: a connector for each regulator module; an ac fuse at the input of each regulator module; and a failure lamp and a test point at the output of each regulator module. The interconnecting diagram for power supply 2A3 is shown in figure 8-60.

1-98. 15/28V Regulator (2A3A1, 2A3A2, and 2A3A4) Circuit Theory
(fig. 1-20)

The 15/28V regulators used in the receiver are identical to those used in the transmitter. Refer to the circuit theory description provided in paragraph 1-43 for 15/28V regulators 1A1A10 through 1A1A12.

1-99. 12V Regulator 2A3A3 Circuit Theory
(fig. 1-19)

The 12V regulator used in the receiver is identical to the 12V regulators used in the transmitter. Refer to the circuit theory description provided in paragraph 1-42 for 12V regulators 1A1A6 through 1A1A9.

1-100. Mixer Preamplifier 2A4/2A11 Circuit Theory
(fig. 1-39)

Mixer preamplifiers 2A4 and 2A11 are identical except for their signal paths. Each mixer preamplifier mixes the carrier signal with the local oscillator signal for their respective channel. The difference frequency produced (IF frequency) is amplified and applied to the appropriated 70-MHz IF filter 2A5 or 2A10. The mixer preamplifier consists of mixer Z1, and preamplifier stages Q1 through Q3. The B+ supply (+15 vdc) is provided from P1-3. Ac filtering of the B+ is provided by decoupling capacitors C5, C10, C14, and C20. Inductors L5, L8, and L10 block ac fluctuations from the B+ input. Test point TP2 15v can be connected to the receiver meter with a test lead to monitor the B+ voltage. Resistor R21 is a metering resistor.

a. Crystal Mixer Z1. The carrier signal is applied to input jack J1 (J1 RF IN) and the local oscillator signal is applied to input jack J2 (J2 LO IN). Crystal mixer Z1 consists of a matched pair of IN23 crystal diodes CR1 and CR2 which mix the carrier signal with the local oscillator signal via coupling capacitors C2 and C3. Mixing the two signals produces numerous frequencies, of which, the four predominant frequencies are-the original carrier frequency, the original local oscillator frequency, the sum of the frequencies, and the difference between the two frequencies, 70 MHz. Only the difference frequency, 70 MHz produced by mixing the two signals is applied to the input circuit for first IF amplifier Q1. All other frequencies produced by the mixing process are RF bypassed to ground in mixer Z1. Additional outputs are provided which permit monitoring the dc current -through crystal diodes CR1 and CR2 with the receiver meter. A positive de voltage is developed across resistor R1 which is proportional to the dc current through crystal diode CR1. This positive dc voltage is sent to the receiver meter selector switch via pin 8 of plug P1. Similarly, a negative dc voltage is developed across resistor R2 which is proportional to the dc current through crystal diode CR2. This negative dc voltage is also sent to the receiver meter selector switch via pin 9 of plug P1. Inductors L1 and L2 are used to block the ac signal from the diode monitoring circuits, and capacitors C1 and C4 provide filtering. A filter in each circuit (C6, L4, C9, and C8, L6, C13) provides additional filtering of the ac signal. Resistors R3, R23, and R4, R22 are metering resistors. Resistors R22 and R23 are variable and are used to adjust meter deflection.

b. First Preamplifier. The input circuit for first preamplifier Q1 is a parallel resonant circuit. Therefore, the resonant frequency and bandwidth of the parallel resonant circuit determines the band of frequencies coupled to the base of first preamplifier Q1. The parallel resonant circuit is formed by L3, C7, the base-emitter capacitance of transistor Q1, and capacitor C12. Its resonant frequency is set at 70 MHz by adjusting IF ADJ control L3. Q1 amplifies the 70-MHz IF signal passed by the input circuit, and the amplifier 70MHz IF signal is coupled through capacitor C11 to the base of the second preamplifier Q2. Resistors

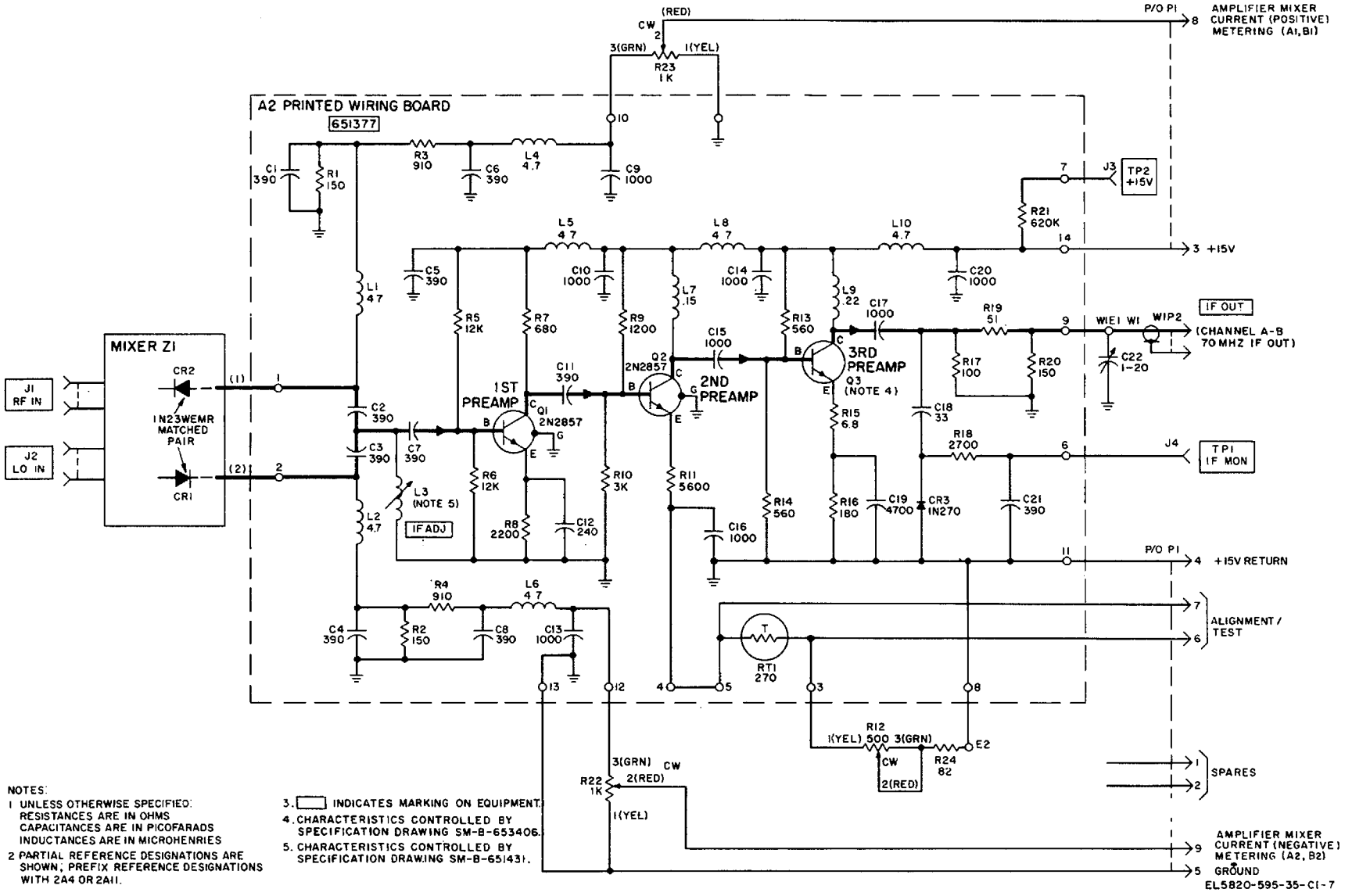


Figure 1-39. Mixer preamplifier 2A4/2A11, schematic diagram.

R5 and R6 provide fixed dc bias for Q2, and resistor R7 is its collector load. Emitter resistor R8 provides negative dc feedback to temperature stabilize first preamplifier Q1, and capacitor C12 provides the ac bypass.

c. Second Preamplifier. Second preamplifier Q2 also amplifies the 70-MHz IF signal, and the output is coupled through capacitor (C15) to the base of third preamplifier Q3. Resistors R9 and R10 provide fixed dc bias for this stage, and inductor L7 is its collector load. Resistor R11, thermistor RT1, and potentiometer R12 provide negative dc feedback to stabilize second preamplifier Q2, and capacitor C16 is the ac bypass. Thermistor RT1 also provides temperature compensation for the gain of this stage over a wide temperature range. Potentiometer R12 sets the operating point of second preamplified stage Q2, and therefore, sets the gain of the second preamplifier stage Q2.

d. Third Preamplifier. Third preamplifier Q3 also amplifies the 70-MHz IF signal. Its output is coupled through capacitor C17 to a 70-MHz IF filter 2A5 or 2A10 through IF OUT COAXIAL CABLE 2A4W1P2. Resistors R17, R19, R20, and capacitor C22, form an impedance matching network to provide a 75-ohm output impedance. Capacitor C22 is variable in this network to permit matching the load. Resistors R13 and R14 provide fixed dc bias for third preamplifier Q3, and inductor L9 is its collector load. Emitter resistors R15 and R16 provide negative dc feedback to temperature stabilize this stage, and capacitor D19 is the ac bypass. The 70-MHz IF signal out of third preamplifier Q3 is also coupled through capacitor C18 to a diode detector formed by CR3, R18, and C21. This provides a positive dc voltage which is proportional to the level of the detected IF signal at jack J4 (TP1 IF MON). Test point TP1 IF MON can be connected to the receiver meter with a test lead.

1-101. 70-MHz IF Filter 2A5/2A10 (12 and 24 Channel) Circuit Theory
(fig. 1-40)

a. The receiver contains two 70-MHz IF filters 2A5 and 2A10 which are incorporated in the receive signal path to restrict the receive bandpass and reject the undersize signals. The 70-MHz IF filter 2A5 provides a 750-KHz, 3 db bandwidth and is used when generating at 12-channel capacity. The 70-MHz IF filter 2A10 provides a 1.5-MHz, 3 db bandwidth and is used during 24channel operation.

b. Both 70-MHz IF filters 2A5, 2A10 are five-pole configurations and approximate a Gaussian shape. The 12-channel IF filter (2A5) is shown in the upper half of figure 1-40. Its insertion loss is 5.5 db maximum at the filter center frequency of 70 MHz. Input and output impedances are 75 ohms. The 24-channel IF filter (2A10) is shown in the bottom half of figure 1-40. Insertion loss of this filter is 7.5 db maximum at 70 MHz; input and output impedances are 75 ohms. The attenuating pad formed by resistors R1, R2, and R3 is added in the 24-channel filter (2A10) to compensate for the added noise bandwidth and to provide equal noise inputs to 'the IF amplifier for either 12 or 24-channel operation.

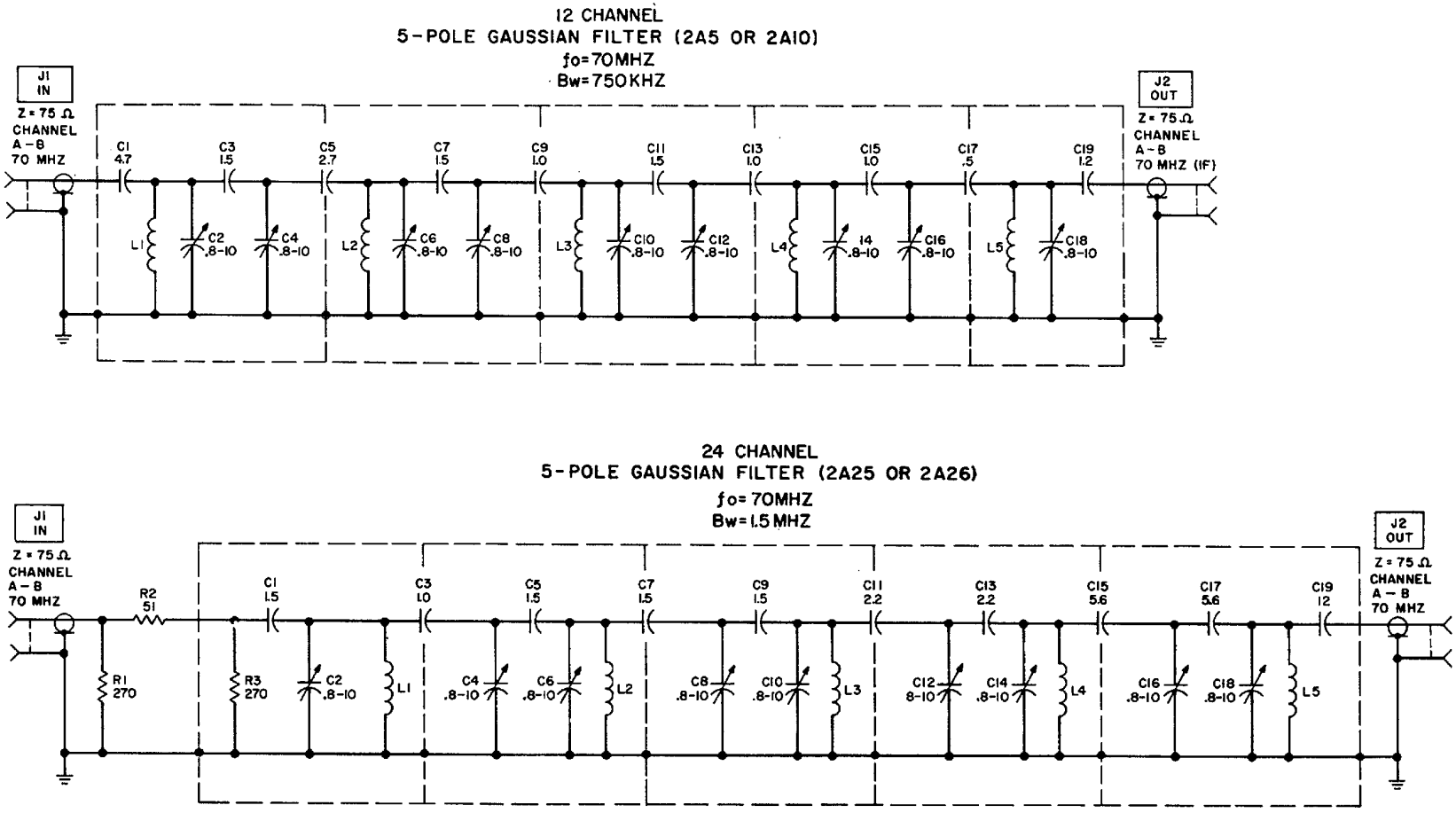
1-102. Frequency Mixer 2A6/2A9 Circuit Theory
(fig. 8-61)

a. The frequency mixer is used to mix the RF signal from the RF synthesizer-frequency multiplier chain with a 220-MHz fixed frequency to derive sidebands which are selected and used for the receiver local oscillator signal. The mixer consists of 220-MHz bandpass filter FL1, crystal mixer Z1 and 4330-to 5070-MHz circulator HY1. A filter network is provided for crystal current metering.

b. The 220-MHz bandpass filter FL1 is a threepole Chebyshev type bandpass filter that uses discrete components. Maximum insertion loss is 8 db; bandwidth is 11.5 MHz at the 3 db reference points. The input and output impedance are 50 ohms resistive.

c. Crystal mixer Z1 is similar to a conventional balanced coaxial mixer but uses two forward diodes CR1 and CR2. The unit accepts a 220-MHz IF input signal at a level of +12 dbm and an RF input signal in the frequency range 4550 to 4850 MHz at a level of +16 dbm to +22 dbm. The resultant RF output frequency is in the range of 4330 to 5070 MHz; conversion loss does not exceed 12 db relative to the IF signal input level thereby producing an output level of about 0 dbm at J2RF OUT. The crystal current metering circuit consists of L1, C1, R1, R2, C3, L2 and FL2 in one mixer diode metering branch and L3, C5, R3, R4, C6, L4 and FL3 in the other mixer diode branch. Capacitors C2 and C4 provide coupling of the 220-MHz IF signal into the crystal mixer Z1.

d. The coaxial circulator HY1 has a bandpass of 4330 to 5070 MHz with a maximum insertion loss of 0.3 db. The circulator provides 18 db isolation



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN PICOFARADS
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN;
   PREFIX REFERENCE DESIGNATIONS WITH 2A5, 2A10, 2A25, OR 2A26.
3. ▭ INDICATES MARKING ON EQUIPMENT.

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Figure 1-40. 70-MHz IF filter 2A5/2A10, schematic diagram.

from port J1 IN to port J2 OUTPUT. A resistive termination is incorporated at port 3 to dissipate the rejected sideband from the following bandpass filter.

1-103. Frequency Multiplier Group 2A7 Circuit Theory
(fig. 8-62)

The frequency multiplier group for the receiver local oscillator chain functions the same as the frequency multiplier group for the transmitter local oscillator chain previously described in paragraph 1-52 with one exception, that is the addition of 4550 to 4850-MHz power divider 2A7HY2 in the output frequency path. The power divider is a combined circulator and coaxial hybrid junction with two output ports OUT-1 J2 and OUT-2 J3. A signal applied to input port J1 INPUT appears at both output ports OUT-1 J2 and OUT-2 J3. The two output port signals are equal in amplitude but one signal is shifted 90 degrees in phase with respect to the other output signal. Input and output impedances are 50 ohms resistive.

1-104. Amplifier-Multiplier 2A8 Circuit Theory
(fig. 1-41)

Amplifier-multiplier 2A8 amplifies and frequency multiplies (times 4) the 284.375 to 303.125-MHz output of frequency synthesizer 2A21. The resultant output signal, 1137.5 to 1212.5 MHz is applied to 1137-1213 bandpass filter 2FL10 in the receiver local oscillator chain. Amplifier-multiplier 2A8 consists of a low level amplifier and a quadrupler stage. The transistors in the low level amplifier are operated in the common emitter configuration. Their inputs at the base junction appear to the source as a low value resistance of approximately 16 ohms in series with an inductive reactance of approximately 8 ohms at 300 MHz. Their collectors appear to the load as a relatively larger resistance of approximately 150 ohms shunted by a low capacitive reactance in the order of 60 ohms. When operated in cascade, a coupling network is required to transform the impedance of the collector of the driving stage to the low input impedance of the driven stage and provide for maximum efficiency and stability.

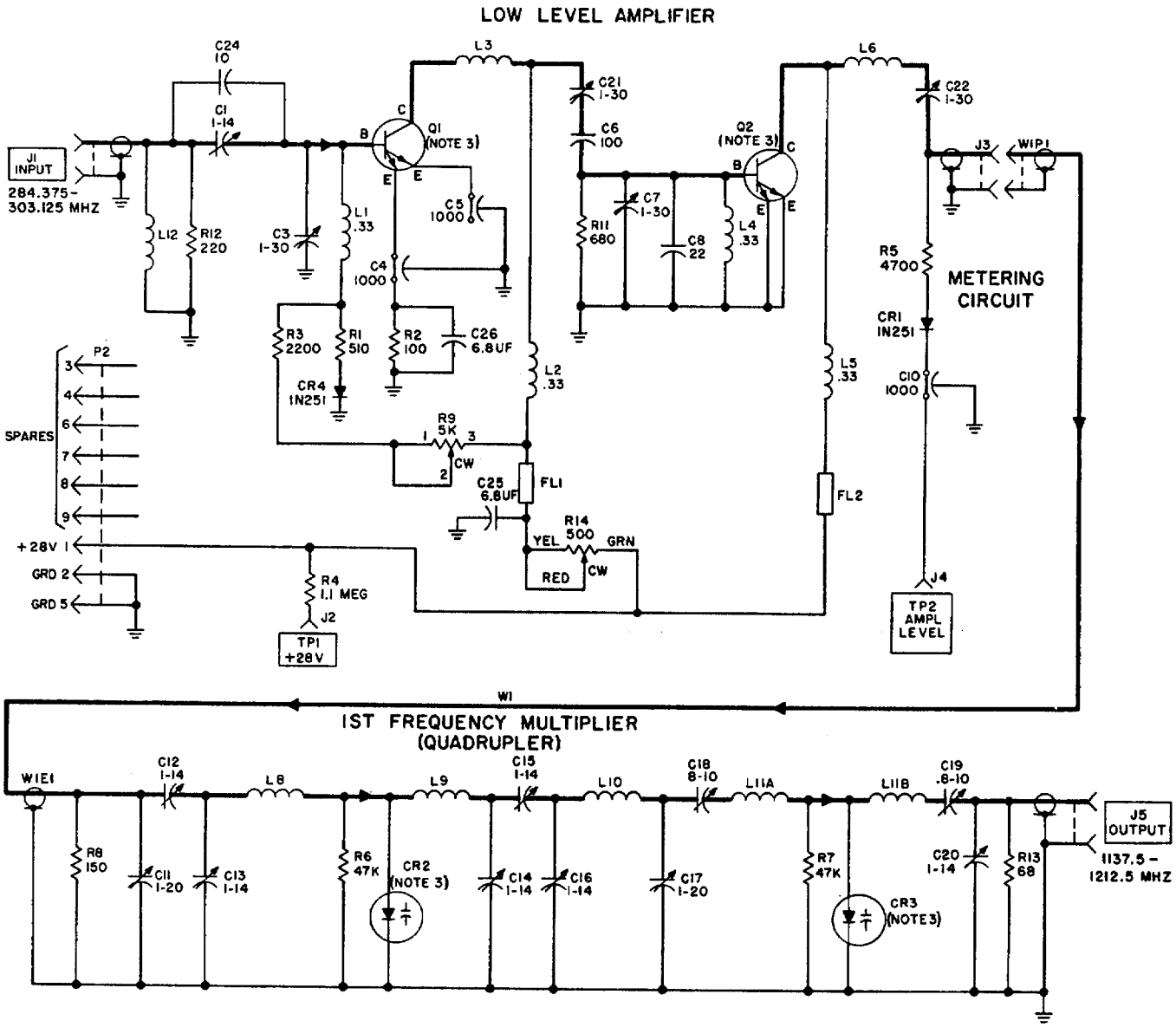
a. Low Level Amplifier. The low level amplifier is comprised of transistor stages Q1 and Q2. The low level 283.375 to 303.125-MHz input signal from frequency synthesizer 2A21 is applied to J1 INPUT connector. A matching network consisting of C1, C3, C24, L12, and R12 couples the input to the base of class a amplifier stage Q1. The network makes the necessary impedance transformation. Capacitors C4 and C5 bypass the emitter of Q1. Resistors R1, R2, R3, and R9 set the dc bias of the stage. Variable resistor R9 provides a means of varying the base bias, thereby permitting adjustment of stage gain. Q1 collector output passes through coupling network L3, C7, C8, and C21 to the base of class C amplifier stage Q2. The output of Q2 is fed to the quadrupler through cable W1. The matching is accomplished using a series network consisting of L6 and C22.

b. Quadrupler. The Quadrupler consists of two varactor multiplier doubler stages CR2 and CR3. Damping resistors R8 and R13 at the input and output provides stabilization. A tuned circuit consisting of C11, C12, C13 and L8 is tuned to the input frequency and couples the input to the first varactor diode CR2. This network matches the impedance from amplifier to CR2. Varactor CR2 is' the nonlinear element in the multiplier which generates the harmonics necessary for frequent multiplication. Self-biasing of the diode is achieved by resistor RS. CR2 is followed by a filter tuned to the second harmonic of the input signal. The filter transforms the diode impedance to 50 ohms thus permitting maximum power transfer. The filter section consists of C14, C15, C16, and L9. Network C17, C18, L10 and L11A provides interstage matching from CR2 to CR3, R7 provides self-biasing for CR3. A bandpass filter C19, C20, and L11B at the output is tuned to the fourth harmonic of the output frequency. The 1137.5-to 1212.5-MHz quadrupler is applied to the 1137 to 1213-MHz bandpass filter 2FL10 through J5 OUTPUT connector.

1-105. IF Amplifier 2A12/2A15 Circuit Theory
(fig. 863)

The IF amplifier is used to amplify the received 70-MHz IF signal to a level sufficient to drive the predetection combining circuits and to produce an amplified agc signal. Gain of the IF amplifier is 63 db minimum; bandwidth is 30 MHz at the 3 db half power points.

a. IF Amplifier. The incoming 70-MHz IF signal is applied to connector P1 and applied through IF GAIN potentiometer R2 to the base of



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN PICOFARADS.
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX REFERENCE DESIGNATIONS WITH 2A8.
3. REFER TO THE APPLICABLE SPECIFICATION DRAWING AS INDICATED BELOW:

DESCRIPTION	REF DESIG	SPEC. DRAWING
TRANSISTOR	2A8Q1	SM-B-683884-2
TRANSISTOR	2A8Q2	SM-B-651534
DIODE	2A8CR2, 2A8CR3	SM-B-651335

4. ☐ INDICATES MARKING ON EQUIPMENT.

EL5820-595-35-CI-8

Figure 1-41. Amplifier-multiplier 2A8, schematic diagram

the control of an age level. The age level is applied to diodes CR1 through CR4 which are connected in the interstage networks of the cascaded transistor stages Q1 through Q5. Diodes CR1 through CR4 present a minimum ac impedance at high dc currents and maximum ac impedance at low dc currents. This provides automatic gain control under the influence of the amplified agc voltage level established at the emitter of emitter follower stage Q10. A high level of agc voltage will cause a high dc current flow through the diodes CR1 through CR4 producing minimum attenuation of the incoming IF signal. The agc voltage is detected by diodes CR5 and CR6 and amplified by dc amplifier stage Q8 which controls current flow through emitter follower stage Q10. Each caseload transistor stage Q1 through Q5 is forward biased by a resistive divider network in their associated base circuit: the amplifier stages are tuned by the variable capacitors C4, C8, C12, C16 and C21 in their associated emitter circuit. Additional degenerative feedback is provided by the unbypassed resistor R57 in the emitter circuit of the input transistor Q1. The amplified IF signal is coupled through buffer Q6 the base or output amplifier Q7. The IF output signal is taken from a center tap on autotransformer T1. Output impedance is 75 ohms.

b. Age Circuit. Full wave detection of the amplified IF signal is provided by diodes CR5 and CR6 in conjunction with capacitors C28 and C31. The detected agc level is developed across series resistors R32 and R37. AGC SEL switch S1 allows selection of the source of age applied to the base of transistor Q8, this can be either the diversity-off (DIV OFF) agc level which is developed by the diodes in the IF amplifier or diversity-on (DIV ON) where the agc level is developed by detecting the combined IF signals in combiner 2A16. Transistors Q8 and Q9 are connected as a differential amplifier; the agc level is coupled from the wiper of AGC GAIN potentiometer R40 to the base of emitter follower transistor Q10. The operation of this circuit was described in a above. Placing AGC SEL switch S1 to TEST position disables the agc function and places the IF gain at a constant maximum value by grounding the base of transistor Q8. This will produce a 7-volt dc level at the cross-connect output (pin 13).

c. Metering Circuit. The metering circuits provide outputs to age metering circuits on the receiver front panel and to antenna alignment indicator 4A7. A meter voltage reference is developed by voltage divider R46, R47 and R48 in series with the + 15-volt supply. The METER ZERO potentiometer R47 allows adjustment of the voltage reference over the range 6.2 to 6.9 volts. The agc voltage level, developed across resistor R51, is coupled through resistor R43 and P3-9 to the receiver agc meter and is also coupled through resistor R52 and P3-11 to the antenna alignment indicator meter. The meters are deflected an amount proportional to the agc voltage level. A series voltage divider consisting of R49, R50 and diodes CR8 and CR9 produce a 1.5 to 7-volt dc reference for an alarm.

1-106. 220-MHz VCO 2A13/2A14 Circuit Theory (fig. 8-4)

Two identical 220 MHz vco's are used in the receiver local oscillator chain. The output of each 220 MHz vco 2A13 and 2A14 is applied to the associated frequency mixer module. The output frequency of each 220 MHz vco is controlled by an apc signal. Each 220 MHz vco consists of 110 MHz vco Y1 and frequency multiplier A1.

a. 110 MHz VCO Y1. The 110 MHz vco Y1 is a sealed assembly that provides an RF output of 110 MHz at a level of 15 milliwatts (across 50 ohms). The output is applied to frequency multiplier A1 via connector J1 and coaxial cable A1W1. The voltage control input (apc) allows a peak-frequency deviation of ± 300 Hz with an input level of ± 0.2-volt peak. A manual frequency adjustment control (FREQ ADJ) is accessible at the top of the assembly and has a tuning range of +400 Hz. The 110 MHz vco Y1 also contains an oven which maintains the ambient temperature at 75° C. An indication that the oven has reached the correct operating temperature is provided in the form of a closed pair of contacts (Pi-7 and P-6).

b. Frequency Multiplier A1. The frequency multiplier doubles the frequency of the incoming 110-MHz oscillator signal and amplifies the doubled frequency to a level of 70 milliwatts (across 50 ohms). The 110-MHz oscillator signal is applied through cable A1W1 to the base of input amplifier transistor Q1 through attenuator pad R1, R2 and R3 and base biasing network C3, R4 and R5. The amplified 110-MHz signal is capacitance coupled by C4 to the primary winding pins 1 and 2 of transformer T1. The frequency doubler stage consisting of transistors Q2 and Q3 is connected to the secondary windings of transformer T1 and conducts on alternate half cycles of the incoming 110-MHz signal; thus, the common collector signal from transistors Q2 and Q3 will be twice the frequency as the input signal. Inductor L3 in parallel with the output capacitance of the transistors resonates at 220 MHz. Capacitor C9 controls the drive to the base of OUTPUT amplifier stage Q4. Zener-diode CR1 in conjunction with resistor R11 provides a regulated 15 volts for application to the collectors of frequency doubler stage Q2 and Q3

and to the base biasing network, CR2, R12, R13, and R14 of output amplifier stage Q4 which amplifies the incoming 220 MHz signal. The output is taken from the tuned resonant circuit consisting of autotransformer L4 and capacitor C14. The output signal is coupled through an attenuator pad consisting of R16, R17, R18, R19 and R21. The output is adjusted to provide 70 milliwatts drive across a 50-ohm load at coaxial cable connector Q1W1 P2OUT. The J3 ALM connector provides a 5-milliwatt sample of the RF output across a 90-ohm load circuit in the alarm monitor 2A20. A sample of the output is detected by diode CR3 and applied to the receiver metering circuit through resistor R21 and filter FL1 METER. TP1 and TP2 provide monitor test points for + 28V and regulated 15V.

1-107. Combiner 2A16 Circuit Theory
(fig. 8-65)

Combiner 2A16 receives the outputs of channel A and channel B IF amplifiers 2A12 and 2A15. The combiner 2A16 monitors the channel A and B IF input levels, and, when the difference in these levels is within an acceptable limit, combines the two IF signals. When the difference in IF levels is greater than the acceptable limit, the weaker signal is suppressed. The combined IF signal (or the selected individual IF signal) is applied to demodulator 2A17. The combiner 2A16 contains a common automatic gain control (age) circuit which monitors the combined output level. The agc circuit generates a gain control signal which is fed back to the IF amplifiers to maintain a constant level at the output. The combiner 2A16 also incorporates individual channel A and B automatic phase control (apc) circuits. Each compares the phase of its channel input signal with the combined output signal. When a phase difference exists, the apc circuits provide a correction signal which is applied to the associated 220 MHZ vco 2A13 or 2A14. The correction signal changes the frequency of the 220 MHz vco bringing the individual and combined IF signals back in phase. A carrier IF alarm circuit in each channel provides a delayed alarm signal to alarm monitor 2A20, whenever its associated input level is below a predetermined level. The delay prevents momentary signal fades from activating the alarm. The combiner circuits are described in a through f below.

a. IF Signal Amplifiers. Each IF input signal is amplified in a three-stage IF signal amplifier comprising Q1, Q2, and Q3, in channel A and Q9, Q10, and Q11 in channel B. Since they are identical, only the channel A circuit is described.

(1) The input at IN CHAN A J1 connector is TM 11-5820-595-35 applied to the base of emitter follower stage Q1 via coupling capacitors C2, C3, divider R1, R2, and tuning inductor L1. Base bias for emitter follower Q1 is supplied by voltage divider R3, R4 and the output is developed across emitter load resistor R5. The output is fed to the base of emitter follower stage Q2 through coupling capacitors C6, C8, squelch diode CR1 and resistor R9. Squelch diode CR1 suppresses the channel A signal when the channel A input is weak. A + 15 volts is applied to the cathode of squelch diode CR1 through resistor R6. When the anode of squelch diode CR1 is at a lower voltage it conducts and the signal is fed to the base of emitter follower stage Q2. The method by which the anode voltage is controlled is described in *d* and *e* below.

(2) The base of emitter follower stage Q2 is biased by voltage divider R7, R8, Resistor R9 at the input improves the operating point stability. The output at the emitter of Q2 is direct coupled to the base of amplifier stage Q3. Resistor R12 is the collector load resistor, and R13, R14, and RT1 provide the emitter load. A positive temperature coefficient thermistor, RT1, prevents output level variations due to changes in ambient temperature. Since its resistance increases with temperature, it reduces the base-emitter bias. This compensates for the tendency for the collector current of the amplifier stage Q3 to increase with temperature. Bypass capacitor C12 limits negative feedback in the emitter circuit. The output of the channel A IF signal amplifier Q3 is combined with the output of the channel B IF signal amplifier Q11 through coupling capacitors C13 and C44. The combined IF signal is fed to emitter follower stage Q12 and through capacitor C43 and resistor R59 to pin 8 of coaxial cable W1P2 OUT which interconnects the combiner 2A16 with demodulator 2A17.

b. AGC Circuit. The agc circuit consists of diode detector CR12, emitter follower Q13, dc amplifier Q18, and associated components. The agc circuit produces dc voltages that are proportional to the combined IF signal level. The dc voltages are used to control the gain of the IF amplifiers, the balanced differential comparator 'circuit (e below), and the system clock correction circuits in digital data modem 1A12.

(1) The combined IF signal is applied to diode detector CR12 in the agc circuit through coupling capacitor C45. The signal is rectified by diode CR12 and filtered through bypass capacitors C47 and C48 for application to the base of emitter follower stage Q13. Base drive current for emitter follower stage Q13 is supplied by a resistance network consisting of R60, R61, R89, R90, and R91. A ± 12 volts, derived from the ± 15-volt

bus by resistor R91 and voltage reference diode CR20, is applied through resistor R90 to the variable arm of AUTO AGC ADJ control R89. The AUTO AGC ADJ control R89 sets the nominal agc level and, in turn, the IF signal level into the demodulator 2A17.

(2) Quiescent base current in emitter follower stage Q13 is determined by the current flowing between the positive voltage at the variable arm of AUTO AGC ADJ control R89 and 12 volts in the emitter circuit of Q13. The total base current in emitter follower stage Q13 is the sum of the rectified current from diode CR12 and the current from the above biasing circuit. Inductor L21 and capacitor C46 prevent signal current from bypassing the diode CR12. The voltage across resistor R60 is applied to the receiver meter panel for monitoring the nominal age level. Diode CR13, connected between R63 and emitter of emitter follower stage Q13, provided temperature compensation. When AGC AUTO-MAN switch S3 is in the AUTO position. output of emitter follower stage Q13, is applied to the 70-MHz IF amplifiers 2A5, 2A10. When AGC SEL switch S3 is in the MAN position, agc control is transferred to voltage divider R68, R69 which is supplied from the + 15 volt bus. The agc control signal is then manually set by varying MAN AGC ADJ control R68.

(3) The age circuit also generates a AGC-PCM control signal for digital data modem 1A12. The drive for this signal is developed at the variable arm of the ALM ADJ control R65 in resistor chain R64, R65, R66. The drive signal is applied to the base of dc amplifier stage Q7 which supplies the output signal used to drive the base of dc amplifier stage Q18 in the AGC circuit. The output from the dc amplifier Q18 consists of AGC-PCM control signal which is applied to digital data modem 1A12 through resistor R67 and PIN 10 of connector P1. The emitter of dc amplifier stage Q18 is returned to ground through diode CR8 which is also in the emitter circuit of dc amplifier stage Q7. Resistors R104 and R108 establish the collector supply voltage for the dc amplifier stage Q18.

c. Apc Circuits. The channel A and channel B apc circuits are basically phase detector circuits. The channel A APC circuit is comprised of T1, Q8, CR9, CR10 and associated components, while that for channel B APC circuit comprises T2, Q17, CR21, CR22 and the associated components. Since the two circuits are identical only the channel A APC circuit is described.

(1) The channel A input signal is applied to the primary winding of transformer T through coupling capacitor C1 and tuning inductor L8. The combined IF signal is fed to the junction of capacitors C24 and C25 through emitter follower stage Q8. Since the secondary winding center tap of transformer T1 is at RF ground through to capacitor C23, the secondary drive is effectively between the junction of capacitors C24 and C25 and secondary of transformer T1. The output, developed across resistor R44, is fed through coupling elements R43, C27, and DL1. Tuning is accomplished through variable capacitor C28. Delay Line DL1 introduces the phase shift required to compensate for phase delays which occur in the IF signal amplifier. Thus, the necessary phase relationship between the channel A and combined IF inputs is restored.

(2) When the two inputs are in phase, a 90 degree phase difference exists between the IF combined signal and the input signal across secondary of transformer T1. For this condition, the voltages across diodes CR9 and CR10 are equal and opposing so that no net current flows. When the two IF signals are out of phase, the voltage across one half of the secondary (transformer T1) is more than 90 degrees out of phase with the IF combined signal, while the other half of the secondary (transformer T1) has a phase difference of less than 90 degrees. Since the diode voltage (CR9 and CR10) is the vector sum of the secondary voltage and the IF combined signal, the diode voltage and the IF combined. signal, and diode voltage associated with the larger phase angle will be greater than the other. The diode currents are opposing and the resulting net current flow is due to the voltage difference. The amplitude represents the extent of the frequency error, and the polarity, the direction of the error.

(3) The detector output from diodes CR9 and CR10 is filtered through capacitors C24, C26, inductor L9 and applied to channel A APC-ON-OFF switch S2. With channel A APC-ON-OFF switch S2 in the ON position, the APC-A correction signal is applied to 220 MHz vco 2A13 through pin 11 of P1. With channel A APC-ON-OFF switch S2 in the OFF position, the output is grounded. The detector output is also applied to voltage divider consisting of resistors R41, R42 which supplied an APC-A metering signal to the meter selector switch in the receiver through pin 12 of P1.

d. Squelch Detector Circuits. The channel A and channel B squelch detector circuits monitor the associated channel A and B inputs. The squelch detector circuits provide a positive or negative output (dc squelch voltage), depending on which input signal (channel A or B) is greater. The dc voltage is applied to the A and B inputs of the balanced differential comparator (e below). The

amplitude of the dc voltage represents the differential level, while the polarity identifies which is the stronger signal. Since the channel A and B squelch detector circuits are identical, only the channel A circuit is described in detail.

(1) The channel A input is fed through capacitor C16 to level detector CR4, CR5, which passes positive half cycles. The channel B input through C50 is similarly processed by level detector CR14, CR15, but this circuit passes negative half cycles. Ripple on the two rectified signals is filtered through bypass capacitors C17 and C51, respectively, and the essentially dc voltages are applied to IF BAL ADJ control R15. The resulting current from the variable arm if IF BAL ADJ control R15 through load resistor R17 represents the differential level. A positive polarity indicates that the associated channel has the higher level; a negative polarity indicates a lower level. The IF BAL ADJ control R15 is set during alignment.

(2) The positive or negative signal is applied to the noninverting input of operational amplifier A1. Capacitor C18, resistors R16, R18, and R19 are compensation and feedback elements which establish the transfer characteristic of the amplifier A1. The channel B SQUELCH ADJ control R18 is used to set the desired squelch threshold.

(3) The output of amplifier A1 is applied to dc amplifier stage Q4 in the balanced differential comparator through diode gate CR6. The anode of diode gate CR6 is biased at approximately 4.4 volts by voltage divider R21, R22, R103 and blocks output levels below 4.4 volts. Variable resistor R21 permits adjustment of the level. In the channel B section, the voltage divider consists of resistors R76 and R77, and is not adjustable. It is important to note that due to the complementary operation of the channel A and B squelch detectors, their operational amplifier output signals are always of equal amplitude but opposite polarity.

e. Balanced Differential Comparator Circuit. The balanced differential comparator circuit controls the squelch diodes CR1 and CR11 in the channel A and B IF signal amplifiers. The circuit consists of three transistor stages Q4, Q7 and Q14 which are common emitter configurations. The circuit receives three inputs. The channel A and B squelch detector circuit outputs are applied to the bases of dc amplifier stages Q4 and Q14 respectively. The agc alarm signal is applied to the top of common emitter resistor R26 through dc amplifier Q7. As noted in the preceding description of the squelch detector, the channel A and B output signals are always of equal amplitude and of opposite polarity. The agc alarm signal is proportional to the combined IF output level. The output at the collector of each dc amplifier stage Q4 and Q14 controls the diode gate CR6 and CR18 in its associated channel A and B IF signal amplifier and also drives its associated carrier IF alarm circuit.

(1) With nearly equal input levels, the squelch detector outputs are negligible. Diode gates CR6 and CR18 are open, and dc amplifier stages Q4 and Q14 operate under control of the fixed base bias derived from voltage dividers R21, R22, R103 and R76, R77, respectively. Both transistors Q4 and Q14 saturate causing a voltage drop across their collector load resistors R23 and R78. The voltage drops bias squelch diodes CR1 and CR11 into conduction. Under these conditions, both IF signal amplifiers supply outputs which are combined and fed to output cable W1.

(2) When the IF input channels become unbalanced, the channel A squelch detector circuit has a positive output sufficient to close diode gate CR6 and the channel B squelch detector circuit has a negative output of equal magnitude diode gate CR18 opens. The increased base voltage at dc amplifier Q4 causes its emitter current to increase, causing the voltage drop across resistor R25 to increase. Since resistor R26 is common to both dc amplifier stages the Q4 and Q14, emitter voltage (Q14) increases sufficiently to cause Q14 to cut off, raising its collector potential to +15 volts is also supplied to voltage divider 1181, R82 in the channel B IF alarm circuit raising the dc amplifier stage Q15 base voltage from a negative to a positive level turning on dc amplifier stage Q15. With dc amplifier stage Q15 turned on, a channel B IF carrier ALM signal is applied to the ALARM monitor 2A20 through diode CR19, emitter follower Q16 and pin 16 of P1.

(3) A third input (agc alarm signal) to the comparator is applied at the junction of R25 and R26. Assume that the input channels are essentially balanced, but the combined output is below radio threshold. The alarm signal derived at the variable arm of ALM ADJ control R65 which is applied to the base of dc amplifier Q7. Above radio threshold this voltage has a small positive value. Since emitter of dc amplifier stage Q7 is held at approximately--0.7 volt by diode CR8, the dc amplifier stage Q7 is turned on shunting resistor R26. At radio threshold, the input level to base of dc amplifier stage Q7 is reduced to the point where it cuts off. The combined emitter currents of dc amplifier stages Q4 and Q14 now flow through resistor R26, increasing the emitter voltage of each dc amplifier stage Q4 and Q14 from a saturated state to a lesser conducting level. The collector voltages (Q4 and Q14) increase, but not sufficiently to cause squelch diode gates CR1 and CR11 to open. However, the increased voltage at

the input to voltage divider R28, R29 and R81, R82 is sufficient to turn on both dc amplifier stages Q5 and Q15, activating both alarm circuits (channel A and B IF carrier alarm).

(4) With channel A SQUELCH ONOFF switch S1 and channel B SQUELCH ON-OFF switch S4 in the OFF position, the switches connect squelch diodes gates CR1 and CR11 to ground through R27, and R80, closing both diode gates CR1 and CR11. The base voltages applied to dc amplifier stages Q5 and Q15 in the channel A and B carrier IF alarm circuits are derived from voltage dividers R27, R28, R29 and R80, R81, R82 respectively. These voltages are approximately --3 volts, so that both transistors are cut off, and the alarms are deactivated.

f. Carrier IF Alarm Circuits. The Channel A carrier IF alarm circuit consists of amplifier stage Q5 emitter follower stage Q6, and diode gate CR7, while the Channel B circuit comprises amplifier stage Q15, emitter follower stage Q16, and diode gate CR19. Since the channel A and channel B IF alarm circuits are identical, only the channel A circuit is described.

(1) With amplifier stage Q5 cut off, the only current path for its collector source is through resistors R30, R33, R34, diode CR7 and the base emitter junction of emitter follower stage Q6 to ground. With the collector of amplifier stage Q5 at approximately +8 volts, and the base of emitter follower stage Q6 at approximately +4 volts, Emitter follower stage Q6 goes into saturation, causing its emitter voltage to go to approximately +3.3 volts. This signal is fed through resistor R35 ho alarm monitor 2A20 through pin 14 of P1 us a Channel A carrier IF Alarm signal. Capacitor C22 charges to approximately +7.5 volts during this period.

(2) When an alarm condition occurs, base of amplifier stage Q5 is driven slightly positive, causing it to conduct and draw collector current through resistor R30. The collector voltage of amplifier Q5 drops and diode CR7 becomes reversed biased. Since the collector voltage of amplifier stage Q5 is lower than the +7.5-volt charge on capacitor C22, the capacitor (C22) discharges through resistors R33 and R34 and the base-emitter junction of emitter follower stage Q6, delaying the voltage drop in the base of emitter follower stage Q6. the purpose of this delay (approximately 5 seconds) is to prevent undesirable alarm indications, during momentary propagation fades. When capacitor C22 voltage has dropper to the collector voltage level of amplifier stage Q5, diode CR7 starts conducting, and voltage in the base of emitter follower stage Q6 drops to a low level. When normal operation is restored, amplifier stage Q5 is cut off, capacitor C22 charges to +7.51 volts, and the circuit stabilizes in the nonalarm status.

1-108. Demodulator 2A17 Circuit Theory (fig. 8-66)

Demodulator 2A17 converts the 70-MHz IF signal from combiner 2A16 to the pcm and order wire signal. The demodulator consists of an input stage, a four-stage limiter, a two-stage discriminator driver, a frequency discriminator, and a video output stage.

a. Input Stage. The input from the combiner 2A16 is applied to J1 IF INPUT connector and through coupling capacitor C1 to input stage Q1. This stage matches the combiner input impedance to the first limiter stage Q2. Input stage Q1 is biased by resistor R2, R4 and R6, while resistor R5 terminates the combiner input. Capacitors C3 and C5 are bypass capacitors. The output is taken from the emitter of input stage Q1 and fed through coupling capacitor C8 to the first limiter shape Q2. A diode detector CR1 connected to the base of input stage Q1 through coupling capacitor C2 monitors the IF input. The detector circuit consists of diode CR1 and resistor R1. When the signal goes negative, diode CR1 conducts grounding the signal; the diode (CR1) is nonconducting during positive half cycles. This produces a rectified signal which is filtered by r-c circuit R3 and C4. The resultant dc is made available through test point J2 (TP2 INPUT LEVEL).

b. Limiter Stages. The purpose of the limiter stages Q2 through Q5 is to prevent amplitude variations (amplitude modulation) from appearing at the frequency discriminator input. The limiter stages Q2 through Q5 operate in the common base configuration. Since the four limiter stages Q2 through Q5 are identical, except for minor variations in biasing and tuning, only the first limiter stage Q2 will be described in detail. The input is applied to the junction of resistors R10 and R11. Resistors R10 and R11, together with voltage divider R7, R8 establish the bias of first limiter stage Q2. The bias is bypassed by capacitors C7 and C11, which serve as a ground return for the RF signal. Variable inductor L5 tunes the collector circuit. Resistor R9, connected across variable inductor L5, limits the first limiter stage bandwidth providing stability. The output of first limiter stage Q2 is tapped from inductor L5. The limiting action is obtained by operating Q2 near saturation. The base is biased at +13.5 volts dc. A resistance of 1015 ohms introduced in the emitter circuit by resistors R10 and R11 results in highly stable operation ear the saturation region. Under these conditions, the collector to emitter voltage is

in the order of 1.0 volt. A negative signal swing tends to further increase the current of first limiter stage Q2 but, because of the near saturation condition, the swing at the collector is limited. With a positive signal swing, the emitter voltage tends to become more positive, thereby reducing the base to emitter voltage. Thus, in turn, causes the emitter voltage to decrease, due to the reduced emitter current through resistors R10 and R11. Because of these counteracting effects, the output voltage swing due to positive signal excursions is also limited. The second, third, and fourth limiter stages operate in an identical manner. The fourth limiter stage Q5 output is tapped from inductor L14 and applied to the first stage of discriminator driver Q6 through capacitor C33. Output of the fourth limiter stage Q5 is also fed to a metering circuit consisting of diode detector CR2, R30, and associated r-c filter R27, C31. The metering circuit, which produces a dc signal available at test point J3 designated TP3 LIM LEVEL. The dc signal is proportional to the limiter output level, operates in the same manner as the metering circuit in the input stage.

c. Discriminator Driver. The discriminator driver consists of transistor stages Q6 and Q7. The first stage Q6 is an emitter follower. The signal enters at the base, and the output is taken off at the junction of emitter resistors t+31 and R32. Biasing is provided by voltage divider R28, R29, and emitter resistors R31 and R32. Capacitors C35 and C37 are bypass capacitors. The input to second stage Q7 is coupled through capacitor C38 to the junction of emitter resistors R36 and R37. The second stage Q7 is configured common base, and, unlike the limiter stages Q2 through Q5, is biased in the linear region. Base bias voltage of +3.75 volts is derived from voltage divider R33, R34, and emitter bias from emitter resistors R36 and R37. The base is bypassed by capacitor C39, and the emitter by capacitor C44.

d. Frequency Discriminator. The frequency discriminator recovers the video signal (pcm and order wire) from the modulated 70-MHz IF signal. It operates on the phase shift principle, and consists of transformer T1, diodes CR3 and CR4, and associated components.

(1) Both the primary and secondary of T1 are tuned to the 70-MHz center frequency. Tuning is accomplished by variable capacitors C43 and C45 respectively. The signal from second stage Q7 of discriminator drive circuit is connected across the primary winding of transformer T1, and also to the center tap of the secondary winding (T1) through capacitor C41. With a 70-MHz signal applied, the voltages across each half segment of secondary winding of transformer are in quadrature with the voltage across the primary winding of T1. They are of equal amplitude and are in opposition. When the signal is above resonance, the phase angle between one half of the secondary winding (T1) of the primary winding (T1) is greater than 90 degrees. Below resonance, these phase relationships are reversed, the phase angle for the first half of the secondary winding (T1) being less than 90 degrees, and that for the second half of secondary winding (T1), greater than 90 degrees. As in the resonant case, the two secondary voltages are of equal amplitude and 180 degrees out-of-phase.

(2) The signals at the cathodes of diodes CR3 and CR4 are the vector sums of the primary and associated secondary voltages. At resonance these signals are of equal amplitude, while off resonance, the signal associated with the half secondary winding (T1) having the greater phase difference, is the larger. The difference between the two voltages is proportional to the frequency excursion. from the resonant frequency. The modulation (video) is recovered by the rectifying action of diodes CR3 and CR4. Since the voltages across diodes CR3 and CR4 are in opposition, the current through load resistors R40 and R41 is produced by the difference between the impressed voltages. The signal developed across the load resistors R40 and R41 has, as its fundamental frequency, the recovered video. Ripple at the IF frequency is bypassed through capacitor C46.

(3) Two positive coefficient thermistors, R35 and R41, are used in the frequency discriminator to compensate for terminal effects in emitter follower stage Q7 and video output amplifier Q8. The thermistors R35 and R41 have a temperature coefficient of approximately +-t0.7 percent per degree centigrade. The resistance of thermistor R35 in the collector circuit of emitter follower stage Q7 increases with increasing ambient temperature. This action compensates for the tendency of collector current of emitter follower stage Q7 to increase as its junction temperature increases. Similarly, thermistor R41 increases the output signal at capacitor C48, with increasing ambient temperature, compensating for thermal effects in video output amplifier Q8, Q9.

(4) A metering circuit is provided at the discriminator output, consisting of R42, C47, and J4 TP4 DISCR. When the mean IF frequency into the discriminator differs from the resonant frequency of transformer T1, a dc component is present in the discriminator output at the junction of resistor R40 and thermistor R41. The de level depends on the frequency offset, and the polarity on whether the IF frequency is above or below transformer T1 resonant frequency. This dc component is extracted by r-c filter R42, C47, and can be monitored at J4 designated TP4 DISCR, thus determining whether the discriminator is properly tuned, or conversely, whether the IF frequency is properly centered.

e. Video Output Amplifier Stage. The video output amplifier stage consists of transistors Q8 and Q9 and associated components. The discriminator output is applied through coupling capacitor C48 to the base of transistor Q8, which together with transistor Q9 comprises a Darlington amplifier. This circuit provides isolation between the frequency discriminator and the low pass filter, 2A18. Voltage divider R43, R44 sets the base bias for transistor Q8, while resistor R43 limits the collector current of transistors Q8 and Q9. Capacitor C51 bypasses the collectors of transistors Q8 and Q9, and the output is developed across resistor R45. The output is coupled through capacitor C52 to terminating resistors R47, R48, and applied to the low pass filter 2A18 through VIDEO OUTPUT connector J6.

1-109. 260-KHz Low Pass Filter 2A18 and 680-KHz Low Pass Filter 2A27 Circuit Theory

(fig. 1-42)

a. The 260-kHz low pass filter 2A18 and 680 kHz low pass filter 2A27 are used in the baseband signal path from demodulator 2A17 to restrict the bandwidth and, thus, reduce the noise components in the signal during 12-or 24-channel operation. The 260-kHz low pass filter 2A18 is used in the radio set during the 12-channel mode of operation and replaced with 680-kHz low pass filter 2A27 during 24-channel operation.

b. The 260-kHz low pass filter 2A18 is shown in section A of figure 1-42. The 260-kHz low pass filter 2A18 filter is a five-pole low pass filter tuned to approximate Gaussian shaping with a 3 db bandwidth of 260 kHz. The peak deviation of the 12-channel frequency modulated signal is adjusted for 250 kHz. At 360 kHz, the filter attenuation is 6.5 db; at 720 kHz, the filter attenuation is 22 db. Source impedance is 50 ohms and the load impedance is 150 ohms. Circuit components consist of L1, L2, and C1, C2, and C3 are the poles of the filter. Resistor R1 provides impedance matching between the equally loaded design of the filter (150-ohm input and output impedances) and the unequal source and load impedance.

c. The 680-kHz low pass filter 2A27 is shown in section B of figure 1-42. The 680-kHz low pass filter 2A27 is also a five-pole low pass filter tuned to approximate Gaussian shaping with a 3 db bandwidth of 680 kHz. The peak deviation of the 24-channel frequency modulated signal is adjusted for 500 kHz. At 961 kHz, the filter attenuation is 6 db; at 1882 kHz, the filter attenuation is 20 db. The circuit component descriptions are the same as described for the 260-kHz low pass filter 2A18.

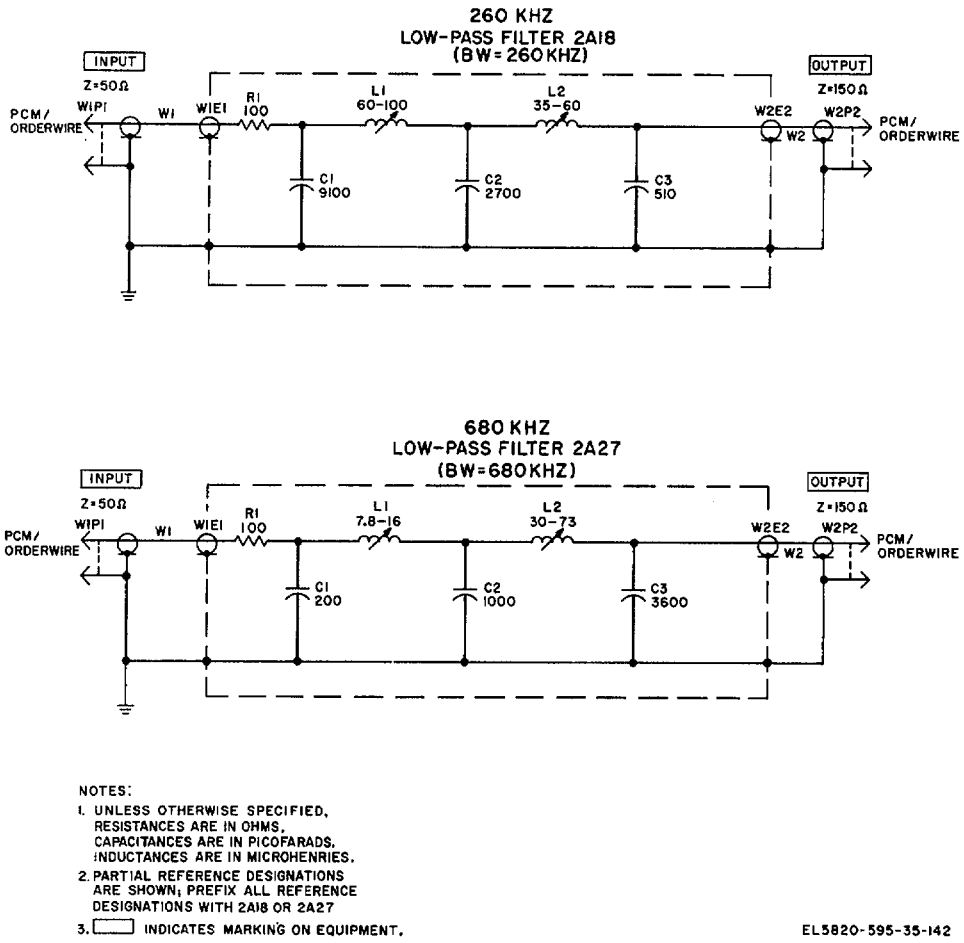


Figure 1-42. 260-kHz low pass filter 2A18 and 680-kHz low pass filter 2A27, schematic diagram.

1-110. AF-RF Amplifier 2A19 Circuit Theory
(fig. 1-25)

AF-RF amplifier 2A19 is a wide band video amplifier and is identical to AF-RF amplifier 1A4 used in the transmitter. The circuit theory description provided in paragraph 1-46 for AF-RF amplifier 1A4 also covers AF-RF amplifier 2A19 with the following exceptions: The pcm and order wire signal from low pass filter 2A18 is applied to J1 1N and is amplified by AF-RF amplifier 2A19; the order wire input (P1-8) is not used; the amplified output (pcm and order wire signal) is applied to digital data modem 1A12 through J2 OUT as a traffic out signal; and a traffic monitor signal is made available at P1-pin 9 and applied to the alarm monitor 2A20.

1-111. Alarm Monitor 2A20 Circuit Theory
(fig. 1-24)

a. Alarm monitor 2A20 is identical to alarm monitor 1A5 used in the transmitter, however, the jumper connections on the associated plate assembly connectors for each module are different. The circuit functions of alarm monitor 1A5 are described in paragraph 1-47. Circuit functions of alarm monitor 2A20 are described in b through g below.

b. Low level alarm monitor input signals are amplified by integrated circuit operational amplifiers AR1, AR2 and AR3 (fig. 1-24(3). These are connected in different configurations to accommodate each particular receiver alarm monitor input signal. The inverting input of the integrated circuit amplifiers is pin 2, the noninverting input is pin 3; the output signal is taken from pin 7. The feedback resistance connected from the output pin 7 to the inverting input pin 2 establishes gain of the operational amplifiers AR1 through AR3.

c. The traffic monitor signal is applied to pin 13

of P2, board A1, to the inverting input pin 2 of operational amplifier AR1. The network consisting of capacitor C1 and resistor R4 are connected across the differential inputs (pins 2 and 3) of operational amplifier AR1 providing lag compensation which increases the high frequency response. The amplified traffic monitor signal is applied to detector circuit consisting of capacitors C4, C5 and diodes CR1 and CR2. The positive detected dc voltage forward biases emitter follower stage Q1. The positive detected dc voltage from diode CR2 is used to forward bias the emitter follower stage Q1. The output signal from emitter follower stage Q1 is applied to an attenuator network consisting of resistors R10 through R12. The attenuated output signal from the junction of resistors R11 and R12 is then applied to a Schmitt trigger circuit (Q5 and Q6) in board A5 through pin 7 of board A1 and pin 8 of board A5. The Schmitt trigger circuit for the traffic monitor signal consists of transistors Q5 and Q6 (fig. 1-24 (2)). When no signal is present transistor Q6 conducts and holds transistor Q5 off due to the voltage developed across common emitter resistor R48. The incoming detected traffic monitor signal will forward bias transistor Q5 when the magnitude of the detected traffic monitored signal exceeds the magnitude of the voltage developed across common emitter resistor R48. When this occurs transistor Q5 conducts and transistor Q6 cuts off until the detected signal again drops below the voltage level of the common emitter resistor R48. The output of the Schmitt trigger circuit (Q5 and Q6) is a series of positive square pulses which are developed at the collector of transistor Q6. These pulses are applied to the base of amplifier stage Q7 to forward bias it into conduction. When inverter stage Q7 is conducting, its collector is at a low level; this provides a low impedance path to ground to light the normal (green) TRAF indicator lamp on receiver meter panel. The inverted output level at the collector : of transistor Q6 is applied to the alarm (red) portion of TRAF indicator lamp. Transistor Q6 provides a low impedance path to ground for the alarm TRAF lamp when no traffic signal is detected (quiescent state of the Schmitt trigger circuit).

d. Two vco lock monitoring signals (VCO-A and VCO-B) are applied to the input circuit of amplifier AR2 through pins A1 and A2 of P2 board A1 (fig. 1-24 (3)). These signals are samples of the receiver channel A 220-MHz local oscillator 2A13 and of the receiver channel B 220-MHz local oscillator 2A14. These signals are summed and applied to detector diodes CR3 and CR4. When these signals are the same frequency (inphase), a steady dc voltage is developed across resistor R18 which is blocked from appearing at the input of amplifier AR2 by capacitor C9. When there is a difference in frequency between the two vco signals an audio difference signal is developed across resistor R18 which is applied as an input to amplifier AR2. This circuit functions the same as integrated circuit AR1 previously discussed in *c* above with the exception that no lag network is incorporated across the differential inputs. (This network. is not necessary for this configuration due to the low signal frequencies developed as an input to the amplifier.) The difference frequency is amplified and applied to detector diodes CR9 and CR10 through pin 17 of board A5 (fig. 1-24 (1)). The positive detected dc voltage forward biases the base of emitter follower stage Q2 and appears across emitter resistor R41. The voltage variations at that junction of emitter resistor R41 are integrated by an r-c network consisting of resistor R43 and capacitor C21. The time constant of the r-c circuit is long to provide a minimum 4-second signal time-delay to the input of the following Schmitt trigger circuit Q8, Q9. (This prevents momentary out-of-phase conditions such as signal fading from triggering the alarm.) The amplified difference frequency is also applied to a high pass filter network consisting of capacitor C17 and resistor R39. The output of the high pass network is applied to detector diodes CR7 and CR8. As the difference between vco frequency increases the reactance of capacitor C17 decreases; therefore, the level of detected voltage across resistor R40 will increase. The detected level controls deflection of the front panel meter when VCO FREQ. DIFF position is selected through the meter selector switch. As the difference frequency increases the meter reading will increase. The delayed out of emitter follower stage Q2 is applied to the base of transistor Q8 of Schmitt trigger circuit through series resistor R55 and pin 19 of board A5 (fig. 1-24 (2)). This circuit functions in an identical manner to Schmitt trigger circuit Q5 and Q6 previously described in c above with the exception that the normal indication is taken from the collector of transistor Q9 and the alarm indication is taken from the collector of amplifier stage Q10. The presence of an input signal will cause an alarm indication, the absence of an input signal will produce the normal indication.

e. The carrier (IF) level A and carrier (IF) level B monitor signals are derived in the combiner 2A16 and are direct-coupled to their respective Schmitt trigger circuits on board A5 through restrictive summing networks on board A1. Resistors R36, R37 and R38 (fig. 1-24 (3)) form part of one summing network, the other part is the series resistor in the combiner carrier alarm output circuit. A plus 8 volts applied to the input pin 16 of board A1 (fig. 1-24 (3)) will cause a normal (green) CARR (IF) A indication and a +2.5-volt input applied to the input pin 16 of board A1 will cause the alarm (red) CARR (IF) A indication. The Schmitt trigger circuit for carrier (IF) level B consists of transistors Q20 and Q21 (fig. 1-24 (2)). Transistor Q22 is an inverter which controls the normal (green) CARR (IF) B indicator on the receiver meter panel. Potentiometer R35 on board A1 (fig. 1-24(3)) and resistors R84 and R85 (fig. 1-24 (2)) are part of the summing network for carrier (IF) level A. Transistors Q17 and Q18 (fig. 1-24 (2)) comprise the Schmitt trigger circuit for carrier (IF) level A. Transistor Q19 is an inverter which controls the normal (green) CARR (IF) A indicator on the receiver meter panel.

f. A six-input diode OR gate and inverting transistor provides the summary alarm function. This circuit consists of diodes CR12 through CR17, transistor Q23 and resistors R102 and R103 (fig. 1-24 O). When the anode of any input diode has a positive voltage level applied to it, it conducts and forward biases transistor Q23 into conduction producing a summary alarm condition. When all of the diodes have a low (or zero) voltage applied to their anodes, they are nonconducting and transistor Q23 is turned off producing a normal indication.

g. Two Zener diodes are incorporated on board A1, which provide regulated plus and minus voltages for the integrated circuits. Zener diode CR5 (fig. 1-243) in conjunction with resistor R31 provides a regulated plus 10 volts. Zener diode CR6 (fig. 1-24 () in conjunction with resistor R33 provides a regulated minus 8.2 volts.

1-112. Frequency Synthesizer 2A21/1A14 Circuit Theory

Frequency Synthesizer 2A21/1 A14 Circuit Theory Frequency synthesizer 2A21 is identical to frequency synthesizer 1A14 used in the transmitter. Refer to paragraphs 1-73 through 1-81 for the circuit theory description.

Section V. FUNCTION OF POWER AMPLIFIER

1-113. General

Major power amplifier (unit 3) components include a meter panel, klystron assembly 3A9V1, control and monitoring modules 3A1 through 3A6, power supply control 3A7, and a high voltage power supply primarily consisting of inverter 3A8 and power supply 3A9A1. The power amplifier boosts the 40-milliwatt RF input signal to a 1-kilowatt RF output signal. The following paragraphs cover the power amplifier as follows: at the block diagram level describing the RF signal flow and power control circuits; functional block diagram level describing the function of each module and the relationships between all power amplifier circuits; and circuit level theory of the modules at the schematic diagram level.

1-114. Power Amplifier Block Diagram Description (fig. 8-67)

The RF signal path through the power amplifier and the power control and protective circuits are shown in figure 8-67. The diagram includes all switches and circuit breakers associated with the power control and protective circuits.

a. RF Circuits. The RF input received from the transmitter and applied to klystron 3A9V1 through variable attenuator 3A9AT1 and input directional coupler 3A9DC1. The four-cavity klystron provides 1-kilowatt (minimum) RF output over its tunable frequency range from 4.4 to 5.0 GHz. Beam voltage for the klystron is a nominal 7500 volts and is provided by the high voltage power supply circuits. The 6.4 vac klystron filament supply voltage is developed in the filament supply circuit.

b. Power Control Circuits. When first starting the power amplifier, power must be applied in a definite sequence. Initially, MAIN POWER circuit breaker 3A9A1CB1, MAIN POWER SWITCH 3A9A32S5, and BEAM SWITCH 3A9A31S4 are in the OFF positions (red indications) all other circuit breakers are in the ON positions, and all interlocks are closed. Closing the MAIN POWER circuit breaker applies 115 vac to' the -12v (B) power supply, the time-delay control module

(3A5), and the MAIN POWER SWITCH, lighting the switch indicator. clear lamp.

(1) Setting the MAIN POWER SWITCH to ON changes the clear lamp indication to green. The BEAM SWITCH indicator lights red. With the MAIN POWER SWITCH on, -12v (B) is applied to the blower shut down circuit of time delay control 3A5. A gating circuit in time delay control 3A5 is enabled allowing 115 vac to pass to circuit breakers 3A9A1CB3, CB4, and CB5. The 115 vac is applied through KLYSTRON BLOWER circuit breaker 3A9A1CB3 to operate the klystron's main blower motor 3A9B1 and through CABINET FANS circuit breaker 3A9A1CB5 to operate cabinet blower motors 3A9B2 through 3A9B5 and blower motor 3A8B1 in inverter assembly 3A8. The 115 vac is also applied through CONTROL POWER circuit breaker 3A9A1CB4 and transformer 3A9T1 to operate power supply control 3A7 and the +28v power supply circuits. Control power supply 3A7 provides +7.5v, -7.5v, and -12v (A) outputs. The +7.5v, -7.5v, and -12v (A) outputs are the operating and control voltages for the power amplifier modules. The -12v (A) output is also applied to main power relay 3A9K1 and to the alarm indicators on the meter panel.

(2) With the MAIN POWER SWITCH in the ON position, 115 vac is also applied through contacts of filament relay 3A9K3 to the filament supply circuit which provides 6.4 vac to the klystron filament. Filament sensing transformer 3A9T4 samples the filament current and provides an input to the beam delay circuit of time delay control module 3A5. The beam delay circuit provides a minimum time-delay of 3.5 minutes after the filament sensing signal is received. After the 3.5 minutes have elapsed, the beam delay circuit provides an enable signal (time-delay signal) to beam gate dc overload control 3A6. This signal enables the application of beam voltage to the klystron when all other operating conditions are normal.

(3) The beam gate dc overload control 3A6 is essentially an AND gate which controls application of primary power (230 vac) to the high voltage power supply and also controls the operation of inverter regulator control module 3A1. In addition to the time-delay signal, the beam gate dc overload control receives control signals from various circuits in the power amplifier. All of the control signals must be normal to operate the high voltage power supply. When any of the control signals are not normal the high voltage power supply is disabled. One of the control signals for the beam gate de overload module is applied through BEAM SWITCH 3A9A31S4. After the filament time-delay has elapsed, the time-delay control signal is normal, as indicated by a green TIME DELAY indication on the meter panel. The BEAM SWITCH is then energized, and when set to the ON position changes from red to green. With the BEAM SWITCH on, the beam switch control signal is normal and the beam gate is enabled providing that the remaining inputs to the beam and gate are normal. The remaining six inputs to the AND gate are listed below with their normal conditions.

(a) The air control signal is normal when the klystron temperature is normal, the external waveguide interlock is closed, and the CABINET FANS circuit breaker is in the ON position.

(b) The ac overload control signal is normal when BEAM POWER circuit breaker is not tripped.

(c) The de overload control signal is normal if the beam current (output of high voltage power supply) is 550 milliamperes or less.

(d) The antenna mismatch control signal is received from module 3A4 and is normal if the power amplifier's reflected power is less than 100 watts (nominal).

(e) The interlock control signal is normal when the power amplifier door interlocks are closed.

(f) In addition to the input control signals described above, a -7.5v signal from power supply control 3A7 and -7.5v through RESET switch 3A9S3 are applied to the beam AND gate and must be present for normal operating conditions.

(4) When all inputs to the beam gate de overload module are normal, main power relay 3A9K1 becomes energized and the beam gate output enables inverter regulator control 3A1. With relay 3A9K1 energized and BEAM POWER circuit breaker 3A9A1CB2 in the ON position, 230 vac is applied to the high voltage power supply circuits. With inverter regulator control module enabled, trigger pulses (25 Hz to 3; 3 kHz)are applied to control the high voltage power supply. An inverter control signal is fed back to module 3A1 from the high voltage supply to regulate the ac control signal. The high voltage power supply will now provide a nominal beam voltage of 7,500 volts to the klystron.

c. Power Control Using MAIN POWER

SWITCH or BEAM SWITCH. Once power has been applied as described in b above, the power amplifier can be turned off and turned on again using the MAIN POWER SWITCH or the BEAM SWITCH. If the MAIN POWER SWITCH is used to turn off the power amplifier, an automatic time-delay of 3.5 minutes is required before it can be turned on again. If the BEAM SWITCH is used to turn off the power amplifier, it can be turned on again immediately. For normal shutdown, it is recommended that the BEAM SWITCH be set to OFF first, and then set the MAIN POWER SWITCH to OFF. This prevents the beam from coming on inadvertently the next time the MAIN POWER SWITCH is pushed.

d. Alarm Monitor Circuits. The necessary power amplifier functions are monitored at the power amplifier meter panel. The lower RF-mismatch, alarm and control module (3A4) monitors the output of the power amplifier for low RF and antenna mismatch conditions. The antenna mismatch is monitored and applied to the beam gate-dc overload control (3A6) along with the other control signals (b above) to control the beam gate. The beam gate output signal is fed back to the lo--RF-mismatch, alarm and control module. If the beam gate becomes disabled or if the RF output drops below 500 watts, the power amplifier alarm signal is enabled. Also, indicator control modules (3A2 and 3A3) monitor certain signals and control status indicators on the meter panel. Indicator control module 3A2 monitors the low RF, beam gate, filament, and air control signals. Indicator control module 3A3 monitors the antenna mismatch, ac overload, ac interlock, dc overload, and time-delay control signals. For normal conditions, the indicators light green. For alarm conditions, the indicators (except TIME DELAY indicator) light red. The TIME DELAY indicator lights amber when the time-delay is in process before beam voltage turn on and lights green when the time-delay is completed.

1-115. Power Amplifier Module Block Diagram Description
(fig. 8-68)

The functional relationships between all power amplifier modules and circuits are shown in figure 8-68. Each module is functionalized and the signal paths through the modules are shown. All circuit breakers are shown in the ON positions for normal operation. The MAIN POWER SWITCH and the BEAM SWITCH indicators are on and lighted green.

a. Primary Power. Single phase 230 vac primary input power is applied through line filters 3A9A8FL1 and FL3 to MAIN POWER circuit breaker 3A9A1CB1. Neutral is connected through line filter 3A9A8FL2 and is not grounded locally. The 230 vac (line to line) input powerlines are applied to the high voltage power supply circuits through contacts of beam power relay 3A9K1 and BEAM POWER circuit breaker 3A9A1CB2. One 115 vac (line to neutral) input powerline is applied to the -12v (B) power supply circuit and to contacts of MAIN POWER SWITCH 3A9A32S5. The other 115 vac (line to neutral) input powerline passes through gate Q3 in time delay control 3A5 and is distributed as follows:

(1) Through CONTROL POWER circuit breaker 3A9A1CB4 and step-down transformer 3A9T1 to operate the +28v power supply circuit and power supply control 3A7.

(2) Through KLYSTRON BLOWER circuit breaker 3A9A1CB3 to operate main blower motor 3A9B1.

(3) Through CABINET FANS circuit breaker 3A9A1CB5 to operate cabinet blower motors 3A9B2 through 3A9B5 and blower motor 3A8B1 which is part of inverter 3A8.

b. Dc Power Supplies. There are three separate dc power supplies in the power amplifier. Power supply control module 3A7 provides the operating and control voltages for most of the modules. The -12v (B) power supply provides the voltage which is applied to the MAIN POWER SWITCH and is required to turn on the power amplifier. The +28v power supply provides an operating voltage for inverter regulator control 3A1.

(1) Full-wave bridge rectifier CR3-CR6 in power. supply control 3A7 receives an input of 28.5 vrms from step-down transformer 3A9T1. The rectified output is applied to regulator circuits Q1, CR7-CR9 which produce regulated +7.5v and -7.5v outputs. Each output is connected to an external (cabinet mounted) capacitor filter. The 4-7.5v output provides operating voltage for modules 3A2, 3A3, 3A4, and 3A6. The -7.5v output provides operating voltage for modules 3A1, and 3A4 through 3A6. The -7.5v output also provides control voltage for switches (MAIN POWER SWITCH, BEAM SWITCH, RESET), auxiliary contacts of the BEAM POWER circuit breaker, and the door interlocks. The 28.5 vrms input to power supply control 3A7 is also applied to rectifier CR1, CR2 which produces -12v (A) output. The -12v (A) output is unfiltered and provides operating voltage for modules

3A4 and 3A6, main power relay 3A9K1, and the alarm indicators.

(2) The -12v (B) power supply is comprised of indicating fuse 3A9F1, transformer 3A9T2, and full-wave bridge rectifier 3A9CR8 (4-diode bridge rectifier package). The 12 vrms input is applied to the bridge rectifier through step-down transformer 3A9T2. The -12v (B) output is applied to a section of the MAIN POWER SWITCH. When the MAIN POWER SWITCH is turned on, the -12v (B) voltage energizes relay K1 in time-delay control 3A5. With K1 energized, gate Q3 in module 3A5 is enabled and passes 115 vac for operation of power supply control 3A7, the +28v power supply, and the blower motors. The MAIN POWER SWITCH indicator lights green for the ON position. In addition, -12v (B) is applied to the BEAM SWITCH through the closed contacts of the MAIN POWER SWITCH. The BEAM SWITCH indicator lights red for BEAM SWITCH OFF and lights green for the BEAM SWITCH ON. When the MAIN POWER SWITCH is turned off, the indicator lights white and the -12v (B) voltage is removed from the time-delay control module 3A5 and the BEAM SWITCH.

(3) The +28v power supply is comprised of full-wave bridge rectifier 3A9A21CR2 (4-diode bridge rectifier package) and regulator circuit 3A9A21CR1, C3, and R1. The full-wave rectifier receives a 28.0 vrms input from step-down transformer 3A9T1. The rectifier output is regulated at +28v and is applied to the inverter regulator control 3A1.

c. Filament Supply Circuit. When the MAIN POWER SWITCH is placed in the ON position, the filament 115 vac supply circuit is energized through contacts of filament voltage relay 3A9K3. In order for relay 3A9K3 to be energized, the AIR indicator on the meter panel must be lighted green (normal condition). For this condition, -7.5v is applied to the relay through klystron thermal switch 3A9V1S2, through P-16B to P16E (interlock), and through closed auxiliary contacts of the CABINET FANS circuit breaker 3A9A1CB5. If the thermal switch detects excessive klystron heat, or the waveguide interlock is not closed, or the CABINET FANS circuit breaker is tripped, the 115 vac input to the filament supply is removed and the AIR indication changes from green to red (alarm condition). For the normal condition, 115 vac is applied to the filament supply circuit which is comprised of FILAMENT RUNNING TIME meter 3A9M1, current-limiting resistors 3A9R4, R6, and R8, meter resistors R5 and R7, FILAMENT VOLTAGE meter 3A9M2, voltage regulator 3A9CR10 and CR11, and step-down transformer 3A9T3.

(1) Meter 3A9M1 registers the filament running time in hours and tenths of hours.

(2) The current limiting resistors limit the current in the filament supply circuit during turn-on when the klystron filament is cold. Resistors 3A9R4 and 3A9R6 are variable.

(3) The meter resistors are in series with meter 3A9M2 and provide the voltage drop to permit appropriate meter indication. Resistor 3A9R5 is variable and is used to calibrate the meter.

(4) Meter 3A9M2 monitors the filament voltage and is calibrated at 6.4 vac.

(5) The voltage regulator consists of two Zener diodes connected across the primary of step-down transformer 3A9T3. The diodes provide an input of 42 vrms to the step-down transformer.

(6) Step-down transformer 3A9T3 provides an output of 6.4 vac which is applied to the klystron filament. Filament voltage sensing circuit 3A9T4, R9 senses the filament voltage and provides an input to time-delay control module 3A5.

d. Beam Time-Delay Circuit. The beam time-delay circuit is part of time-delay control module 3A5. The input to the circuit is received from the filament voltage sensing circuit which consists of filament current sensing transformer 3A9T4 and resistor 3A9R9. The ac voltage across resistor 3A9R9 is applied to bridge rectifier CR9-CR6 of the beam time-delay circuit. The ac voltage (approximately 2.5 vac) is rectified and applied to filament sensing gate Q4, Q5. When this gate is enabled, the beam turn-on time-delay is started. The time-delay is determined by the beam time delay gate (Q6, Q7). The BEAM TD control R11 is adjusted for a time-delay of 3.5 minutes. The TIME DELAY indicator on the meter panel lights amber when the time-delay is in process. After the 3.5 minutes have elapsed, the TIME DELAY indicator changes from amber to green and the beam -ate and dc overload control module 3A6 is enabled. The FILAMENT indicator on the meter panel lights red when the filament sensing voltage is less than 2.5 vac and lights green when 2.5 vac (filament current sensed) is present and a signal is applied to energize the beam time-delay circuit.

e. Beam Gate-Dc Overload Control 3A6. Beam gate dc overload control 3A6 controls the application of 230 vac primary power to the high voltage

power supply and operation of inverter regulator control module 3A1. Module 3A6 is functionally comprised of a beam AND gate, beam gate driver Q1, Q2, relay driver Q3, Q4, and dc overload trigger Q5, Q6.

(1) Enabling the beam AND gate is depended upon eight normal input control signals. In addition to the beam time-delay input described in d above, the following control signals must be present.

(a) The ac overload control signal (-7.5v) is present when BEAM POWER circuit breaker 3A9A1CB2 is ON, and -7.5v is applied through the circuit breaker to the AND gate. The AC OVERLOAD indicator on the meter panel is lighted green for this condition. If the BEAM POWER circuit breaker trips, the beam gate is disabled and the AC OVERLOAD indicator changes from green (normal) to red (alarm).

(b) The air control signal (-7.5v) is present when the klystron temperature is not excessive, the external waveguide interlock is closed, and CABINET FANS circuit breaker 3A9A1CB5 is ON. -7.5v is applied to the AND gate via klystron thermal switch 3A9V1S2, the P16 interlock, and auxiliary contacts of the CABINET FANS circuit breaker. Also, for this condition, the AIR indicator is lighted green and filament voltage relay 3A9K3 is energized. If the thermal switch, P16 interlock, or CABINET FANS circuit breaker are not closed, the beam gate is disabled, the filament voltage relay is deenergized, and the AIR indication on the meter panel changes from green (normal) to red (alarm).

(c) The beam switch on control signal (-7.5v) is present when the BEAM SWITCH is in the ON position and -7.5v is applied to the AND gate through closed contacts of the BEAM SWITCH. The BEAM SWITCH indicator is lighted green for this condition. If the BEAM SWITCH is set to the OFF position, the beam gate is disabled and the switch indicator changes from green to red.

(d) The antenna mismatch control signal (-7.5v) is present when the power amplifier's reflected power is less than 100 watts. The antenna mismatch control signal is received from low RF-mismatch, alarm and control module 3A4 and applied to the AND gate. The ANTENNA MISMATCH indicator on the meter panel is lighted green for this condition. If the reflected power is 100 watts or more, the beam gate is disabled and the ANTENNA MISMATCH indication changes from green (normal) to red (alarm).

(e) The -7.5v control signal is applied directly to the AND gate from power supply control 3A7. If the -7.5v power supply output fails, the beam gate is disabled.

(f) The ac interlock control signal (-7.5v) is present when the cabinet interlocks are closed. This applied -7.5v to the AND gate via closed contacts of cabinet interlock switches 3A9S6 (high voltage ground and interlock switch), 3A9S7 (ac interlock switch), and 3A9S9 (fan/ac interlock switch). The AC INTERLOCK indicator on the meter panel is lighted green for this condition. If the interlock switches are not closed, the beam gate is disabled and the AC INTERLOCK indication changes from green (normal) to red (alarm).

(g) The dc overload control signal -7.5v) is applied to the AND gate when the beam current (output of high voltage power supply) is 550 milliamperes or less. A calibrated sample of the beam current is applied to dc overload trigger Q5, Q6 in module 3A6. Normally, the sampled current is not sufficient to trigger the dc overload circuit. For this condition, the beam AND gate is enabled and the DC OVERLOAD indicator on the meter panel is lighted green. For an alarm condition, the sampled current is sufficient (3.5 to 4.0 vdc) to enable the trigger circuit causing the beam gate to be disabled and the DC OVERLOAD indication to change from green (normal) to red (alarm). The DC OVLD ADJ control establishes the input level to the dc overload trigger circuit (Q5, Q6) causing it to operate when the input rises above 3.5 vdc. A rise above 3.5 vdc at the input of the trigger circuit occurs when the beam current rises about 550 milliamperes. Once the dc overload alarm condition has been corrected, the dc overload trigger circuit must be disabled. Depressing the RESET switch, removes -7.5v operating voltage and disables the circuit.

(2) When all eight inputs to the AND gate are present as described above, beam gate driver Q1, Q2 provides a -7.5v output which is applied to the BEAM indicator on the meter panel, inverter regulator control module 3A1, and low RF-mismatch, alarm and control module 3A4. For this condition, the BEAM SWITCH indicator is lighted green, the circuits in inverter regulator control module 3A1 are enabled, and the beam gate signal applied to the low RF-mismatch, alarm and control circuits inhibits the power amplifier alarm output. Also, when all eight inputs to the. AND gate are present, relay driver circuit Q3, Q4 provides the return path to energize main power relay 3A9K1. With relay 3A9K1 energized,

230 vac primary input power is applied to the high voltage power supply and the external preheater circuit is disabled. The external preheater is used to supply hot air through the power amplifier input air duct for initial warmup during very cold weather (less than zero degrees Fahrenheit). If any of the inputs to the AND gate are removed, the return path to energize relay 3A9K1 is removed. With relay 3A9K1 deenergized, the 230 vac primary input power to the high voltage power supply is removed and the external preheater circuit is enabled. With the beam AND gate disabled, the BEAM indication changes from green (normal) 'to red (alarm), inverter regulator control 3A1 is disabled, and circuits in low RF mismatch, alarm and control module 3A4 enable the power amplifier summary alarm signal. Consequently, the beam voltage is removed from the klystron and the CNTRL ALARM indicator on the transmitter meter panel lights red to indicate an alarm condition in the power amplifier.

f. Low RF-Mismatch, Alarm and Control 3A4. The low RF-mismatch, alarm and control module monitors the status of the beam gate and the forward and reflected power outputs of the power amplifier. The beam gate control signal is fed back from module 3A6 to AND gate CR2, CR3 in module 3A4 and indicates the status (on or off) of the beam gate in module 3A6. The low RF control signal is a sample of the power amplifier's forward output power and is fed back to low RF trigger circuit Q1 in module 3A4 through diode detector 3A9CR15, filter 3A9FL7, and output directional coupler 3A9DC2. The antenna mismatch control signal is a sample of the power amplifier's reflected power output and is fed back to mismatch amplifier Q6 and Q7 in module 3A4 through diode detector 3A9CR14, filter 3A9FL4, and output direction coupler 3A9DC2. Output directional coupler 3A9DC2 provides samples of the output power. The forward power sample is 50 db below the actual forward power and the reflected power sample is 36 db below the actual reflected power.

(1) The detected low RF control signal is applied to low RF trigger circuit Q1, Q2. For normal conditions (forward output power is greater than 500 watts), the control signal is of sufficient amplitude (-1.0 vdc) to turn on the trigger circuit. The LOW RF control adjusts the trigger circuit to operate when the forward output power is greater than 500 watts or any other preset value. With the trigger circuit turned on, the LOW RF indicator is lighted green and transistor switch Q3 is turned on applying -7.5v to AND gate CR2, CR3. The other input to the AND gate is the beam gate control signal which is also -7.5v for normal conditions. With both inputs to the AND gate normal (-7.5v), -7.5v is applied through OR gate CR4, CR7 to relay control circuit Q4, Q5. With -7.5v applied to the relay control circuit, relay K1 is energized (normal condition) and the power amplifier alarm signal is disabled. If either of the -7.5v inputs to the AND gate is removed, the -7.5v input to the relay control circuit is removed and relay K1 becomes deenergized (alarm condition). With K1 deenergized, ground is applied to the power amplifier alarm output line causing the CNTRL ALARM indicator on the transmitter meter panel to light red (alarm condition). The -7.5v beam gate input to the AND gate is removed if the beam gate becomes disabled as described in e above. With the beam gate disabled, the BEAM indicator on the power amplifier meter panel is also lighted red. The -7.5v low RF input to the AND gate is removed when the power amplifier forward output power drops below 500 watts (trip point is nominally 500 watts but may be set to other values). For this condition, low RF trigger Q1, Q2 is disabled turning off transistor switch Q3. Consequently, the -7.5v low RF input to the AND gate is removed. The low RF alarm condition will cause a red LOW RF indication on the power amplifier meter panel in addition to the red CNTRL ALARM indication on the transmitter meter panel. The other input to OR gate CR4, CR7 is from the BEAM SWITCH. When the BEAM SWITCH is in the OFF position (power amplifier not in use) -7.5v is applied through the OR gate to the relay control circuit causing relay K1 to be energized. Consequently, the power amplifier's summary alarm signal is disabled when the BEAM SWITCH is in the OFF position.

(2) The antenna mismatch control signal is applied to mismatch trigger circuit Q6, Q7. For normal conditions (reflected power is less than 100 watts), the control signal (generated by the detected RF) is not of sufficient amplitude to turn on the mismatch trigger circuit. With the trigger circuit turned off, mismatch driver Q8 provides an output of -7.5v which is applied to antenna mismatch indicator driver Q5, Q6 on indicator control 3A3 and to beam gate dc overload control 3A6. For this condition, the ANTENNA MISMATCH indicator is lighted green and the beam'" gate is enabled. For an alarm condition (reflected power is 100 watts or more), the antenna mismatch control signal is of sufficient amplitude (-1.0 to

-1.3 vdc) to turn on the mismatch trigger circuit. The ANT. MIS. control adjusts the trigcircuit to operate when the reflected power is 100 watts. With the trigger circuit turned on, mismatch driver Q8 provides an output of 0 volt causing the ANTENNA MISMATCH indication to change from green (normal) to red (alarm) and disabling the beam gate in module 3A6. As previously described, the disabled beam gate control signal is fed back to module 3A4 and enables the power amplifier summary alarm output line (CENTRL ALARMS indicator on transmitter meter panel lights red). Once the antenna mismatch alarm condition has been corrected (reflected power is less than 100 watts), the mismatch trigger circuit must be disabled. Depressing the RESET switch, on the power amplifier meter panel removes -7.5v operating voltage and disables the circuit.

g. Inverter Regulator Control Module 3A1. The inverter regulator control provides the trigger pulses (25Hz to 3. 3kHz) required to operate the high voltage power supply. The trigger pulses enable SCR's Q1-Q4 in the dc-to-ac converter circuit of inverter module 3A8. The pulses are produced by bistable multivibrator circuit Q9, Q10 in inverter regulator control 3A1. The multivibrator is controlled by the beam gate control signal (-7.5v) from module 3A6 and inverter feedback control signal (0 to -5v) which is a sample of the high voltage power supply output.

(1) The beam gate control signal is applied to relay control circuit Q1, Q4 in module 3A1. For normal conditions, the control signal level is -7.5v causing the relay control circuit to energize relay K1. There is a time-delay of approximately 1.5 second from application of the beam gate control signal until relay K1 becomes energized. With relay K1 energized, +28v is removed from the input of frequency control circuit Q5 and applied to pulse gate circuit Q7, Q8 allowing trigger pulses to be applied to bistable multivibrator Q9, Q10.

(2) The inverter feedback control signal (0 to -5v) is applied to amplifier comparator circuit Q3. The amplifier comparator circuit receives the inverter control signal and compares it with a positive input from reference circuit Q2. The BEAM VOLT ADJ control is used to adjust the positive reference input to the amplifier comparator. When the combined input goes more positive, the comparator transistor conducts more, and when the combined input goes less positive, the comparator transistor conducts less. The output of the comparator controls the operation of frequency control circuit Q5 which determines the frequency of the pulses produced by pulse generator Q6. The pulse generator output is applied to pulse gate Q7, Q8 which triggers bistable multivibrator Q9, Q10. The frequency of the bistable multivibrator outputs are applied to balanced amplifier circuits. One multivibrator output is applied through transformer T1 and amplifier circuit Q11, Q13 to output transformer T3. The other multivibrator output is applied through transformer T2 and amplifier Q12, Q14 to output transformer T4. The amplifiers provide output pulses (25 Hz to 3.3 kHz) with a minimum peak amplitude of 10 volts. Each output transformer (T3 and T4) provides two output pulses which trigger SCR's in the dc-to-ac converter circuits of the high voltage power supply.

(3) As stated previously, the frequency of the output pulses is determined by the inverter control input signal and the setting of the BEAM VOLT ADJ control. Output pulses at 3, 3 kHz rate are provided when the amplitude of the inverter feedback control signal is 0 volt. Output pulses at a 25 Hz rate are provided when the BEAM VOLT ADJ control is set at midrange and the amplitude of the inverter feedback control signal is -5 vdc. The circuit response time is slow. A change in output frequency will take place 3 seconds (minimum) after a change in inverter control signal amplitude.

h. High Voltage Power Supply. The high voltage power supply provides the beam voltage (7,500 volts) for the klystron. The 230 vac primary power is applied to the high voltage power supply through line filters 3A9A8FL1, FL2, FL3, the MAIN POWER circuit breaker, contacts of main power relay 3A9K1, and the BEAM POWER circuit breaker 3A9A1CB2.

(1) The 230 vac input is rectified by fullwave bridge rectifier CR5-CR8 in inverter module 3A8. The rectified output (200 volts nominal) is applied through a filter circuit 3A9A1L1, L2, C1-C3 and an overload protection circuit to a dc-to-ac converter circuit in inverter module 3A8. The overload protect circuit is comprised of overload sensor circuit Q1, overload trigger circuit Q2, and overload gate Q3. When an overload condition is sensed by circuit Q1, the overload trigger circuit enables the overload gate. The overload gate becomes a short circuit and causes the BEAM POWER circuit breaker to trip removing the 230 vac primary power input to the high voltage power supply.

(2) The filtered 200 vdc output of the fullwave bridge rectifier is applied across the dc-to-ac converter. Four trigger pulse (25 Hz to 3.3 kHz) from inverter control regulator 3A1 are applied to SCR's Q1 through Q4 in the dc-to-ac converter. The pulses trigger the SCR's at 25Hz to 3.3kHz) frequency rate. The resulting output of the dc-to-ac converter is 200 vrms single phase (25 Hz to 3.3 kHz) which is applied to step-up transformer 3A9A1T2. The voltage is stepped up to 9,000 vac and applied to full-wave rectifier 3A9A33CR4 (4 diode, full-wave rectifier package). The rectified kV output (7,500 volts) is applied to a filter circuit 3A9A33L1 and 3A9A33C7. Resistor 3A9A33A1R20 and capacitors 3A9A33A1C14, 3A9A33A1C15, and 3A9A33A1C16 form an RC integrating filter. The filtered high voltage output of the full-wave bridge rectifier appears across capacitor 3A9A33C7.

(3) The +HV output leg of the high voltage power supply is applied to the BEAM CURRENT meter 3A9M4 through a metering circuit for monitoring. The BEAM I CAL control in the metering circuit is. used to calibrate the meter for 0.55-amp midscale reading. The dc overload control signal is fed back from the metering circuit and is applied to dc overload trigger circuit Q5, Q6 in module 3A6.

(4) The -Hv output leg of the high voltage power supply is applied to the BEAM VOLTAGE meter 3A9M3 and metering circuit for monitoring. The inverter feedback control signal (0 to 5V), developed across resistor 3A9A23R15, in metering circuit is applied to amplifier comparator circuit Q3 in module 3A1. The -HV output leg is also connected to the high voltage ground and interlock switch 3A9S6. Interlock switch 3A9S6 is gravity actuated and is controlled by the red door located between modules 3A5 and 3A6. When the door is initially opened, the ac interlock control signal path through one section of 3A9S6 is opened. When the door is fully opened, ground is applied through the other section of 3A9S6 to discharge the capacitors in the HV output. Consequently, interlock switch 3A9S6 turns off the high voltage power supply before grounding the HV output. Also, with 3A9S6 opened, the AC INTERLOCK indication on the meter panel changes from green to red. When either the ac interlock switch 3A9S7 or fan/ac interlock switch 3A9S9 is opened, the high voltage power supply is also turned off and the AC INTERLOCK indicator lights red. Neither 3A9S7 nor 3A9S9, however, grounds the HV output.

i. RF Circuits. The 4.4 to 5.0-GHz RF input signal from the transmitter is applied to the first cavity of klystron 3A9V1 through variable attenuator (0 to 30 db) 3A9AT1 and input directional coupler 3A9DC1. The -tunable four cavity klystron provides a power amplifier output of 1 kilowatt with a 40-milliwatt RF input applied to the klystron. The 40-milliwatt klystron input is obtained by adjusting variable attenuator 3A9AT1. Main tuning of the klystron is accomplished by setting the MAIN TUNING 1ST CAVITY control to the desired frequency within the 4.4 to 5.0-GHz band as indicated on the FREQUENCY GHZ dial. Fine tuning is accomplished by using the FINE TUNING 2ND CAVITY, 3RD CAVITY, and 4TH CAVITY controls. The klystron RF output is applied to the external waveguide switch through output directional coupler 3A9DC2 and harmonic filter 3A9FL8. Harmonics of the desired RF signal (4.4 to 5.0 GHz) produced in the klystron are rejected by the harmonic filter. The filter provides 50 db 2d harmonic rejection, 30 db 3d harmonic rejection, and 20 db 4th harmonic rejection.

(1) A sample of the RF input signal (20 db down from the main line RF input signal) is derived from the input directional coupler through diode detector 3A9CR13 for application to meter circuit (3A9A23R19, C13). Level adjustment is provided by input variable attenuator 3A9AT1. The RF input signal is applied to RF MONITOR meter 3A9M8 by depressing the INPUT FORWARD MILLIWATT pushbutton switch (P/O 3A9S8) on the meter panel. With the input level properly adjusted, the meter should indicate 40 milliwatts RF input power.

(2) A sample of the forward power output signal is derived from the output directional coupler through filter 3A9FL6 to diode detector 3A9R17 for application to meter calibration circuit 3A9A23R17 and C11. The OUT FWD control is used to calibrate the meter. The for

ward power signal is applied to the RF MONITOR meter by depressing the ANTENNA FORWARD WATTS X10 pushbutton switch (P/O 3A9S8) on the meter panel. The output directional coupler also selects a portion of the forward output power signal through filter 3A9FL7 to diode rectifier 3A9CR15. The rectified signal, designated "low RF," is fed back to control the low RF trigger circuit Q1, Q2 in module 3A4. The low RF control signal indicates an alarm condition when the forward RF power drops below a preset level.

(3) A sample of the reflected power signal is derived from the output directional coupler through filter 3A9FL4 to rectifier diode 3A9CR14 for application to meter calibration circuit (3A9A23R18 and C12). The OUT REFL control is used to calibrate the meter. The reflected power signal is applied to the RF MONITOR meter by depressing the ANTENNA REFLECTED WATTS pushbutton switch (P/O 3A9S8) on the meter panel. The meter should indicate less than 100 watts of reflected power. Also, the output of diode detector 3A9CR14 designated antenna mismatch, is fed back to control the mismatch trigger circuit Q6, Q7 in module 3A4. The antenna mismatch control signal disables the beam gate (removing beam, voltage) and indicates an alarm condition when the reflected power rises to 100 watts.

j. Power Turnoff and Blower Shutdown. *The* BEAM SWITCH and the MAIN POWER SWITCH are used during routine operation to turn off the power amplifier. The BEAM SWITCH is turned off first. Setting the BEAM SWITCH to the OFF position (BEAM SWITCH indicator changes from green to red) disables the beam gate causing the beam voltage to be removed from the klystron. Also, the BEAM indicator on the power amplifier meter panel changes from green to red and the power amplifier summary alarm is enabled causing the CENTRL ALARM indicator on the transmitter meter panel to light red and the audible alarm to sound. Setting the MAIN POWER SWITCH to the OFF position causes the MAIN POWER SWITCH indicator to change from green to white and the BEAM SWITCH indicator to extinguish. With the MAIN POWER SWITCH off, the 115 vac input to the filament supply, and the -7.5v and -12v (B) inputs to the time-delay control module (3A5) are switched off.

(1) With the 115 vac input to the filament supply removed, the klystron filament is shut off.

(2) With the filament sensing voltage and -12v(B) operating voltage removed from time-delay control module 3A5, the FILAMENT indication changes from green to red and the TIME DELAY indicator changes from green to amber.

(3) With the MAIN POWER SWITCH off, the -7.5v and -12v (B) inputs to the blower shutdown portion of module 3A5 are removed, however, -7.5v from power supply control 3A7 is applied to blower shutdown circuit Q1, Q2 and OR gate CR4, CR5 in module 3A5. The -7.5v OR gate input keeps relay 3A5K1 energized, thus keeping the blower motors (3 A9B1 through 3A9B5 and 3A8B1), power supply control 3A7, and the +28v power supply in operation. The blower motors, power supply control, and the +28v power supply will continue to operate for 3.5 minutes after the MAIN POWER SWITCH has been turned off. After 3.5 minutes have elapsed, 'blower shutdown circuit Q1, Q2 will deenergize relay K1 causing gate Q3 to be disabled. With gate Q3 disabled, the 115 vac input power is removed and the blower motors, power supply control, and 28v power supply are turned off.

(4) With the power supply control and the +28v power supply turned off, all dc voltages (except -12v (B)) are removed. For this condition, all power amplifier indicators (except MAIN POWER SWITCH indicator) are extinguished. The MAIN POWER SWITCH indicator will stay lighted.

1-116. Module Circuit Theory

The power amplifier module circuit theory descriptions are provided in paragraphs 1-117 through 1-123. Module circuit theory descriptions appear in sequential reference designation order and are at the schematic diagram level. The high voltage power supply circuit theory description (para 1-123) covers inverter 3A8, HV power supply 3A9A1, and certain cabinet mounted components. The circuit theory descriptions for all other cabinet mounted components are provided at the block diagram level (para 1-115). The power amplifier interconnecting diagram (fig. 8-69) illustrates all cabinet mounted components, cabinet wiring, and module interconnections.

1-117. Inverter Regulator Control 3A1 Circuit Theory (fig. 8-70)

Inverter regulator control 3A1 provides 25Hzto 3.3 kHz trigger pulses for gating the high power

silicon controlled rectifiers in inverter 3A8. The trigger pulses are required to generate the beam voltage. The repetition rate of the trigger pulses can be adjusted manually at module 3A1 which causes the beam voltage to vary. Module 3A1 also provides regulation by sampling the beam voltage and changing the repetition rate of the trigger pulses to keep the beam voltage constant. The module is in operation only when the beam gate is turned on (beam voltage is applied to the klystron). When the beam gate is turned off, the module is disabled and the triggering pulses are turned off. Circuit operation when the beam gate is turned on and when the beam gate is turned off are described in*a* and *b* below.

a. Beam-On Condition. When the beam gate is turned on, -7.5v is applied to pin B and through filter FL4 to diode CR1. Diode CR1 cuts off and I capacitor C1 starts to charge. It takes approximately 1.5 second for C1 to charge to the level required to turn on Q1. This delay allows ac to be applied to the high voltage power supply before the triggering pulses are generated. Capacitor C1 charges to -4.5v, diode CR2 breaks down and conducts through the base of Q1. Q1 conducts causing Q4 to conduct since the base of Q4 goes towards ground potential. With Q4 conducting, relay K1 becomes energized removing +28v from the gate of Q5 allowing Q5 to conduct through R10 and comparator transistor Q3. In addition, 28v is applied across voltage divider R18, R20. Approximately 23 volts is applied to the gate of SCR Q8 enabling Q8. With Q8 enabled, pulse gate Q7 draws current and pulses from pulse generator Q6 are amplified by Q7.

(1) The beam voltage generated in the high voltage power supply is controlled by a change in the repetition rate of the pulses generated by pulse generator Q6. The rate of the pulses generated is controlled by capacitor C3 and the effective resistance between the supply voltage and the gate input to Q6. Two resistance paths exist between the gate input to Q6 and the supply voltage. One of the resistance paths consists of resistor R15. The other resistance path includes fixed resistor R13, variable resistor R12 and the frequency control circuit (field effect transistor, FET, Q5). The lower the resistance to the gate input of Q6, the higher the frequency of the pulses generated. If variable resistor R12 is adjusted for less resistance, Q5 draws more current and the pulse rate is higher. Variable resistor R12 is adjusted to give a maximum rate of 3. 3kHz and fixed resistor R15 provide the minimum rate of 25 Hz.

(2) The 25Hz to 3.3kHz trigger pulses generated by Q6 are amplified by Q7 and applied through capacitors C5 and C6 to "steering" diodes CR6 and CR7. in the base circuits of bistable multivibrator transistors Q9 and Q10. If Q9 is conducting, Q10 is cut off. With Q10 cut off, +28v appears at the collector of Q10 and at the anode of CR6. The first negative pulse from pulse gate Q7 will pass through CR6 (CR7 is already back biased) to the base of Q9 causing Q9 to cut off. With Q9 cut off, the base of Q10 goes to a high potential through resistor R27 causing Q10 to conduct. The cycle repeats when the next pulse is applied which passes through CR7 and cut3 off Q10. Square waves from the bistable multivibrator are coupled through resistors R26 and R29 to the primary of transformers T1 and T2. Transformers T1 and T2 differentiate the pulses which are then applied to the base circuits of emitter followers Q11 and Q12. Resistors R31 and R32 are load resistors across the secondaries of transformers T1 and T2. The emitter follower outputs appear across load resistors R33 and R34. Diodes CR8 and CR9 allow only the positive pulses to pass to the bases of power amplifiers Q13 and Q14.The pulses generated by Q9, Q11, and Q13 are coupled to one pair of SCR's in inverter 3A8 through two output windings of transformer T3 and pins K,: L and pins P, N . The pulses generated by Q10, Q12, and Q14 are coupled to the other pair of SCR's in inverter 3A8 through two output windings of transformer T4 and pins V, U and pins S, R . First one circuit (i.e. Q9, Q11, Q13) is in operation and then the other. They never operate simultaneously. Resistors R37 through R40 provide a nominal loading of the circuits before the pulses leave module 3A1.

(3) Module 3A1 also regulates the beam voltage applied to the klystron. In order to do this a sample of the high voltage is fed back to the module and applied to pin D. The sampled voltage (0 to -5v) is applied to the base of amplifier comparator circuit transistor Q3. Resistors R3, R4 and R6 form an impedance matching pad. A positive voltage is provided at the base of Q3 by the reference circuit (FET transistor Q2). The positive reference voltage causes Q3 to conduct. BEAM VOLT ADJ potentiometer (R8) is used tc2 adjust the current flow through Q3. If the BEAM VOLT ADJ potentiometer is set for minimum resistance, Q3 draws more-current' and the collector of Q3 approaches "ground potential. When Q3 conducts more, the' frequency control circuit (FET transistor Q5) also conducts more and the pulse repetition rate is increased. With a sample

of the beam voltage applied to the base of Q3, regulation of beam voltage is achieved. *For example,* assume that the beam voltage increases because of instability (that is, line voltage increases). For this condition, the sampled voltage applied to the base of amplifier comparator Q3 goes more negative and causes Q3 to conduct less. This, in turn, results in less current flow in pulse generator Q6 which decreases the pulse repetition rate and reduces the rms value of the signal produced by inverter 3A8. Thus, regulation is accomplished.

b. Beam-Off Condition. When the beam gate is turned off, -7.5 volts is removed from pin B. The -7.5 volts at pin A causes current to flow through R2, CR1, and R1 resulting about 1volt across capacitor C1. As a breakdown voltage of 4.5 volts is required for diode CR2 cut off, thus inhibiting operation of the remaining circuits.

1-118. Indicator Control 3A2 and 3A3 Circuit Theory
(fig. 1-43)

Indicator control 3A2 and 3A3 monitor various signals and control the status indicators on the power amplifier meter panel. The modules contain identical circuits and are interchangeable. Indicator control module 3A2 monitors the low RF, beam gate, filament, and air control signals. Indicator control module 3A3 monitors the antenna mismatch, ac overload, dc overload, and time-delay control signals.

a. The indicator module contains five identical indicator driver circuits. Each indicator driver circuit is comprised of two transistors which control a status indicator on the power amplifier meter panel. The input transistor provides the ground return for the green lamp (normal) portion of the indicator. The output transistor provides the ground return for the red lamp (alarm) portion of the indicator. When one transistor is conducting (associated lamp is lighted), the other transistor is cut off (associated lamp is extinguished). Since all circuits are identical, the following description covers only the BEAM indicator control circuit (transistors Q1 and Q2) on indicator control module 3A2.

b. Assume that the beam gate is turned on (normal condition). For this condition, a negative voltage (approximately -7.5 volts) is applied to pin U. The negative voltage is sufficient to overcome the positive bias supplied by resistor R2, TM 11-5820-59535 causing transistor Q1 to conduct. With Q1 conducting, the ground return is applied to pin N causing the green lamp to light. The ground return also causes the base of Q2 to go positive and Q2 cuts off. With Q2 cut off, the ground return is removed from pin H causing the red lamp to go out.

c. Assume that the beam gate is turned off (alarm condition). For this condition, 0 volt (open circuit) is applied to pin U. The +7.5-volt bias applied to the base of Q2 through resistor R2 causes transistor Q1 to cut off. With Q1 cut off, the ground return is removed from pin N causing the green lamp to go out. The -12v supply for the green lamp is applied to the base of Q2 through the green lamp, pin N, and resistor R3. The -12 volts overcomes the +7.5 volts applied through resistor R4 and causes Q2 to conduct. With Q2 conducting, the ground return is applied to pin H causing the red lamp to light.

d. The status of the input signals to modules 3A2 and 3A3 can be determined at front panel test points TP1 through TP5 by noting the polarity of the voltage to ground at each point. If it is negative, the input transistor (green lamp) should be turned on. If it is positive, the output transistor (red lamp) should be turned on.

1-119. Low RF-Mismatch, Alarm and Control Module 3A4 Circuit Theory
(fig. 8-71)

The low RF-mismatch, alarm and control module continuously monitors the status of the beam gate and the forward and reflected power levels at the output of the power amplifier.

a. A sample of the forward RF power output is directed from output directional coupler 3A9DC2 and is rectified by a detecting diode. The rectified signal, designated "low RF," is applied to pin 17 of the low RF-mismatch, alarm and control module.

(1) Normally (forward output power greater than 500 watts), the low RF signal is of sufficient negative amplitude (-1.0 vdc) to causing transistor Q1 to conduct. Thermal resistor R1 and capacitor C1 form an integrator circuit at the input (base) of Q1. The integrator prevents instantaneous input changes from affecting circuit operation. LOW RF control potentiometer R2 controls the operating point of the circuit and is set so that transistor Q1 conducts when the forward power output is greater than 500 watts. With Q1 conducting, the gate input to silicon controlled

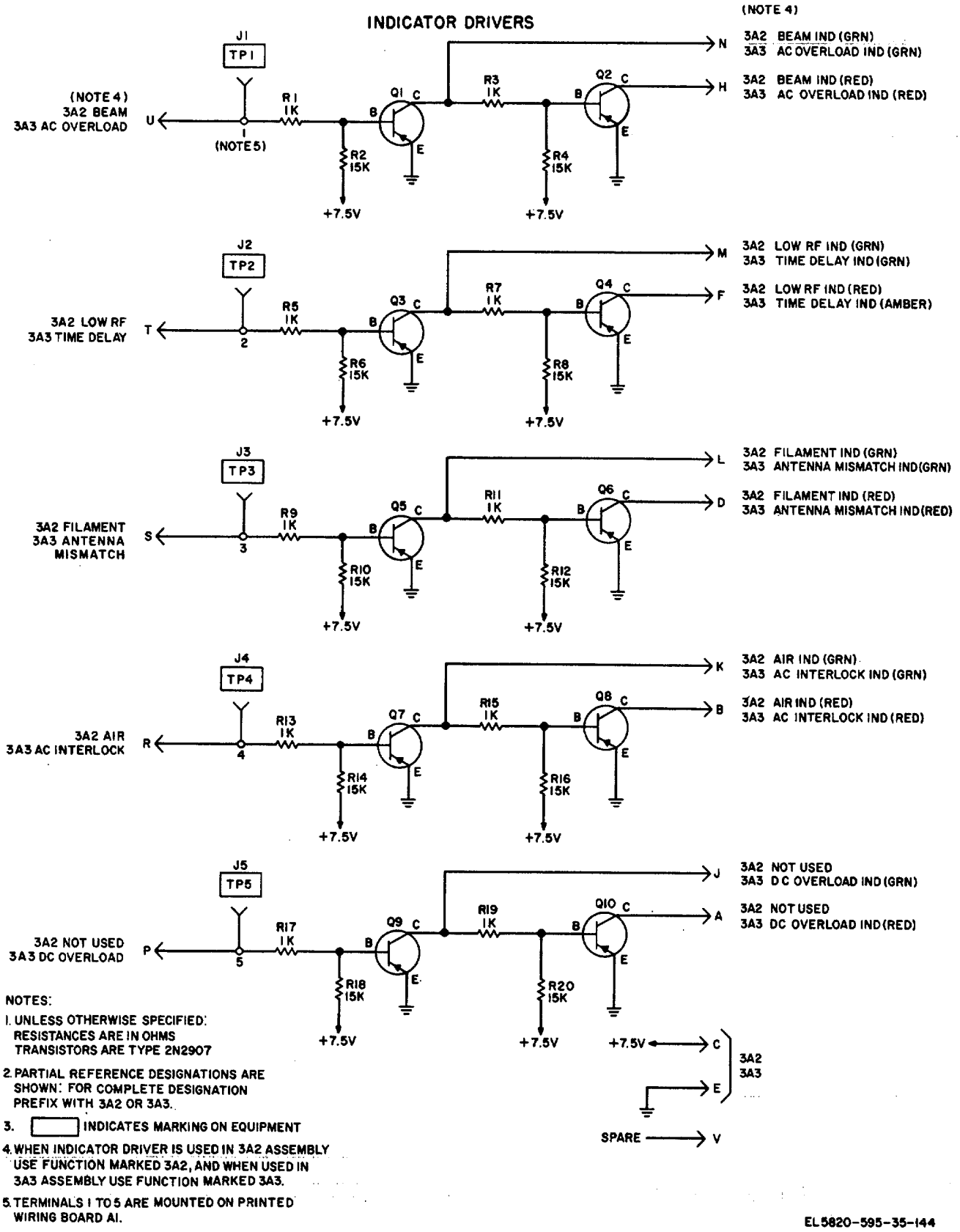


Figure 1-43. Indicator Control 3A2/3A3, schematic diagram.

rectifier (SCR) Q2 becomes less negative due to the voltage drop across resistors R3 and R4 causing Q2 to conduct. With Q2 conducting, the -12v (unfiltered) supply voltage appears across resistor R5 and is filtered by diode CR1, resistor R6, and capacitor C2. The resultant negative voltage across capacitor C2 is applied to indicator control 3A2 through pin V causing the LOW RF indication on the power amplifier meter panel to change from red to green. The negative voltage across C2 also biases transistor Q3 into conduction. With Q3 conducting, -7.5v is applied across resistor R9 which reverse biases diode CR3. For this condition, a negative voltage is applied through diodes CR4, CR5, and CR6 to the base of transistor Q4 biasing Q4 into conduction. With Q4 conducting the base of Q5 is at a less negative potential due to the voltage drop across resistors R10 and R12. This drives transistor Q5 into conduction and causes relay K1 to become energized. With relay K1 energized, external alarm output pins M and P are shorted through the relay contacts causing the external summary alarm circuit to be disabled (normal condition).

(2) For an alarm condition (forward power 500. watts or less), the low RF input signal becomes less negative causing transistor Q1 to cut off. With Q1 cut off, the gate input to SCR (Q2) goes more negative which results in Q2 cutting off during the next excursion to zero of the unfiltered -12 vdc supply voltage. When Q2 cuts off, the negative bias voltage across capacitor C2 is removed causing 0 volt to be applied to indicator driver 3A2 and to the base of transistor Q3. For this condition, the LOW RF indication on the power amplifier meter panel changes from green to red. Transistor Q3 also cuts off removing the negative voltage across resistor R9 causing diode CR3 to be forward biased. With CR3 forward biased, the negative voltage bias at the base of transistor Q4 is removed causing Q4 to cut off. With Q4 cut off, the bias voltage at the base of Q5 becomes more negative causing Q5 to cut off. When Q5 cuts off, relay K1 becomes deenergized. With relay K1 deenergized, external alarm output pins M and N are shorted through the relay contacts, causing the external summary alarm circuit to be enabled (alarm condition).

b. Diodes CR2 and CR3 form an AND gate. Diode CR3 is controlled by the low RF input as previously described. The beam AND gate enabling input signal controls operation of diode CR2. Normally, the beam AND gate input level to pin T is -7.5v causing diode CR2 to be reversed biased. With CR2 reversed biased, a negative voltage is applied to the base of transistor Q4. For this condition, transistors Q4 and Q5 conduct and relay K1 is energized (normal condition). When the beam gate input level is 0 volt, CR2 is forward biased removing the negative voltage from the base of Q4. For this condition, transistors Q4 and Q5 are cut off and relay K1 is deenergized (alarm condition).

c. Diodes CR4 and CR7 form an OR gate. Diode CR4 is controlled by the low RF and beam AND gate input signals as previously described. Diode CR7 is controlled by the BEAM SWITCH. Normally, the BEAM SWITCH is in the on position causing a beam switch input level of 0 volt at pin S. With 0 volt applied to pin S, diode CR8 is forward biased disabling the beam switch input to the OR gate. For this condition, the OR gate is controlled by the beam gate and low RF inputs. When the BEAM SWITCH is in the off position (power amplifier not in use), -7.5v (alarm disable) is applied to pin S causing diode CR8 to be reversed biased. With CR8 reversed biased, a negative voltage is applied to the base of transistor Q4 causing transistors Q4 and Q5 to conduct and relay K1 to energize which disables the power amplifier's summary alarm output.

d. A sample of the reflected RF power is directed from output directional coupler 3A9DC2 and is rectified by a detecting diode. The rectified signal designated "antenna mismatch" is applied to pin F of the low RF-mismatch, alarm and control module.

(1) Normally (reflected power less than 100 watts), the antenna mismatch input is not of sufficient negative amplitude to bias mismatch trigger Q6 into conduction. With Q6 cut off, the gate input to SCR (Q7) is at a high negative level causing Q7 to be cut off. With Q7 cut off, mismatch driver Q8 is biased into conduction. With Q8 conducting, -7.5v is applied across resistor R20 in the collector circuit. The negative voltage is applied to indicator driver 3A3 via isolating diode CR11 and pin J causing the ANTENNA MISMATCH indication on the power amplifier meter panel to light green. The negative voltage is also applied to beam gate-dc overload control module 3A6 through isolating diode CR12 and pin H to enable the beam gate.

(2) For an alarm condition (reflected power 100 watts or more), the RF-mismatch input is sufficient (-1.0 to -1.5 vdc) to cause mismatch trigger Q6 to conduct. Resistor R15 and capacitor C3 form an integrator circuit at the base of Q6.

ANT MIS control (resistor R16) controls the operating point of the circuit and is set so that transistor Q6 conducts when the reflected power is .100 watts or greater. With Q6 conducting, the gate input to Q7 becomes less negative due to the voltage drops across R17 and R18 causing Q7 to conduct. When Q7 conducts, a negative voltage is applied across resistor R19 and biases mismatch driver Q8 off. With Q8 cut off, the negative voltage across resistor R20 is removed causing the outputs at pins J and H to be at 0 volts. For this condition, the ANTENNA MISMATCH indication on the power amplifier meter panel changes from green to red and the beam gate in module 3A6 is disabled.

1-120. Time-Delay Control Module 3A5 Circuit Theory
(fig. 8-72)

The time-delay control module provides two separate time-delay circuits. One circuit is a beam time-delay circuit which provides a delay of approximately 3.5 minutes before beam voltage is applied to the klystron. The other circuit is a blower shutdown delay circuit which delays shutdown of the six blower motors in the power amplifier cabinet for approximately 3.5 minutes after the MAIN POWER SWITCH has been set to the OFF position.

a. Beam Time-Delay Circuit. The input to the beam time-delay circuit is derived from filament sensing transformer 3A9T4. The transformer senses the current in the klystron filament circuit and provides a voltage drop (approximately 2.5 vac) across resistor 3A9R9 (fig. 8-69). Both transformer 3A9T4 and resistor 3A9R9 are cabinet mounted components and are external to the time-delay control module.

(1) The ac voltage drop across resistor 3A9R9 is applied to full-wave bridge rectifier CR6-CR9 through pins 8 and 4 of the time-delay control module. Front panel test points TP2 and TP3 are provided for monitoring the ac input across pins 8 and 4. The rectified negative output filtered by resistor R7, capacitor C4, and diode CR10 is applied to the base of transistor Q4. With transistor Q4 biases into conducting, gate input to SCR (Q5) is enabled causing Q5 to conduct. Front panel test point TP4 is provided for monitoring the status (on or off) of Q5. With Q5 conducting, the -12v (unfiltered) supply voltage appears across resistor R9 and is filtered by resistor R10 and capacitor C5. The negative voltage across capacitor C5 is applied through pin F to indicator control module 3A2 causing the FILAMENT indication on the power amplifier meter panel to change from red to green.

(2) Also, the negative voltage across capacitor C5 is used to charge time-delay capacitors C6 and C7 and start the beam time-delay. Capacitors C6 and C7 are connected in parallel with each other, and the combination is connected in series with resistor R12 and BEAM TD potentiometer R11. The charging rate (time-delay) is adjusted by the BEAM TD potentiometer. The potentiometer is set so that a period of approximately 3 minutes elapses before the voltage level is sufficient to turn on beam time-delay gate Q6 and Q7. When unijunction transistor Q6 conducts, the gate input to SCR (Q7) is enabled causing Q7 to conduct. When Q7 conducts, a negative voltage (approximately -7.5v) is applied across resistor R15. The voltage is applied through isolating diode CR11 and pi 10 to beam gate dc overload control module 3A6 where it enables the beam and gate. The negative voltage across resistor R15 is also applied through isolating diode CR12 and pin 3 to indicator control module 3A3 which causes the TIME DELAY indication on the power amplifier meter panel to change from amber to green. Test points TP5 and TP6 on the front panel of the time-delay control module are provided for monitoring the beam gate (pin 10) and time-delay indicator (pin 3) outputs.

(3) When the ac input to pins 8 and 4 is removed (no filament current), transistor Q4 cuts off. With Q4 cut off, the gate input to SCR (Q5) is removed and Q5 cuts off during the next excursion through zero of the unfiltered -12v supply voltage. With Q5 cut off, the time-delay capacitors (C6 and C7) discharge causing beam time-delay gate Q6 and Q7 to cut off. For this condition, the FILAMENT indication changes from green to red, the TIME DELAY indication changes from green to amber, and the beam AND gate is disabled.

b. Blower Shutdown Time-Delay Circuit. The blower shutdown time-delay circuit controls removal of the 115 vac input line which operates power supply control 3A7 and the six blower motors in the power amplifier. The 115 vac input line is applied to controlled rectifier Q3 through pins T and 16. Q3 functions as a gate to control the application of the 115 vac input to output pins V and 18. Operation of the gate is controlled by relay K1.

(1) When the MAIN POWER SWITCH is turned on, -12v (unfiltered) is applied through

pin B, diodes CR3 and CR5, and resistor R5 causing relay K1 to energize. With K1 energized, the gate input to Q3 conducts. With Q3 conducting, the 115 vac input is passed to output pins V and 18 causing the blower motors and control power supply to operate. Once power supply control 3A7 is turned on, -7.5v is applied to pins A and K. Also, -7.5v from power supply control 3A7 is applied to pin 11 via the MAIN POWER SWITCH which is in the on position. The -7.5v inputs to pins A and 11 are applied across capacitors C1 and C2 which are connected in parallel with each other. Diode CR1, connected in series with the pin 11 input, provides isolation. The parallel combination of C1 and C2 is connected in series with resistor R2 and BLOW TD potentiometer R1. With -7.5v applied to both the negative and positive plates of capacitors C1 and C2, the capacitors cannot discharge through R1 and R2 and the blower shutdown circuit is disabled.

(2) When the MAIN POWER SWITCH on the power amplifier is turned off, -7.5v is removed from pin 11 and -12v (unfiltered) is removed from pin B. However, relay K1 remains energized by the -7.5v applied through pin K, diodes CR3 and CR4, and resistor R5. With -7.5v removed from pin 11, capacitor C1 and C2 start to charge through resistor R2 BLOW TD potentiometer R1. The charging rate is adjusted by BLOW TD potentiometer R1. The BLOW TD potentiometer is set so that a period of approximately 3 minutes is required to raise the voltage level on the positive plates of capacitors C1 and C2 to the turn on potential of unijunction transistor Q1. Front panel test point TP1 is provided for monitoring the input to Q1. When Q1 conducts, current flows through the primary of transformer T1, transistor Q1, and resistor R3 to ground. The voltage surge induced in the primary of T1 is coupled to the secondary of T1 enabling the gate input to SCR Q2. With Q2 conducting, the -7.5v input through pin K, diode CR4, and resistor R5 is applied to ground causing disabling relay K1. When KI deenergized, Q3 cuts off and the 115 vac output at pins 18 and V is removed causing the blower motors and power supply control 3A7 to shut down.

1-121. Beam Gate-Dc Overload Control 3A6 Circuit Theory
(fig. 1-44)

The beam gate-de overload control module controls the application of 230 vac primary power to the high voltage power supply and also provides the beam gate signal which controls operation of inverter regulator control module 3A1. The beam gate dc overload control module is functionally comprised of an AND gate, a beam gate driver, a relay driver circuit, and a dc overload trigger circuit.

a. Beam AND Gate. The beam AND gate is comprised of diodes CR1, CR5 through CR8, and CR10 through CR12. The eight inputs to the AND gate are applied across resistors R1, R6 through R9, and R14 through R16 respectively. All eight inputs must be at -7.5v to enable the AND gate. With all eight inputs at -7.5v, the AND gate diodes are reverse biased and a negative potential is applied to the base of transistors Q1 and Q3 through resistor R17 and diodes CR2 through CR4. The negative potential is greater than the positive potential causing transistors QI and Q3 to conduct (normal condition). If any one of the eight inputs is removed (drops to 0 volt), the associated AND gate diode is forward biased causing a positive potential at the base of transistors Q1 and Q3. For this condition, transistors Q1 and Q3 are cut off (alarm condition). Test points TP1 through TP8 are provided on the module front panel for monitoring the eight inputs to the AND gate. Diode CR9, resistor R10, and capacitor C1 function as a surge current protection circuit.

b. Beam Gate Driver. The beam gate driver circuit is comprised of transistor stages Q1 and Q2. For normal operating conditions, a negative potential is applied to the base of transistor Q1 through diodes CR2 through CR4. The negative potential is greater than the positive potential applied through resistor R2 causing Q1 to conduct. With Q2 conducting, the potential on the base of transistor Q2 becomes less negative due to the voltage drops across R4, Q1, and R3. This causes transistor Q2 to conduct resulting in a voltage drop of approximately -7.5 volts across collector resistor R5. The negative voltage is applied -via output pin L to inverter regulator control 3A1, low RF-mismatch, alarm and control 3A4 and to the BEAM indicator on the front panel of the power amplifier cabinet. With the negative voltage applied to pin L, the inverter regulator control module is enabled, the power amplifier summary alarm circuit in module 3A4 is disabled, and the BEAM indicator is lighted green (normal indication). For an alarm condition, the negative potential at the base of transistor Q1 is removed causing transistors Q1 and Q2 to cut off. With transistor Q2 cut off, the negative voltage applied to output pin L is removed. This causes

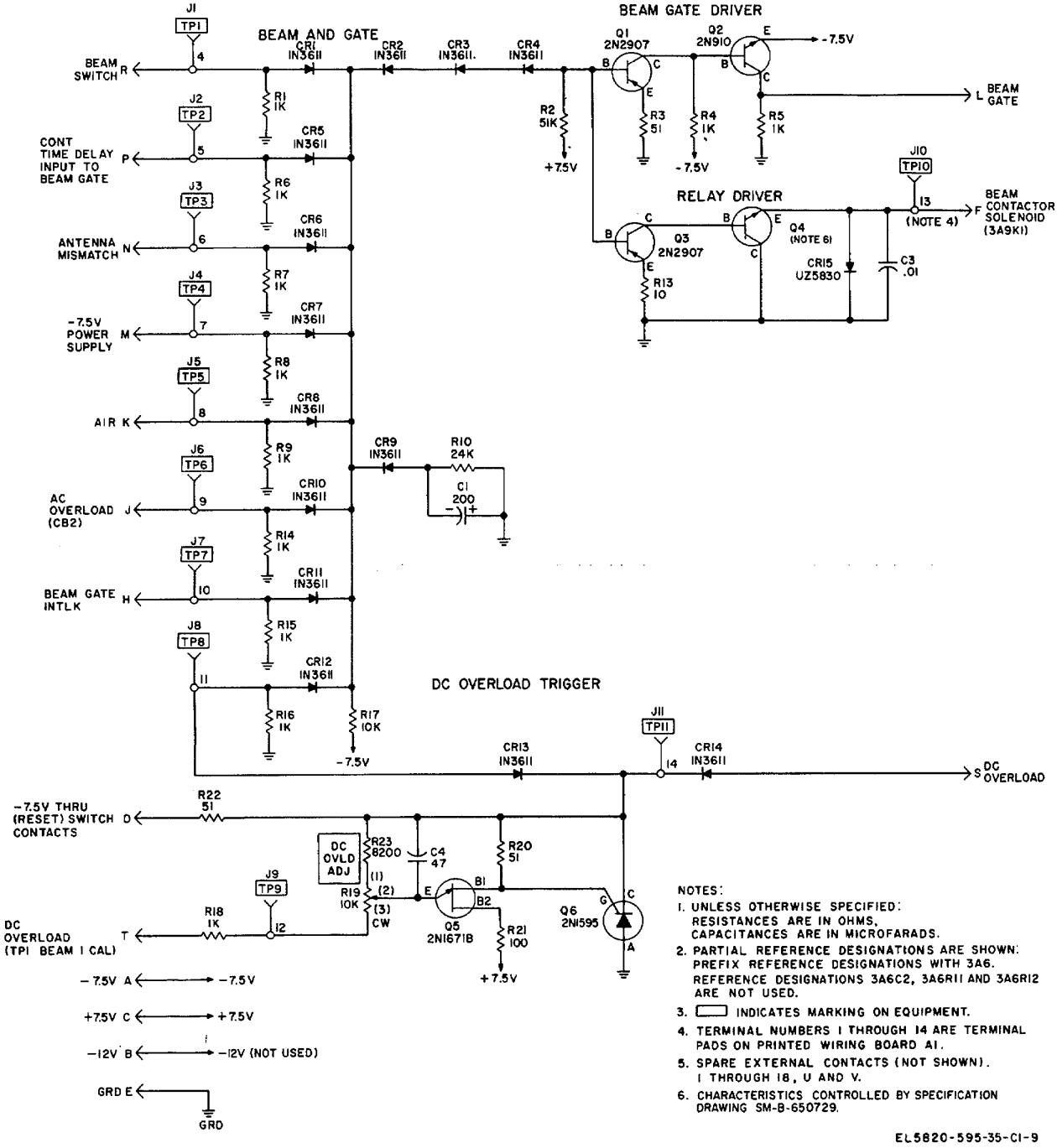


Figure 1-44. Beam gate-dc overload control SA6, schematic diagram.

the inverter control module to be disabled, the power amplifier summary alarm circuit in module 3A4 to be enabled, and the BEAM indication to change from green to red.

c. Relay Driver. The relay driver circuit is comprised of transistor stages Q3 and Q4. For normal operating conditions, a negative potential is applied to the base of transistor Q3 through diodes CR2, CR3, and C'R4. The negative potential is greater than the positive potential applied through resistor R2 causing Q3 to conduct. With Q3 conducting, the base of transistor Q4 becomes more positive causing Q4 to conduct. For this condition, the return path for external main power relay (beam contactor solenoid) 3A9K1 is completed through output pin F and transistor Q4 causing the relay to energize (normal condition). For an alarm condition, the negative potential at the base of transistor Q3 is removed causing transistors Q3 and Q4 to cut off. With Q4 cut off, the return path for the external main power relay is removed and the relay becomes deenergized (alarm condition). Front panel test point TP10 is provided for monitoring the status of the relay driver circuit. Diode CR15 and capacitor C3 are connected across output transistor Q4 to protect the circuit from voltage transients when the external relay deenergizes.

d. Dc Overload Trigger. The dc overload circuit is comprised of unijunction transistor Q5 and controlled rectifier Q6 stages. A detected sample of the high voltage output is applied to the base of unijunction transistor Q5 through pin T, input resistor R18, and one side of DC OVLD ADJ potentiometer R19. Front panel test point TP9 is provided for m9nitoring the sampled input voltage. The other side of potentiometer is connected to -7. 5v through resistors R22 and R23, pin D, and the external RESET switch. Normally, the sampled input voltage at pin T is not sufficient (less than 3.5 vdc) to turn on unijunction transistor Q5. A sampled input of 3.5 vdc or less indicates that the beam current is 550 milliamperes or less. With Q5 cut off, the gate input to controlled rectifier Q6 is disabled causing Q6 to be cut off. With Q6 cut off, the -7.5v input from the RESET switch is applied through pin D and resistor R22 to the cathode junction of diodes CR13 and CR14. Front panel test point TP11 is provided for monitoring the status of the dc overload trigger circuit. The negative voltage is applied through diode CR13 and reverse biases diode CR12 thus enabling the beam AND gate.

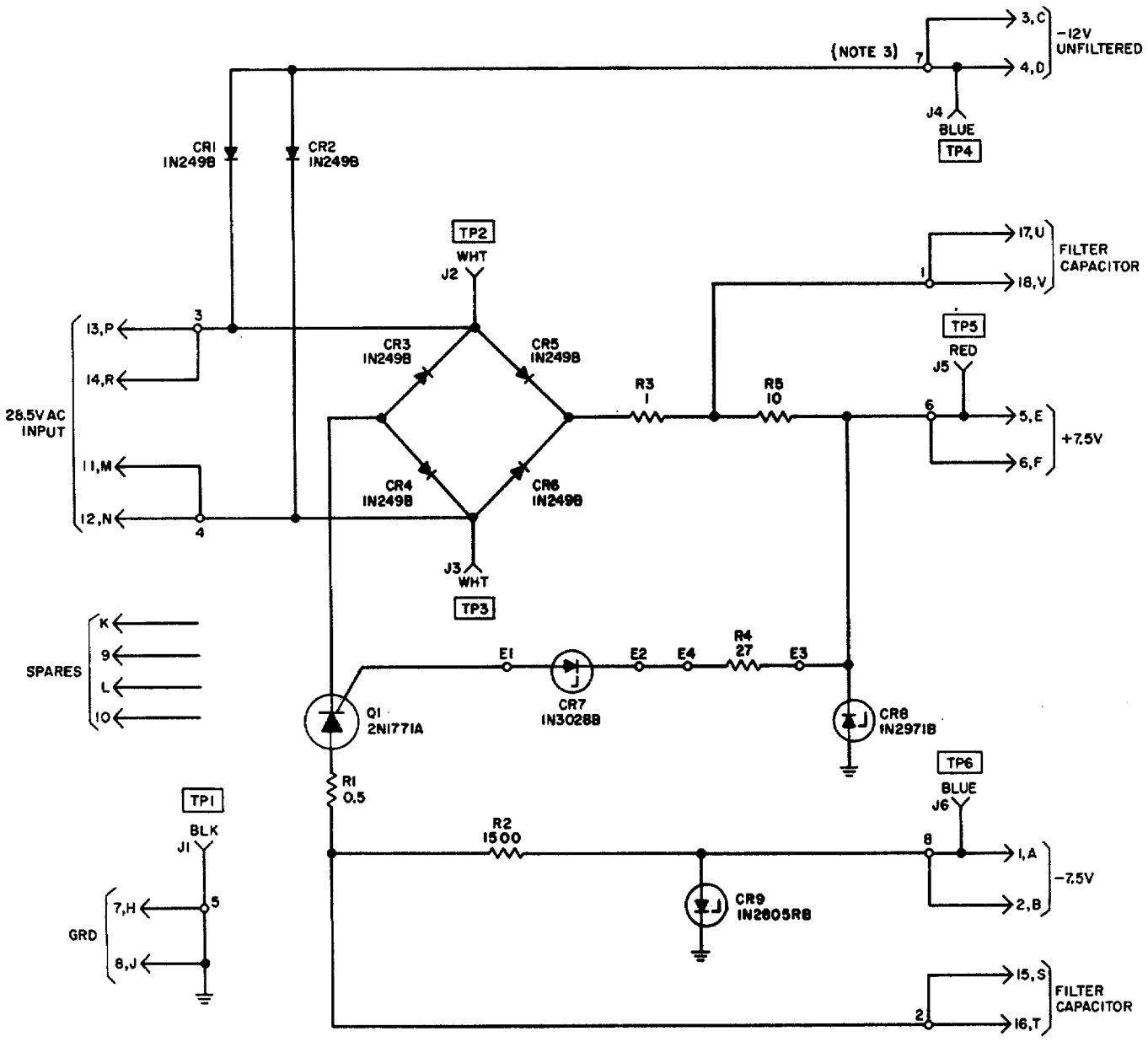
The negative voltage is also applied through diode CR14 and appears at output pin S. The negative output voltage is applied to indicator control module 3A3 which causes the DC OVERLOAD indicator in the front panel to light green. When the high voltage output current rises above 550 milliamperes, the sample voltage rises about 3.5 vdc and turns on Q5. With Q5 turned on, the gate input to controlled rectifier Q6 becomes less negative due to voltage drop across R20, Q5, and R21. This causes Q6 to conduct resulting in a ground potential at the junction of CR13 and CR14. For this condition, diode CR13 is reversed biased and diode CR12 of the beam gate is forward biased causing the beam AND gate to be disabled. Also, diode CR14 is reversed biased and the output at pin S goes to zero potential causing the DC OVERLOAD indication to change from green to red. Once the overload condition has been corrected, the circuit is returned to a normal state by momentarily depressing the external front panel RESET pushbutton. When the pushbutton is depressed, the -7.5v input to pin D is removed which causes Q6 to cease conducting.

1-122. Power Supply Control 3A7 Circuit Theory

(fig. 1-45)

The power supply control module provides +7.5v, -7.5v, and -12v output voltages. The +7.5v and -7.5v outputs are filtered by external capacitors (cabinet mounted). The -12v output is unfiltered. When CONTROL POWER circuit breaker 3A9A1CB4 is closed, the module input is 28.5 vrms from stepdown transformer 3A9T1 (fig. 8-69).

a. +7.5v Supply. The +7.5 volt output is obtained by a circuit consisting of a full-wave bridge, voltage regulator network, and external filter capacitor. The 28.5 vrms input is applied across terminals 3 (pins 13, P, and 14, R) and 4 (pins 11, M, and 12, N) to two full-wave bridge rectifiers (CR3-CR6). Test points TP2 and TP3 are provided on the front panel for monitoring the input across terminals 3 and 4. Rectifiers CR5 and CR6 conduct on alternate half cycles of the 28 vrms input (when the anodes are positive) resulting in a positive dc voltage across cabinet mounted capacitor 3A9C6 (fig. 8-69). The filter capacitor is connected through terminal 1 (pins 17, U and 18, V) to the junction of voltage divider resistors R3 and R5. Zener diode CR8 provides a regulated +7.5 vdc output at terminal 6 (pins 5, E and 6, F). Test point TP5 is provided on the



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX REFERENCE DESIGNATIONS WITH 3A7.
3. TERMINALS E1 THROUGH E4 ARE MOUNTED ON PRINTED WIRING BOARD A1. TERMINALS 1 THROUGH 8 ARE TERMINAL PADS ON PRINTED WIRING BOARD A1.
4. ▭ INDICATES MARKING ON EQUIPMENT.

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Figure 1-45. Power supply control 3A7, schematic diagram.

front panel for monitoring the +7.5 vdc output at terminal 6.

b. -7.5v Supply. The -7.5 volt output is obtained in a similar manner as the +7.5 volt output using the other half of the full-wave bridge rectifier, another cabinet mounted filter capacitor, and a voltage regulator network. Rectifier CR3 and CR4 of the full-wave rectifier conduct on alternate half cycles of the 28 vrms input voltage (when the cathodes are negative), thereby developing a negative de voltage across cabinet mounted filter capacitor 3A9C5 (fig. 8-69). The filter capacitor is connected through terminal 2 (pins 15, S and 16, T) to the junction of voltage divider resistors R1 and R2. Zener diode CR9 provides a regulated -7.5 vdc output at terminal 8 (pins 1, A and 2, B). Zener diode CR7 controls the gate input which turns on controlled rectifier Q1. Q1 must be conducting in order to develop the -7.5 vdc output at terminal 8. The positive gating voltage is developed across Zener diode CR8. If the +7 vdc output should fail, diode CR7 acts as a protective device and removes the gate voltage from controlled rectifier Q1. As a result, the -7.5 vdc output at terminal 8 is removed. Resistors R1 and R4 are current-limiting resistors. Test point TP6 is provided on the front panel for monitoring the -7.5 vdc output.

c. -12v Supply. The -12-volt output is unfiltered and unregulated and is derived from full wave rectifier diodes CR1 and CR2 which are connected across the 28 vrms input at terminals 3 and 4. Each diode conducts on alternate half cycles of the 28 vrms input (when the cathodes are negative), thereby developing an unfiltered and unregulated -12 vdc at output terminal 7 (pins 3, 7 and 4, D). Test point TP4 is provided on the front panel for monitoring the -12 vdc output at terminal 7.

1-123. High Voltage Power Supply Circuit Theory
(fig. 8-73)

The high voltage power supply provides the beam voltage (8,500 volts maximum) for the klystron. The high voltage power supply is functionally comprised of an ac input circuit, 200 vdc supply circuit, filter and overload protection circuit, dc to-ac converter, and a high voltage rectifier and filter circuit. Each circuit is described in a through e below.

a. Ac Input Circuit. The ac input circuit consists of cabinet mounted relay 3A9K1 and TM 11-5820-595-35 circuit breakers CB1 through CB5 in HV power supply 3A9A1. The 230 vac (single phase) is applied to the 200 vdc supply circuit (full-wave bridge rectifier) in inverter 3A8 through pins 3A9A1J2-1 and 3, MAIN POWER circuit breaker 3A9A1CB1-A and B, pins 3A91J2-4 and 5, closed contacts (L1, T1, and L2, T2) of cabinet mounted relay 3A9K1, BEAM POWER circuit breaker 3A9A1CB2, and pins 3A9A1J3-B and A. In addition, -7.5v is applied through pin 3A9A1JI-H, auxiliary contacts (3 and 5) of the BEAM POWER circuit breaker, and pin 3A9AlJ1-J to the beam gate. The -7.5v input is required to enable the beam gate (para 1-121). When the beam gate is enabled, relay 3A9K1 becomes energized allowing 230 vac power to pass (via closed contacts L1, T1, and L2, T2) to the 200 vdc supply circuit . in inverter 3A8 and disabling (open contacts NC1 and NC2) the shelter mounted preheater. Also, with beam gate enabled, 25 Hz to 3. 3kHz trigger pulses are applied to the dc-to ac converter in inverter 3A8. The function of each remaining circuit breaker (3A9A1CB3 through 3A9A1CB5) is given below.

(1) 115 vac is applied through KLYSTRON BLOWER circuit breaker 3A9A1CB3, and pins 3A9AIJ1-A and G to the klystron blower motor.

(2) 115 vac is applied through CONTROL POWER circuit breaker 3A9A1CB4, pins 3A9AlJlA and F, and cabinet mounted transformer 3A9T1 to the dc power supplies (control power supply module 3A7 and the +28-volt power supply)

(3) 115 vac is applied through CABINET FANS circuit breaker 3A9A1CB5, and pins 3A9A1J1-B and F to cabinet mounted blower motors 3A9B2 through 3A9B5. Also, 115 vac operating voltage is applied through CABINET FANS circuit breaker 3A9A1CB5 and pin 3A9A1J3-M to inverter blower motor 3A8B1. In addition, -7.5v is applied through auxiliary contacts 3 and 5 and pins 3A9A1J1-D and C to the beam gate.

b. 200 vdc Supply Circuit. The 200 vdc supply circuit consists of full-wave bridge rectifier (CR5 through CR8) in inverter 3A8. The 230 vac input is rectified and the resulting 200 vdc output is applied through pins 3A8P2-C and D to the filter and overload protection circuit in HV power supply 3A9A1.

c. Filter and Overload Protection Circuit, The filter and overload protection circuit in HV power supply 3A9A1 consists of an LC filter network, overload sensor (transistor circuit Q1), dc over

load trigger (controlled rectifier Q2), and dc overload gate (controlled rectifier Q3).

(1) The positive 200-volt input is applied to pin 3A9AlJ3-C. The LC filter network (L1, L2, C1, C2, C3) provides filtering of the 120-cycle rectified ac. Resistor R5 is a bleeder resistor. The filtered 200 vdc output is applied to the dc-to-ac converter via pins 3A9AIJ3-E and H.

(2) The purpose of the overload protection circuit is to short circuit the positive and negative 200 vdc lines when an overload condition occurs. The short circuit causes BEAM POWER circuit breaker 3A9A1CB2 to trip. With 3A9A1CB2 tripped, the 230 vac input is removed before inverter 3A8 or power transformer 3A9A1T2 can be damaged. When the current exceeds 100 amperes, the overload protection circuit triggers controlled rectifier Q3 into conduction. With Q3 conducting, a short circuit is placed across the 200 vdc output lines. For normal conditions, overload sensor Q1 is turned on. Zener diode CR2 (5.1v) and resistor R8 establish the turn on voltage for Q1. Zener diode CR5 (22 volts) and resistor R7 provide the operating voltage for the overload circuit. With Q1 turned on (conducting), the gate input to overload trigger Q2 is removed causing Q2 to be turned off. With Q2 turned off, the gate input to overload gate (crowbar) Q3 is not present causing Q3 to be turned off. When the current flow through R4 exceeds 100 amperes, the voltage at the base of Q1 becomes negative causing Q1 to turn off. With Q1 turned off, the gate input to Q2 is enabled and Q2 conducts. Zener diode CR3 (9.lv) and resistor R9 establish the turn on voltage for Q2. With Q2 conducting, the gate input to Q3 is enabled causing Q3 to conduct. Consequently, a short circuit is connected across the 200 vdc output lines. The excessive current in the circuit due to the short causes the BEAMI POWER circuit breaker to trip. With the BEAM POWER circuit breaker tripped, 230 vac input power is removed from the full-wave bridge rectifier in inverter 3A8. The -7.5v signal to enable the beam gate is also removed.

d. Dc-to-Ac Converter. The dc-to-ac converter consists of four silicon controlled rectifiers (3A8Q1 through 3A8Q4), arranged in a full-wave bridge configuration, and stepup transformer 3A9A1T2. The positive 200 vdc input is applied to the anodes of Q1 and Q3 via pin 3A8P2-E. The negative 200 vdc input is applied to the cathodes of Q2 and Q4 via pin 3A8P2-H. The silicon controlled rectifiers will not conduct until trigger pulses are applied to their gates. The trigger pulses(25 Hz to 3. 3 kHz) generated in inverter regulator control 3A1 are applied via four pairs of input pins (3A8P1-B and C, M and N, E and F, J and K). Trigger pulses applied simultaneously via pins B, C, and E, F fire silicon controlled rectifiers Q1 and Q4 and trigger pulses are applied simultaneously via pins M, N, and J, K fire silicon controlled rectifiers Q2 and Q3. After the trigger pulses are removed the rectifiers will continue to conduct until capacitor 3A9A1C6 is charged. Assume that trigger pulses are removed from Q1 and Q4 gate inputs. Q1 and Q4 will continue to conduct until capacitor 3A9AlC6 is charged. A damped wave, formed by inductors 3A8L1, 3A8L4, capacitor 3A9A1C6, and the load presented by the primary of transformer 3A9A1T2, causes Q1 and Q4 to turn off. Capacitor 3A9A1C6 discharges through diodes 3A9A8CR1 and CR4. Time constants formed by R1, C1, and R4, C4 dissipate transients. The same sequence as described for Q1 and Q4 is followed for the other pair of controlled rectifiers (Q2 and Q3). The rms value of the inverter output voltage is determined by the repetition rate of the trigger pulses applied to the controlled rectifiers. As the pulse rate increases from 25 Hz to 3.3 kHz, rms value of output voltage increases by about 2 to 1. Stepup transformer 3A9A1T2 provides an output of 9,000 vac across its secondary when 200 vrms is applied to its primary. CR 9 through CR12 provide surge current protection. The 9, 000 vac output of 3A9A1T2 is applied across full-wave bridge rectifier 3A9A33CR4 (cabinet mounted).

e. High Voltage Rectifier and Filter Circuit. The high voltage rectifier and filter circuit consists of full-wave bridge rectifier 3A9A33CR4 (4-diode, bridge rectifier package), filter (3A9A33L1 and 3A9A33C7), and integrating RF filter 3A9A33A1. The 9,,000 vac input is; applied across bridge rectifier 3A9A33CR4 which provides a rectified output of 7,500 volts. Filtering is accomplished by inductor 3A9A33L1 and capacitor 3A9A33C7. Resistor R20 and capacitors C14, C15,and C 16on printed wiring board 3A9A33A1 form RC integrating filter.

Section VI. FUNCTION OF ANTENNA ALIGNMENT INDICATOR

1-124. General

Antenna alignment indicator 4A7 is-used to measure the relative signal strength of receiver channels A and B. The channel A and channel B age levels are applied to the antenna alignment indicator and are measured to provide relative signal strength indications and thus facilitate antenna adjustment.

1-125. Antenna Alignment Indicator 4A7 Circuit Theory

(fig. 1-46)

The receiver agc signals are applied to the meters (Ml and M2) via connector P1, cable W1, and switch S1 (ON position). Capacitors C1 and C2 average out the fluctuations of the incoming age signals to provide peak readings on the meters. In the OFF (TRANSIT) position, switch S1 provides a short across each meter. Terminals E1 and E2 are provided for connecting a telephone handset to permit communication over the link and also with shelter personnel. Terminals E1 and E2 are connected to the remote phone circuitry via P1-F and P1-g.

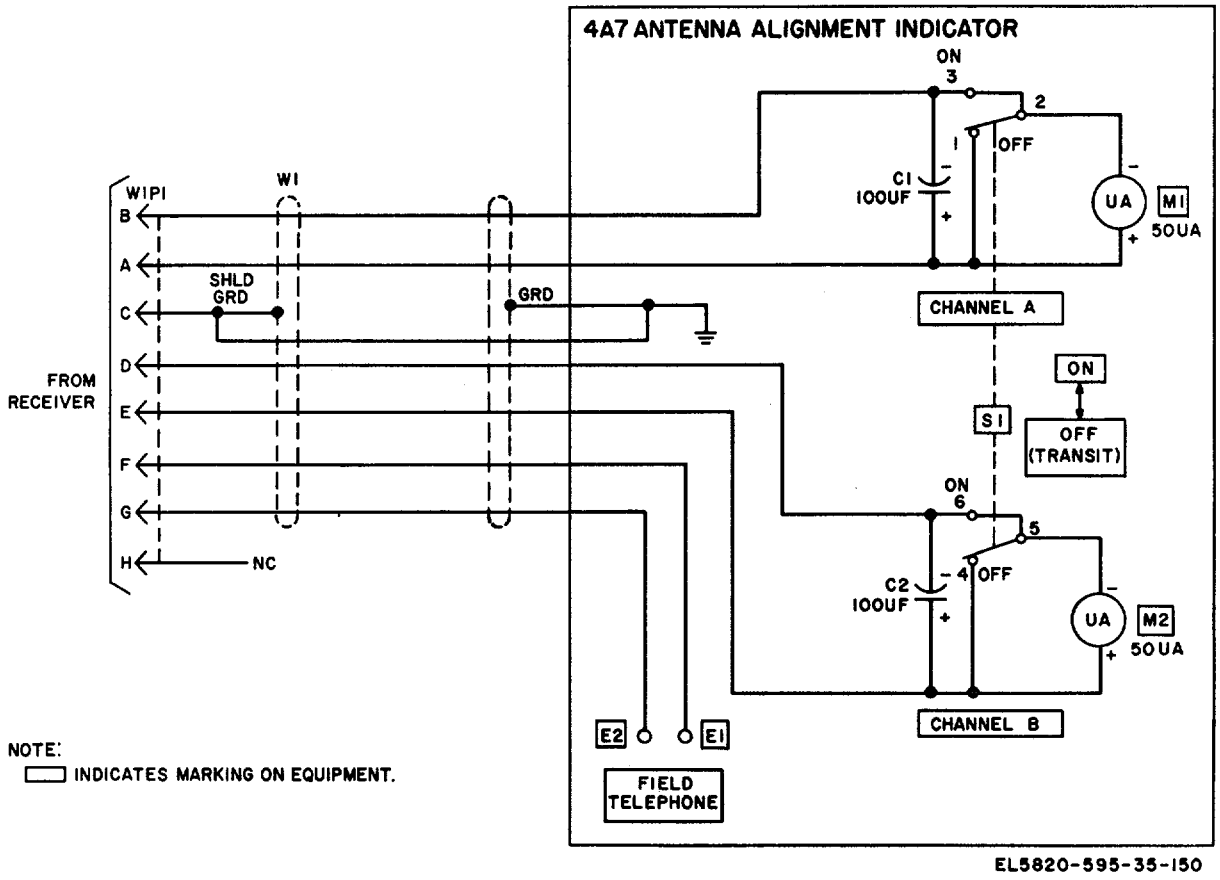


Figure 1-46. Antenna alignment indicator 4A7, schematic diagram.

CHAPTER 2

RADIO SET AN/GRC-143

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

WARNING: ELECTRO MAGNETIC RADIATION

High frequency electromagnetic radiation is present in the power amplifier. Do not work on the power amplifier waveguides or the external waveguides connected to the power amplifier cabinet while the power amplifier is turned on. High frequency electromagnetic radiation can cause fatal internal burns. It can literally "cook" internal organs and flesh. If you feel the slightest warming effect while near the power amplifier MOVE AWAY QUICKLY!

WARNING

Voltages are present in the radio set that can cause death or serious injury upon contact. 115 vac is present in the transmitter, receiver and power amplifier. In addition, 230 vac and voltages in excess of 7000 volts are present in the power amplifier. Do not disable or bypass any equipment interlocks provided for personnel safety and equipment unless specifically stated, then observe all the required Caution and Warning instructions contained in the procedure. Do not place hands or tools near any high voltage terminal in the power amplifier cabinet.

2-1. Scope of Maintenance

The direct support maintenance procedure in this manual supplement the maintenance procedures covered in TM 11-5820-595-12. Procedures for maintaining Radio Set AN/GRC-143 at the direct support level are contained in this chapter and chapter 3 through 6. This chapter lists the tools, test equipment and materials required, covers organization of troubleshooting procedures, and lists the periodic calibration checks and test required as periodic preventive maintenance. It also includes interunit troubleshooting instructions. Direct support maintenance for the individual units of Radio Set AN/GRC-143 and minor components are covered in chapters 3, 4, 5 and 6.

2-2. Tools, Test Equipment, and Materials

The following chart lists the tools, test equipment, and materials required to troubleshoot, test, repair, calibrate, and adjust the radio set at the direct support maintenance level:

Item	Federal stock No.	References
Toolkit, Radio Repair TK-100/G	5180-605-0079	
Toolkit, Electronic Equipment TK-105/G	5180-610-8177	
Attachment, Bar Extension Solid	5120-248-7326	
Hand Ratchet, Socket Wrench, T Sliding	5120-221-7966	
Socket, Wrench, DHEX 12 Point 1/4-inch	5120-235-5869	
Extraction Tool, MS24256 R20	5120-079-4601	
Insertion Tool, MS24256 A20	5120-079-4598	
Extraction Tool, MS24256 R12	5120-079-9461	
Insertion Tool, MS24256 A12	5120-079-4600	
Extraction Tool, MS18278 Size 20	5120-230-3770	
Extractor, CET-C6B	5120-963-7661	
Crimping Tool, MS3191-4 W/Head Assembly W1	5120-856-3732	

Item	Federal stock No.	References
Crimping Tool, MS 3191-4 W/Head Assembly W25	5120-230-3771	TM 11-6625-366-15
Multimeter, TS-352B/U	6625-242-5023	
Counter Electronic Digital Readout AN/USM-207	6625-921-6368	TM 11-6625-700-10
Test Set, Radio Frequency Power AN/USM-161	6625-892-5541	TM 11-6625-498-12
Oscilloscope, AN/USM-281	6625-053-3112	TM 9-6625-2362-12
Signal Generator, AN/URM-52B	6625-965-1501	TM 11-6625-214-10
Test Set, Electrical Meter TS-656/U	6625-348-0666	TM 11-6625-226-12
Facilities Kit, Meter Calibration MK-1207/GRC	6625-133-7863	

2-3. Organization of Troubleshooting Procedures

a. General. The first step in servicing a defective radio set is to sectionalize the fault. Sectionalization means tracing the fault to a major unit within the radio set. The second step is to localize the fault. Localization means tracing the fault to a defective circuit or assembly within the faulty unit. Some faults, such as a defective module or subassembly cannot be repaired at the direct support level, and must be replaced after localization. The majority of faults, however, must be isolated. Isolation means tracing the fault to a defective wire or circuit element within the defective circuit or assembly.

b. Sectionalization. Listed below is a group of checks that are arranged to reduce unnecessary work, and to aid the repairman in tracing a fault to the major unit responsible for abnormal operation.

(1) *Visual inspection*. The purpose of visual inspection is to utilize the meter and alarm indicators provided on each unit of the radio set to sectionalize the fault. Most troubles in the radio set create visual alarms or improper meter indications on the faulty unit.

(2) *Operational checks and tests*. When visual inspection fails to sectionalize the fault, the operational checks provided in the monthly preventive maintenance checks and services chart of TM 11-5820-595-12 should be performed. These checks will frequently indicate the general location of the trouble; and in some instances, will determine the exact nature of the trouble. Operational tests are provided for the transmitter (paras 3-8 and 3-9) and receiver (paras 4-8 through 4-10). These tests check the operating capabilities of the transmitter and receiver and will aid the maintenance man in sectionalizing troubles in the radio set.

(3) *Interunit cable checks*. When a fault cannot be sectionalized to a major unit using the techniques listed above, the trouble is probably due to disconnected or defective interunit cabling. The interunit cable checks provided in paragraph 2-6 will aid in locating troubles in interunit cabling.

c. Localization. After the trouble has been sectionalized (b above), it must be localized to a defective circuit or assembly within the faulty unit. The localization procedures consist of troubleshooting charts (paras 3-3, 4-3, and 5-3) that will aid the repairman in localizing troubles within the radio set. In many instances, the localization procedures will trace the trouble to a replaceable part within the faulty unit. If not, the localization procedures will reference the isolation procedures to be used to find and correct the trouble.

d. Isolation. When a trouble has been localized to a repairable circuit or assembly through use of the troubleshooting charts (*c* above), then the trouble isolation checks (paras 3-5 through 3-7, and 4-5 through 4-7) referenced in the troubleshooting chart, must be used to trace and isolate the trouble to a defective wire or circuit element.

2-4. Periodic Calibration Checks and Tests

Periodic calibration checks and tests must be performed as periodic preventive maintenance by the direct support maintenance man to check the operating condition of the radio set and to maintain the calibration accuracy of its metering circuits. The calibration checks and tests to be performed are listed in a through c below in the order of their recurring maintenance interval. The maintenance interval specified is based on -a: 40-hour equipment operating week. If the equipment is operated for longer periods, the maintenance interval must be adjusted to compensate for

the extended equipment operating time. *For example*, if the equipment is operated 80 hours a week, the maintenance interval must be halved to compensate for the extended equipment operating period. If trouble is encountered during performance of the calibration checks and tests, refer to the troubleshooting cards (paras 3-3, 4-3, and 5-3) for corrective action. Maintenance forms and records to be used and maintained on this equipment are specified in TM 38-750.

a. Quarterly Calibration Checks and Tests.

(1) Transmitter frequency accuracy test (para 3-8).

(2) Transmitter output power and metering test (para 3-9).

(3) Calibration of transmitter radio test set (para 3-41).

(4) Receiver frequency accuracy test (para 4-8).

(5) Receiver local oscillator chain output power and metering test (para P10).

(6) Calibration of power amplifier input power metering circuit (para 5-21).

(7) Calibration of power amplifier forward power metering circuit (para 5-22).

(8) Power amplifier antenna mismatch trip point adjustment and reflected power metering circuit calibration (para 5-25).

b. Semiannual Calibration Checks and Tests.

(1) Calibration of transmitter traffic metering circuit (para 3-37).

(2) Receiver lock and capture test (para 4-9).

(3) Power amplifier dc overload trip point adjustment and beam current metering circuit calibration (para 5-24).

c. Yearly Calibration Checks and Tests.

(1) Calibration of transmitter meter 1A16M1 (para 3-35).

(2) Calibration of transmitter radio test meter 1A15M2 (para 3-36).

(3) Calibration of receiver meter 2A22M1 (para 4-32).

(4) Calibration of receiver traffic metering circuit (para 4-33).

(5) Calibration of power amplifier filament voltage meter 3A9M2 (para 5-17).

(6) Calibration of power amplifier: beam voltage meter 3A9M3 (para 5-18).

(7) Calibration of power amplifier beam current meter 3A9M4 (para 5-19).

(8) Calibration of power amplifier RF monitor meter 3A9M5 (para 5-20).

(9) Power amplifier filament voltage adjustment and metering circuit calibration (para 5-26).

(10) Power amplifier filament current sensing check (para 5-27).

(11) Calibration of antenna alignment indicator meters 4A7M1 and 4A7M2 (para 6-2).

Section II. INTERUNIT TROUBLESHOOTING

2-5. General

When trouble is encountered during radio set operation, and the trouble cannot be sectionalized to a single unit using the sectionalization checks in TM 11-5820-595-12, radio set interunit cables should be checked as the possible source of equipment malfunction.

2-6. Interunit Cable Checks

When interunit cables are suspect as being defective, continuity checks should be made on the cables. An interface cable wiring chart is provided in TM 11-5820-595-12 that lists all the radio set interunit cables. The radio set interconnecting cables diagram in TM 11-5820-595-12 provides routing information for performing the interunit cable checks.

CHAPTER 3

TRANSMITTER DIRECT SUPPORT MAINTENANCE

Section I. TRANSMITTER TROUBLESHOOTING

WARNING

115 vac is present in the transmitter. Do not remove or replace parts, or perform continuity or resistance checks while primary power is applied to the equipment.

3-1. Scope of Transmitter Maintenance

This chapter contains direct support maintenance procedures for troubleshooting, testing, repairing, calibrating and adjusting the transmitter. Paragraph 3-2 specifies transmitter preventive maintenance. Detailed procedures are provided for troubleshooting (paras 3-3 through 3-9), repairs (paras 3-10 through 3-33), and calibration and adjustments (paras 3-34 through 3-42). Procedures for deenergizing and energizing the radio set are provided in paragraphs 3-12 and 3-13.

3-2. Transmitter Periodic Calibration Checks and Tests

Periodic calibration checks and tests must be performed as periodic preventive maintenance on the transmitter to verify the calibration accuracy of metering circuits and check operating condition. Paragraph 2-4 lists the calibration checks and tests that must be performed on each unit of the radio set, and specifies the maintenance interval in which they should be performed.

3-3. Transmitter Troubleshooting Chart

WARNING

Removal and replacement of parts, or continuity and resistance checks must not be performed while primary power is applied to the radio set.

a. General. The transmitter troubleshooting chart is supplied as an aid in localizing troubles in the transmitter. The chart lists the symptoms that may be observed when sectionalizing a trouble to the transmitter. The chart also lists the probable trouble and includes or references procedures to be used to locate and correct the trouble.

b. *Use of the Chart.* The transmitter troubleshooting chart (d below) supplements the operational checks and corrective measures contained in TM 11-5820-595-12. Apply the operational checks and corrective measures in TM 11-5820-595-12 before using the troubleshooting chart in this manual. If the corrective measures for operational checks in TM 11-5820-595-12 fail to correct the trouble or indicate that higher category of maintenance is required, apply the corrective measures listed in the chart below. To use the chart, read down the symptom column of the troubleshooting chart until the abnormal indication or condition is found. Then perform the corrective measures indicated in the chart for that item.

c. Conditions for Troubleshooting. In general, transmitter troubleshooting starts with the radio set turned on and handling pcm traffic. This is required to properly identify and prevent misleading trouble symptoms which could delay fault location. If traffic is not being received from the distant transmitting station, use the radio set loop back test given in TM 11-5820-595-12 to simulate received traffic. During performance of the troubleshooting procedure, it is often necessary to check a part by substitution or to perform continuity and resistance checks. Instructions for performing continuity and resistance checks are provided in paragraph 3-4, and instructions for removal and replacement of parts are provided in paragraph 3-10. Figures 3-3 through 3-19 are parts location diagrams which will aid the repairman in locating parts in the transmitter.

d. Transmitter Troubleshooting Chart.

Item	*Symptom*	*Probable trouble*	*Corrective measure*
1	5 AMPS SLO-BLO fuse on transmitter meter panel blows when replaced.	*a.* Blower 1A16B1 defective.....	*a.* Remove blower 1A16B1 (para 3-18) and check its resistance as follows: T1 to T4 should be 500±100 ohms. T1 to T5 should be 800±100 ohms.
		b. Capacitor 1A16C1 defective.....	*b.* Check capacitor 1A16C1 by substitution (para 3-19).
		c. Defective wiring in primary power distribution circuits.	c. Perform the transmitter primary power distribution checks (para 3-5).
		d. Power transformer 1A16T1 defective.	*d.* Check power transformer 1A16T1 by substitution (para 3-30).
2	Any indicator on power supply 1A1 not lighted.	*a.* Power supply chassis 1A1A13 defective.	*a.* Check power supply chassis 1A1A13 by substitution (para 3-16). If indicator lights after 1A1A13 is replaced, use the power supply chassis 1A1A13 checks (para 3-7) to isolate trouble.
		b. Defective component or wire in dc power distribution circuits.	*b.* Use the transmitter dc power distribution checks (para 3-6) to isolate trouble.
		c. Defective component or wire in primary power distribution circuits.	*c.* Use the transmitter primary power distribution checks (para 3-5) to isolate trouble.
3	5V and 28V indicators on frequency synthesizer 1A14 not lighted.	*a.* Defective wiring -	*a.* Remove frequency synthesizer 1A14 (para 3-28) and check for continuity between pins 5 and 6 of connector 1A16XA14 (fig. 8-14).
		b. Frequency synthesizer main chassis 1A14A10 defective.	*b.* Replace frequency synthesizer main chassis 1A14A10 (para 3-28).
4	28V indicator on frequency synthesizer 1A14 not lighted.	Frequency synthesizer main chassis 1A14A10 defective.	Replace frequency synthesizer main chassis 1A14A10 (para 3-28).
5	5V indicator on frequency synthesizer 1A14 not lighted.	Same as item 4 above	Same as item 4 above.
6	SYNTH OVEN indicator on transmitter meter panel not lighted.	*a.* Defective wiring	*a.* Check for continuity between: pin 2 of 1A16XDS9 (fig. 8-14) and pin 1 of 1A16XA14; pin 1 of 1A16XDS9 and pin G of 1A16XDS1; and pin 3 of 1A16XDS9 and the E2 CAB GRD lug on top of the transmitter cabinet.
		b. Indicator light 1A16XDS9 defective.	*b.* Deenergize the radio set (para 3-12) and check indicator light 1A16XDS9 by substitution.
		c. Frequency synthesizer main chassis 1A14A10 defective.	c. Check frequency synthesizer main chassis 1A14A10 by substitution (para 3-28).
7	Blower 1A16B1 not in operation.....	*a.* Blower 1A16B1 defective.....	*a.* Remove blower 1A16B1 (para 3-18) and check its resistance as follows:. T1 to T4 should be 500±100 ohms. T1 to T5 should be 800±100 ohms.

Item	Symptom	Probable trouble	Corrective measure
		b. Capacitor 1A16C1 defective	*b.* Check capacitor 1A16C1 by substitution (para 3-19).
8	Any module fault indicator lamp on frequency synthesizer 1A14 lighted.	Frequency synthesizer main chassis 1A14A10 defective.	Replace frequency synthesizer main chassis 1A14A10 (para 3-28).
9	Any step of the transmitter power supply voltage checks (TM 11-5820-595-12) fails.	Same as item 2 above	Refer to item 2.
10	Any step of the transmitter module test point checks (TM 11-5820-595-12) fails.	Defective component or wire in the dc power distribution circuits.	Perform the transmitter dc power distribution checks (para 3-6).
11	All status and alarm indicators on the transmitter meter panel not lighted.	*a.* 5 AMPS SLO-BLO fuse 1A16F1 defective.	*a.* Check 5 AMPS SLO-BLO neon fuse indicator on transmitter meter panel. If lighted, refer to item 1 above.
		b. Same as item 2 above	*b.* Check indicators on power supply 1A1. If any indicator not lighted, refer to item 2 above.
12	CNTRL ALARM indicator on transmitter meter panel lighted red.	*a.* Functional alarm detected, causing CNTRL ALARM indicator to light red.	*a.* Check alarm indicators on transmitter, receiver, and power amplifier. If any alarm indicator other then CNTRL ALARM is lighted red, troubleshoot on basis of that alarm indication .
		b. Defective wiring	*b.* Remove order wire assembly 1A13 (para 3-27) and check resistance between pins 22, 23, 24, and 25 of connector 1A16XA13B and the E2 CAB GRD lug on top of the transmitter cabinet (fig. 8-14). If any pin is grounded, use the transmitter interconnecting diagram (fig. 8-14) to trace and isolate the defective wire.
		c. Order wire chassis 1A13A7 defective.	*c.* Check order wire chassis 1A13A7 by substitution (para 3-27).
13	TRAF indicator on transmitter meter panel lighted red.	*a.* Defective wiring	*a.* Turn meter selector switch 1A16S4 to TRAFFIC. If 1A16M1 indication is in the orange band, remove alarm monitor 1A5 and check resistance between pin 2 and 11 of connector 1A15W1XA5A (fig. 8-14). Resistance should be greater than 10 ohms.
		b. Coaxial cable 1A16W1 defective	*b.* Check shelter mounted TRAF IN alarm indicator. If lighted red, check coaxial cable 1A16W1 by substitution.
		c. Digital data modem chassis 1A12A15 defective.	*c.* Check digital data modem chassis 1A12A15 by substitution (para 3-26).
		d. Coaxial cable 1A16W8 defective	*d.* Check coaxial cable 1A16W3 by substitution.
		e. Defective wiring	*e.* Remove alarm monitor 1A5 and check resistance between pin A3 and 5 of connector 1A15W1XA5B (fig. 8-14). Resistance should be greater than 100,000 ohms. Re-

Item	Symptom	Probable trouble	Corrective measure
			move modulator 1A8 and check resistance between pin A3 of connector 1A15WIXA5B and pin 7 of connector 1A15W1XA8 (fig. 8-14). Resistance should be between 100 and 400 ohms.
14	RF POWER indicator on transmitter meter panel lighted red.	*a.* Error in frequency synthesizer 1A14 frequency.	*a.* Check SYNTH LOCK indicator on transmitter meter panel. If lighted red, refer to item 15 below.
		b. Defective wiring.	*b.* Check INTERLOCK indicator on transmitter meter panel. If lighted red, refer to item 19 below.
		c. Defective module in RF output circuits.	*c.* Turn meter selector switch 1A16S4 to RF POWER. If 1A16M1 indication is not in the yellow band, refer to item 32 below.
		d. Defective wiring	*d.* Remove alarm monitor 1AS and check resistance between pin 2 and 25 of connector 1A15W1XA5A (fig. 8-14). Resistance should be greater than 10 ohms.
15	SYNTH LOCK indicator on transmitter meter panel lighted red.	*a.* Frequency synthesizer main chassis 1A14A10 defective.	*a.* Check frequency synthesizer main chassis 1A14A10 by substitution (para 3-28).
		b. Defective wiring	*b.* Remove frequency synthesizer 1A14 (para 3-28) and alarm monitor 1A5 and check for continuity between pin 7 of connector 1A16XA14 and pin 17 of connector 1A15W1XA5B (fig. 8-14). Also check resistance between pins 2 and 9 of connector 1A15W1XA5A (fig. 8-14). Resistance should be greater than 10 ohms.
16	REFL RF POWER indicator on transmitter meter panel lighted red.	*a.* Directional coupler 1DC2 and/or coaxial cable 1A16W15 defective.	*a.* Disconnect interunit coaxial cable connected to RF OUTPUT connector J8 on top of the transmitter cabinet. Connect two 10 db attenuators (CN-845/USM-161) to the J8 RF OUTPUT connector. If the REFL RF POWER indicator is still lighted red, check directional coupler 1DC2 and coaxial cable 1A16W15 by substitution (para 3-31).
		b. Interunit coaxial cable between transmitter RF OUTPUT connector J8 and power amplifier RF INPUT connector J3 defective.	*b.* Check interunit coaxial cable by substitution.
		c. Power amplifier coaxial cable 3A9W1 defective.	*c.* Check coaxial cable 3A9W1 (fig. 5-12) by substitution.
		d. Power amplifier variable attenuator 3A9AT1 defective.	*d.* Check variable attenuator 3A9AT1 (fig. 5-12) by substitution.
		e. Power amplifier coaxial cable 3A9W2 defective.	*e.* Check coaxial cable 3A9W2 (fig. 5-13) by substitution.

Item	Symptom	Probable trouble	Corrective measure
		f. Power amplifier directional coupler 3A9DC1 defective.	*f.* Check directional coupler 3A9DC1 (fig. 5-13) by substitution.
		g. Power amplifier coaxial cable 3A9W4 defective.	*g.* Check coaxial cable 3A9W4 (fig. 5-12) by substitution.
17	RADIO TO CABLE MODEM indicator on transmitter panel lighted red.	Digital data modem chassis 1A12A15 defective.	Check digital data modem chassis 1A12A15 by substitution (para 3-26).
18	CABLE TO RADIO MODEM indicator on transmitter meter panel lighted red.	*a.* Digital data modem chassis 1A12A15 defective.	*a.* Check digital data modem chassis 1A12A15 by substitution (para 3-26).
		b. Coaxial cable 1A16W1 defective	*b.* Check coaxial cable 1A16W1 (fig. 3-4) by substitution.
19	INTERLOCK indicator on transmitter meter panel lighted red.	*a.* Equipment interconnect cable harness defective.	*a.* Disconnect the equipment interconnect cable harness from EQUIPMENT INTERCONNECT J4 on top of the transmitter. If INTERLOCK indicator lights green, perform the inter-unit cable checks (para 2-6).
		b. Defective wiring	*b.* Set POWER ON-OFF switch on transmitter meter panel to OFF. Check resistance between pins U and Y or connector 1A16W19J4 (fig. 8-14). Resistance should be greater than 100 ohms.
		c. Relay 1A16K1 defective	*c.* Replace relay 1A16K1 (para 3-21).
20	Any digital data modem 1A12 failure indicator lamp not lighted.	Digital data modem chassis 1A12A15 defective.	Replace digital data modem chassis 1A12A15 (para 3-26).
21	No indication on meter 1A16M1 when meter selector switch 1A16S4 is set to each of its positions.	*a.* Meter selector switch 1A16S4 defective.	*a.* Set meter selector switch 1A16S4 to TEST LEAD (+) and check for continuity between pins C and 5 of 1A16S4B (fig. 8-14). Also check for continuity between pin C of 1A16S4A and the E2 CAB GRD lug on top of the transmitter.
		b. Meter 1A16M1 defective	*b.* Check meter lA16Ml using-the calibration procedure given in paragraph 3-35.
22	OW TEST meter indication not in black band when order wire test given in TM 11-5820-595-12 is being performed.	*a.* Same as item 18 above MODEM	*a.* Check CABLE TO RADIO indicator. If lighted red, refer to item 18 above.
		b. Order wire chassis 1A13A7 defective.	*b.* Check order wire chassis 1A13A7 by substitution (para 3-27).
23	MODULATOR CONTROL meter indication not in black band.	*a.* Defective wiring	*a.* Remove modulator 1A8 and check resistance between pins 1 and 2 of connector 1A15W1XA8 (fig. 8-14). Resistance should be greater than 10 ohms. Also check resistance between pins 3 and 4 of connector 1A15WlXA8. Resistance should be greater than 5 ohms.
		b. Defective metering circuit	*b.* Check for continuity between pin 10 of connector 1A15W1XA8 and pin 9 of 1A16S4B (fig. 8-14). If continuity is obtained, check for continuity between pin 9 of 1A16S4A and the E2 CAB GRD

Item	Symptom	Probable trouble	Corrective measure
			lug on top of the transmitter cabinet.
24	MODULATOR OUTPUT meter indication not in black band.	*a.* Defective wiring	*a.* Perform the corrective measures indicated for item 23a above.
		b. Defective metering circuit	*b.* Check for continuity between pin 9 of connector 1A15W1XA8 and pin 11 of 1A16S4B (fig. 8-14). If continuity is obtained, check for continuity between pin 11 of 1A16S4A and the E2 CAB GRD lug on top of the transmitter cabinet.
25	FREQ. CONTROL CTR FREQ. meter indication not in blue band.	*a.* Defective wiring	*a.* Remove electronic frequency control 1A7 and check resistance between pins 3 and 4 of connector 1A15W1XA7 (fig. 8-14). Resistance should be greater than 5 ohms.
		b. Defective metering circuit	*b.* With meter selector switch 1A16S4 set to FREQ CONTROL CTR FREQ, check for continuity between pins 6 and 7 or connector 1A15W1XA7 (fig. 8-14).
26	FREQ CONTROL OUTPUT meter indication riot in black band.	*a.* Defective wiring	*a.* Perform the corrective measures indicated for item 25a above.
		b. Defective metering circuit	*b.* Check for continuity between pin 9 of connector 1A15W1XA7 and pin 15 of 1A16S4B (fig. 8-14). Also check for continuity between pin 15 of 1A16S4A and the E2 CAB GRD lug on top of transmitter cabinet.
27	TRAFFIC meter indication not in orange band.	*a.* Same as item 13 above	*a.* Check TRAF indicator on transmitter meter panel. If lighted red, refer to item 13 above.
		b. Metering circuit requires calibration.	*b.* Calibrate the transmitter traffic metering circuit (para 3-37).
28	SYNTHESIZER meter indication not in yellow band.	*a.* Frequency synthesizer main chassis 1A14A10 defective.	*a.* Check frequency synthesizer main chassis 1A14A10 by substitution (para 3-28).
		b. Defective metering circuit	*b.* Remove frequency synthesizer 1A14 (para 3-28) and check for continuity between pin A1of connector 1A16XA14 and pin 19 of lA16S4B (fig. 8-14). Also check for continuity between pin 19 of 1A16S4A and the E2 CAB GRD lug on top of the transmitter cabinet.
29	AMPL-MULT meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 1A16S4 to RF POWER. If 1A16Ml indication is in yellow band, perform the transmitter output power and metering test (para 3-9).
		b. Same 28 above	*b.* Turn meter selector switch 1A16S4 to SYNTHESIZER. If 1A16M1 indication is not in yellow band, refer to item 28 in this chart.

Item	Symptom	Probable trouble	Corrective measure
		c. Coaxial cable 1A16W6 defective	*c*. Check coaxial cable 1A16W6 (fig. 3-4) by substitution.
		d. Defective wiring	*d*. Remove amplifier-frequency multiplier 1A11 (TM 11-5820-595-12) and check resistance between pins 1 and 2 of connector 1A15W1XA11(fig.8-14). Resistance should be greater than 7 ohms.
		e. 1137- to 1213-MHz bandpass filter 1FL5 or 1137- to 1213-MHz circulator 1HYl defective.	*e*. Check 1137- to 1213-MHz bandpass filter 1FL5 and 1137- to 1213-MHz circulator 1HY1 by substitution (para 3-25).
30	2ND MULT meter indication not in yellow band.	a. Metering circuit requires calibration.	*a.* Turn meter selector switch 1A16S4 to RF POWER. If 1A16M1 indication is in yellow band, perform the transmitter output power and metering test (para 3-9).
		b. Same as item 29 above	*b*. Turn meter selector switch 1A16S4 to AMPL-MULT. If 1A16M1 indication is not in yellow band, refer to item 29 above.
		c. 2275- to 2425-MHz circulator 1A10HY1 defective.	*c*. Check 2275- to 2425-MHz circulator 1A10HY1 by substitution (para 3-24).
		d. 1137- to 1213-MHz circulator 1HY1 defective.	*d.* Check 1137- to 1213-MHz circulator 1HY1 by substitution (para 3-25).
31	3RD MULT (LOCAL OSC) meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 1A16S4 to RF POWER. If 1A16M1 indication is in yellow band, perform the transmitter output power and metering test (para 3-9).
		b. Same as item 30 above	*b*. Turn meter selector switch 1A16S4 to 2ND MULT. If 1A16M1 indication is not in yellow band, refer to item 30 above.
		c. 4.4- to 5.0-GHZ circulator 1A9HY1 defective.	*c*. Check 4.4- to 5.0-GHZ circulator 1A9HY1 by substitution (para 3-23).
		d. Frequency mixer 1A9 defective	*d*. Replace frequency mixer 1A9 (TM 11-5820-595-12).
		e. 2275- to 2425-MHz circulator 1A10HY1 defective.	*e*. Check 2275- to 2425-MHz circulator 1A10HY1 by substitution (para 3-24).
32	RF POWER meter indication not in yellow band.	*a*. Metering circuit requires calibration.	*a*. Check RF POWER indicator on transmitter meter panel. If lighted green, calibrate the RF POWER metering circuit (para 3-38).
		b. Same as item 31 above	*b*. Turn meter selector switch 1A16S4 to 3RD MULT (LOCAL OSC). If lA16Ml indication is not in yellow band, refer to item 31 above.
		c. Error in transmitter frequency	*c*. Perform the transmitter frequency accuracy test (para 3-8).

Item	Symptom	Probable trouble	Corrective measure
		d. Frequency mixer 1A9 defective	*d*. Check frequency mixer 1A9 by substitution (TM 11-5820-595-12).
		e. 4.4- to 5.0-GHz bandpass filter 1FL3 defective.	*e*. Check 4.4- to 5.0-GHz bandpass filter 1FL3 by substitution (para 3-31).
		f. 5.0-GHz low pass filter 1FL4 defective.	*f*. Check 5.0-GHz low pass filter 1FL4 by substitution (para 3-31).
		g. Directional coupler 1DC2 defective.	*g*. Check directional coupler 1DC2 by substitution (para 3-31).
33	REFL RF POWER meter indication greater than 20.	*a*. Same as item 16 above	*a*. Check REFL RF POWER indicator. If lighted red, refer to item 16 above.
		b. Metering circuit requires calibration.	*b*. Calibrate the REFL RF POWER metering circuit (para 3-39).
34	Frequency synthesizer 1A14 frequency error greater than 3 kHz, as determined by test (para 3-8).	*a*. Standard RF oscillator 1A14A7 defective.	*a*. Check standard RF oscillator 1A14A7 by substitution.
		b. RF oscillator 1A14A1 defective	*b*. Check RF oscillator 1A14A1 by substitution.
		c. Frequency synthesizer 1A14 defective.	*c*. Check frequency synthesizer 1A14 by substitution (para 3-28).
35	Cannot adjust transmitter modulator frequency to 150 MHz±-20 kHz (para 3-42).	*a*. Modulator 1A8 defective	*a*. Check modulator 1A8 by substitution.
		b. Electronic frequency control 1A7 defective.	*b*. Check electronic frequency control 1A7 by substitution.
36	Transmitter output power less than 150 milliwatts as determined by test (para 3-9).	*a*. Amplifier-frequency multiplier 1A11 defective.	*a*. Check amplifier-frequency multiplier 1A11 by substitution (TM 11-5820-595-12).
		b. Frequency multiplier group 1A10 defective.	*b*. Check frequency multiplier group 1A10 by substitution (TM 11-5820-595-12).
		c. Frequency mixer 1A9 defective	*c*. Check frequency mixer 1A9 by substitution (TM 11-5820-595-12).
		d. Frequency synthesizer 1A14 defective.	*d*. Check frequency synthesizer 1A14 by substitution (para 3-28).
37	Cannot calibrate the TRAFFIC metering circuit (para 3-37).	Defective component or wire in metering circuit.	Remove alarm monitor 1A5 and check resistance between pin 12 of connector 1A15W1XA5B and the E2 CAB GRD lug on top of the transmitter cabinet (fig. 8-14). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 1A16R7 (fig. 3-5) is varied from one extreme to the other. Make the same resistance check between pin 17 of 1A16S4B and pin 12 of connector 1A15W1XA5B.
38	Cannot calibrate the RF POWER metering circuit (para 3-38).	*a*. Defective wiring	*a*. Remove alarm monitor 1A5 and check for continuity between pin 2 of connector 1A15W1XA5B and the center conductor of coaxial cable 1A15W12P1 (fig. 8-14).
		b. Defective component or wire in metering circuit.	*b*. Check resistance between pin 4 of connector 1A15W1XA5B and the E2 CAB GRD lug on top of

Item	Symptom	Probable trouble	Corrective measure
			transmitter cabinet (fig. 8-14). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 1A16R6 (fig. 3-5) is varied from one extreme to the other. Make the same resistance check between pin 4 of connector lA15W1XA5B and pin 27 of 1A16S4B.
		c. Directional coupler 1DC2 defective	*c*. Check directional coupler 1DC2 'by substitution (para 3-31).
39	Cannot calibrate REFL RF POWER metering circuit (para 3-39).	*a*. Defective wiring	*a*. Remove alarm monitor 1A5 and check for continuity between pin 14 of connector 1A15W1XA5B and the center conductor of coaxial cable 1A15W15W13P1 (fig. 8-14).
		b. Defective component or wire in metering circuit.	*b.* Check resistance between pin 15 of connector 1A15W1XA5B and the E2 CAB GRD lug on top of transmitter cabinet (fig. 8-14) Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 1A16R5 (fig. 3-5) is varied from one extreme to the other. Make the same resistance check between pin 15 of connector 1A15W1XA5B and pin 29 of 1A16S4B.
		c. Directional coupler 1DC2 defective.	*c.* Check directional coupler 1DC2 by substitution (para 3-31).
40	Cannot calibrate 3RD.MULT (LOCAL OSC) metering circuit (para 3-40).	a. Defective wiring	*a*. Check for continuity between the center conductor of coaxial cable 1A15W11P1 and terminal 1 of potentiometer 1A16R2 (fig. 8-14).
		b. Defective component or wire in metering circuit.	*b.* Check resistance between terminal 1 of potentiometer 1A16R2 and pin 25 of 1A16S4A (fig. 8-14). Note that resistance varies smoothly from zero to 50.000 ohms as potentiometer 1A16R2 (fig. 3-5) is varied from one extreme to the other.
		c. 4.4- to 5.0-GHz circulator 1A9HY1 defective.	*c.* Check 4.4- to 5.0-GHz circulator 1A9HY1 by substitution (para 3-23).
41	Cannot calibrate 2ND MULT metering circuit (para 3-40).	a. Defective wiring	*a*. Check for continuity between the center conductor of coaxial cable 1A15W10P1 and terminal 1 of potentiometer 1A16R3 (fig. 8-14).
		d. Defective component or wire in metering circuit.	*b.* Check resistance between terminal 1 of potentiometer 1A16S4A (fig. 8-14). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 1A16R3 (fig. 3-5) is varied from one extreme to the other.
		c. 2275- to 2425-MHz circulator 1A10HY1 defective.	*c.* Check 2275- to 2425-MHz circulator 1A10HY1 by substitution (para 3-24).

Item	Symptom	Probable trouble	Corrective measure
42	Cannot calibrate AMPL-MULT metering circuit (para 3-4).	*a.* Defective wiring	*a.* Check for continuity between the center conductor of coaxial cable 1A15W8P1 and terminal 1 of potentiometer 1A16R4 (fig. 8-14).
		b. Defective component or wire in metering circuit.	*b.* Check resistance between terminal 1 of potentiometer 1A16R4 and pin 21 of 1A16S4A (fig. 8-14). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 1A16R4 (fig. 3-5) is varied from one extreme to the other.
43	Cannot calibrate radio test set (para 3-41).	*a.* 100-MHz RF oscillator 1A2 defective.	*a.* Use the radio test set check given in TM 11-5820-595-12 to check radio test set.
		b. Coaxial cable 1A15W14 defective.-	b. Check continuity of coaxial cable 1A15W14 (fig. 3-4).
		c. Crystal mixer 1Z1 defective	*c.* Check crystal mixer 1Z1 by substitution (para 3-22).
		d. RF power divider 1DC1 defective	*d.* Check RF power divider 1DC1 by substitution (para 3-22).
		e. Variable attenuator 1AT3 and/or coaxial cable 1A16W16 defective.	*e.* If RECEIVER CHAN A input is low, check variable attenuator 1AT3 and coaxial cable 1A16W16 by substitution (para 3-22).
		f. Variable attenuator 1AT4 and/or coaxial cable 1A16W17 defective.	*f.* If RECEIVER CHAN B input is low, check variable attenuator 1AT4 and coaxial cable 1A16W17 by substitution (para 3-22).
44	Cable loop back test (TM 11-5820 595-12) indicates radio set is faulty.	*a.* Coaxial cable 1A16W1 or 1A16W2 defective.	*a.* Check coaxial cables 1A16W1 and 1A16W2 by substitution.
		b. Digital data modem chassis 1A12A15 defective.	*b.* Check digital data modem chassis 1A12A15 by substitution (para 3-26).

3-4. Transmitter Continuity and Resistance Checks

WARNING

115 vac is present in the transmitter. Do not perform any continuity or resistance checks while the radio set is energized.

To perform any continuity or resistance check given in the transmitter troubleshooting chart, proceed as follows:

a. Deenergize the radio set (para 3-12).

b. Connect the TS-352B/U test leads between the two points given in the troubleshooting chart.

c. For continuity checks observe that the meter indication on TS-352B/U is less than 5 ohms. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

d. For resistance checks observe that the indication is within the tolerance specified in the troubleshooting chart. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

e. After the trouble has been corrected, energize the radio set (para 3-13) and check that the corrective action taken has corrected the trouble.

3-5. Isolating Troubles in Transmitter Primary Power Distribution Circuit

WARNING

115 vac is present in the transmitter. Do not perform any trouble isolation check given in this paragraph while the radio set is energized.

To isolate a trouble in the primary power distribution circuit of the transmitter, proceed as follows:

a. Remove power supply 1A1 from the transmitter (para 3-16).

b. Remove switch 1A16S3 protective cover (fig.

3-7) by removing the two nuts and screws securing it to the transmitter meter panel.

c. Remove order wire and frequency synthesizer assembly 1A13/1A14 from the transmitter (para 3-27).

d. On the TS-352B/U, turn the FUNCTION switch to OHMS, and connect the two test leads supplied with TS-352B/U to the OHMS terminals.

e. Refer to primary power distribution checkpoint chart provided in h below. Set the range switch on TS-352B/U to the position indicated for check step 1, and connect the TS-352B/U test leads between transmitter checkpoints 1 and 2 for the same check step.

f. Observe that TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If not, use the transmitter interconnecting diagram (fig. 8-14) to trace and isolate the trouble.

g. Repeat *e* and *f* information above for each successive check step listed in the chart.

h. Primary power distribution checkpoint chart.

Check step	=Range switch position on TS-352B/U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
1	RX1	1A16J7-A	1A16S3-4	Less than 1
2	RX1	-A	1A16S3-3	Less than 1[a]
3	RX10000	-A	1A16E2 (CAB GRD)	Infinityb
4	RX10000	-A	1A16J7-C	Infinityb
5	RX1	-B	A16E2 (CAB GRD)	Zero
6	RX1	-C	1A16S3-2	Less than 1
7	RX1	-C	1A16S3-1	Less than 1[a]
8	RX10000	-C	1A16J7-B	Infinityb
9	RX1	1A16S3-1	1A16XA14-6	Less than 1
10	RX1	-3	1A16XA14-6	Less than 1
11	RX1	-3	1A16S3-1	Less than 2
12	RX10000	-3	1A16E2 (CAB GRD)	Infinity
13	RX1	1A16W18XA1A	1A16W18XA1A-20	Less than 1
14	RX10000	-1	1A16E2 (CAB GRD)	Infinity
15	RX1	-3	1A16W18XA1A-22	Less than 1
16	RX10000	-3	1A16E2 (CAB GRD)	Infinity
17	RX1	-6	1A16W18XA1A-25	Less than 1
18	RX10000	1A16W18XA1A-6	1A16E2 (CAB GRD)	Infinity
19	RX1	-7	1A16W18XA1A-26	Less than 1
20	RX10000	-7	1A16E2 (CAB GRD)	Infinity
21	RX1	-9	1A16W18XA1A-28	Less than 1
22	RX10000	-9	1A16E2 (CAB GRD)	Infinity
23	RX1	1A16W18XA1A-10	1A16W18XA1A-29	Less than 1
24	RX10000	-10	1A16E2 (CAB GRD)	Infinity
25	RX1	-11	1A16W18XA1A-30	Less than 1
26	RX10000	-11	1A16E2 (CAB GRD)	Infinity
27	RX1	-12	1A16W18XA1A-31	Less than 1
28	RX10000	-12	1A16E2 (CAB GRD)	Infinity
29	RX1	-14	1A16W18XA1A-33	Less than 1
30	RX10000	-14	1A16E2 (CAB GRD)	Infinity
31	RX1	-16	1A16W18XA1A-35	Less than 1
32	RX10000	-16	1A16E2 (CAB GRD)	Infinity
33	RX1	-18	1A16W18XA1A-37	Less than 1
34	RX10000	-18	1A16E2 (CAB GRD)	Infinity
35	RX1	-19	1A16E2 (CAB GRD)	Zero

Switch 1A16S3 set to ON position.
Switch 1A16S3 set to OFF position.

3-6. Isolating Troubles in Transmitter DC Power Distribution Circuit

WARNING

115 vac is present in the transmitter. Do not perform any trouble isolation check given in this paragraph while the radio set is energized.

To isolate a trouble in the dc power distribution circuit of the transmitter, proceed as follows: a. Remove power supply 1A1 from the transmitter (para 3-16).

b. Remove modules 1A2, 1A4, 1A5, 1A7, 1A8, and 1A1 from the transmitter (TM 11-5820-595-12).

c. Remove order wire and frequency synthesizer assembly 1A13/1A14 (para 3-27), and digital data modem 1A12 (para 3-26a(1) through (3)) from' the transmitter.

d. On the TS-352B/U, turn the FUNCTION switch to OHMS, and connect the two test leads

h. Dc power distribution checkpoint chart.

e. Refer to dc power distribution checkpoint chart provided in h below. Set the range switch on TS-352B/U to the position indicated for check step 1, and connect the TS-352B/U test leads between transmitter checkpoints 1 and 2 of the same check step.

f. Observe that TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If. not, use the transmitter interconnecting diagram (fig. 8-14) to trace and isolate the trouble.

g. Repeat *e* and *f* information above for each successive check step listed in the chart.

Check step	=Range switch position on TS-352B/U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
1	RX1	1A16XA1B-2	1A16XA12B-3	Zero
2	RX10000	-2	1A16XA1B-21	Infinity
3	RS10000	-2	1A16E2 (CAB GRD)	Infinity
4	RX1	-21	1A16XA12B-4	Zero
5	RX1	-3	1A16XA12B-6	Zero
6	RX100001	-3	1A16E2 (CAB GRD)	Infinity
7	RX100001	-3	1A16XA1B-22	Infinity
8	RX1	-22	1A16XA12B-7	Zero
9	RX1	-7	1A16XA12B-8	Zero
10	RX10000	-7	1A16E2 (CAB GRD)	Infinity
11	RX10000	-7	1A16XA1B-26	Infinity
12	RX1	-26	1A16XA12B-9	Zero
13	RX1	-8	1A16XA13B-36	Zero
14	RX10000	-8-	1A16E2 (CAB GRD)	Infinity
15	RX10000	-8	A16XAB-27	Infinity
16	RX1	-27	1A16XA13B-37	Zero
17	RX1	-10	A16XA13B-38	Zero
18	RX10000	-10	A16E2 (CAB GRD)	Infinity
19	RX10000	-10	A16XA1B-29	Infinity
20	RX1	-29	1A16XA13B-39	Zero
21	RX1	-11	1A16XA13B-34	Zero
22	RX10000	-11	1A16E2 (CAB GRD)	Infinity
23	RX10000	-11	1A16XA1B-30	Infinity
24	RX1	-30	-1A16XA13B-35	Zero
25	RX1	-12	1A16XA12B1	Zero
26	RX10000	-12	A16E2 (CAB GRD)	Infinity
27	RX10000	-12	1A16XA1B-31	Infinity
28	RX1	-31	1A16XA12B-2	Zero
29	RX1	-14	1A15W1XA5A-16	Zero
30	RX1	-14	1A16XA12B-12	Zero
31	RX10000	-14	1A16E2 (CAB GRD)	Infinity
32	RX10000	-14	1A16XA1B-33	Infinity
33	RX1	-33	1A15WXA5A-17	Zero
34	RX1	-33	1A16XA12B-13	Zero
35	RX1	-15	1A15W1XA2-3	Zero
36	RX1	-15	1A15W1XA4-3	Zero
37	RX1	-15	1A15W1XA7-3	Zero
38	RX1	-15	1A15W1XA8-3	Zero
39	RX10000	-15	1A16E2 (CAB GRD)	Infinity
40	RX10000	-15	1A16XA1B-32	Infinity

Check step	Range switch Position on TS-352B /U -	Receiver check points		S-352B /U indication in ohms
		Point 1	Point 2	
41	RX10000	1A16XAB-15	1A16XA1B-34	Infinity
42	RX1	-32	1A16W19J4-V	Zero
43	RX1	-34	1A15W1XA2-4	Zero
44	RX1	-34	1A15W1XA4-4	Zero
45	RX1	-34	1A15W1XA7-4	Zero
46	RX1	-34	1A15W1XA8-4	Zero
47	RX1	-16	1A16W19J4-F	Zero
48	RX1	-16	1A15W1XA5A-1	Zero
49	RX1	-16	1A15W1XA8-1	Zero
50	RX1	-16	1A16XA13B-29	Zero
51	RX1	-16	1A16XDS5-C2	Zero
52	RX1	-16	1A16XDS9-1	Zero
53	RX1	-16	1A16XDS1-G	Zero
54	RX1	-16	1A16XDS10-G	Zero
55	RX1	-16	1A16XDS14-G	Zero
56	RX1	-16	1A16XDS18-G	Zero
57	RX1	-16	1A16XA1B-35	Greater than 10
58	RX1	-35	1A16W19J4-G	Zero
59	RX1	-35	1A15W1XA5A-2	Zero
60	RX1	-35	1A15W1XA8-2	Zero
61	RX1	-35	1A16XA13B-30	Zero
62	RX1	-35	1A16XDS5-B2	Zero
63	RX1	-35	1A16XDS9-3	Zero
64	RX1	-18	1A15W1XA1-1	Zero
65	RX10000	-18	1A16XA1B-37	Infinity
66	RX10000	-18	1A16E2 (CAB GRD)	Infinity
67	RX1	-37	1A15W1XA11-2	Zero

3-7. Isolating Troubles in Power Supply Chassis 1A1A13

To isolate a trouble in power supply chassis 1AIA13, proceed as follows:

a. Remove plug-in modules lAlA1 through 1A1A4, and 1A1A6 through lA1A12 from power supply chassis lA1A13 by performing steps 1 through 8 of paragraph 3-16a.

b. Remove the ten screws and associated washers (fig. 3-8) securing rear shield to power supply chassis 1AIA13.

c. On the TS-352B/U, turn the FUNCTION switch to OHMS, and connect the two leads supplied with TS-352B/U to the OHMS terminals.

d. Refer to power supply chassis 1A1A13 checkpoint chart provided in g below. Set the range switch on TS-352B/U for the position indicated in check step 1, and connect the TS-352B/U test leads between checkpoints 1 and 2 for the same check step.

e. Observe the TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If not, use the power supply 1A1 interconnecting diagram (fig. 8-16) to trace and isolate the trouble.

f. Repeat *d* and *e* information above for each successive check step listed in the chart.

g. Power supply chassis 1AlA13 checkpoint chart.

Check step	Range switch Position on TS-352B /U -	Receiver check points		S-352B /U indication in ohms
		Point 1	Point 2	
1	RX1	A1A13P1-1	1A1A13XA1-14	Less than 1
2	RX10000	-1	1A1A13P1-9	Infinity
3	RX10000	-1	1A1A13P1-20	Infinity
4	RX1	-20	1A1A13XA1-15	Zero
5	RX1	-3	1A1A13XA2-14	Less than 1
6	RX10000	-3	1A1A13P1-19	Infinity

Check step	Range switch Position on TS-352B /U -	Power supply chassis 1A1A13 checkpoints		TS-352B /U indication in ohms
		Point 1	Point 2	
7	RX10000	-3	1A1A13P1-22	Infinity
8	RX1	-22	1A1A13XA2-15	Zero
9	RX1	-6	1A1A13XA3-1	Less than 1
10	RX10000	-6	1A1A13P-19	Infinity
11	RX10000	-6	1A1A13P1-25	Infinity
12	RX1	-25	1A1A13XA3-15	Zero
13	RX1	-7	1A1A13XA4-14	Less than 1
14	RX10000	-7	1A1A13P-19	Infinity
15	RX10000	-7	1A1A13P-26	Infinity
16	RX1	-26	1A1A13XA4-15	Zero
17	RX1	-9	1A1A13XA6-14	Less than 1
18	RX1	-9	1A1A13P1-19	Infinity
19	RX10000	-9	1A1A13P1-28	Infinity
20	RX1	-28	1A1A13XA6-15	Zero
21	RX1	-10	1A1A13XA7-14	Less than 1
22	RX10000	-10	1A1A13P-19	Infinity
23	RX10000	-10	1A1A13P1-29	Infinity
24	RX1	-29	1A1A13XA7-15	Zero
25	RX1	-11	1A1A13XA8-14	Less than 1
26	RX10000	-11	1A1A13P1-19	Infinity
27	RX10000	-11	1A1A13P1-30	Infinity
28	RX1	-30	1A1A13XA8S-15	Zero
29	RX1	-12	1A1A13XA9-14	Less than 1
30	RX10000	-12	1A1A13P1-19	Inanity
31	RX0000	-12	1A1A13P-31`	Infinity
32	RX1	-31	1A1A13XA9-15	Zero
33	RX1	-14	1A1A13XA10-14	Less than 1
34	RX10000	-14	1A1A13P1-19	Infinity
35	RX10000	-14	1A1A13P1-33	Infinity
36	RX1	-33	1A1A13XA10-15	Zero
37	RX1	-16	1A1A13XA11-14	Less than 1
38	RX10000	-16	1A1A13P1-19	Infinity
39	RX10000	-16	1A1A13P1-35	Infinity
40	RX1	-35	1A1A13XA11-15	Zero
41	RX1	-18	1A1A13XA12-14	Less than 1
42	RX10000	-18	1A1A13P1-9	Infinity
43	RX10000	-18	1A1A13P-37	Infinity
44	RX1	-37	1A1A13XA12-15	Zero
45	RX10000	1A1A13P2-2	1A1A13J1	200K±2K
46	RX1	-2	1A1A13XA1-13	Zero
47	RX10	-2	1A1A13XA1-8	Less than 120
48	RX1	-21	1A1A13XA1-8	Zero
49	RX10000	-3	1A1A13J2	200K±2K
50	RX1	-3	1A1A13X2-13	Zero
51	RX10	-3	1A1A13XA2-8	Less than 120
52	RX1	-22	1A1A13XA2-8	Zero
53	RX1	-7	1A1A13XA3-8	Zero
54	RX10000	-7	1A1A13J38	237K+2.4K
55	RX10	-7	1A13XA3-13 8	Less than 140
56	RX1	-26	1A1A13XA3-13	Zero
57	RX1	-8	1A1A13XA4-8	Zero
58	RX10000	-8	1A1A13J4	237Kh2.4K
59	RX10	-8	1A1A13XA4-13	Less than 140
60	RX1	-27	1A1A13XA4-13	Zero
61	RX10000	-10	1A1A13J6	475K h4.8K
62	RX1	-10	1A1A13XA6-13	Zero
63	RX100	-10	1A1A13KA6-8	Less than 250
64	RX1	-29	1A1A13XA6-8	Zero
65	RX10000	-11	1A1A13J7	475K±4.8K
66	RX1	-11	1A1A13XA7-13	Zero
67	RX100	-11	1A1A13XA7-8	Less than 250
68	RX1	-30	1A1A13XA7-8	Zero

Check step	Range switch Position on TS-352B /U -	Power supply chassis 1A1A13 checkpoints TS-352B /U		indication in ohms
		Point 1	Point 2	
69	RX10000	1A1A13P2-12	1A1A13J8	475K44.8K
70	RX1	-12	1A1A13XA8-13	Zero
71	RX100	-12	1A1A13XAS-8	Less than 250
72	RX1	-31	1A1A13XA8-8	Zero
73	RX10000	-13	1A1A13J10	604K-6K
74	RX1	-13	1A1A13XA10-13	Zero
75	RX100	-13	1A1A1A3XA10-8	Less than 330
76	RX1	-32	1A1A13XA10-8	Zero
77	RX1	-14	1A1A13XA9-8	Zero
78	RX10000	-14	1A1A13J9	475K + 4.8K
79	RX100	-14	1A1A13XA9-13	Less than 250
80	RX1	-33	1A1A13XA9-13	Zero
81	RX10000	-15	1A1A13J10	604K6K
82	RX1	-15	1A1A13XA10-13	Zero
83	RX100	-15	1A1A13XA10-8	Less than 330
84	RX1	-34	1A1A13XA10-8	Zero
85	RX10000	-16	1A1A13J11	1.1 Meg-100K
86	RX1	-16	1A1A13XA11-13	Zero
87	RX100	-16	1A1A13XA11-8	Less than 600
88	RX1	-35	1A1A13XA11-8	Zero
89	RX10000	-18	1A1A13J12	1.1 Meg-100K
90	RX1	-18	1A1A13XA12-13	Zero
91	RX100	-18	1A1A13XA12-8	Less than 600
92	RX1	-37	1A1A13XA12-8	Zero

3-8. Transmitter Frequency Accuracy Test

a. General. The transmitter frequency accuracy test is used to check the frequency generating components in the transmitter and determine when corrective action must be taken. The test must be performed at the periodic maintenance interval specified in paragraph 2-4 and when indicated in the transmitter troubleshooting chart (para 3-3d). The performance standards listed in the chart (e below) indicate the minimum requirements for equipment maintained in the field and the corrective action to be taken if the performance standards are not met. This test will interrupt transmit radio communications.

b. Test Equipment Required.

(1) Counter Electronic, Digital Readout AN/USM-207.

(2) Adapter, TNC male to BNC female 11CP4 (part of MK-1207/GRC).

(3) Capacitive Decoupler 1IA2 (part of MK-1207/GRC).

(4) Adapter, UG-274B/U (part of AN/ USM-207).

c. Test Conditions. This procedure assumes that the radio set is turned on and connected for normal operation at the start of the test. Prior to performing the test, the maintenance man should notify the Multiplexer TD-204/U and distant radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

d. Initial Test Equipment Turn On. Turn on the AN/USM-207 and allow a 15-minute warmup period.

e. Procedure.

Step No.	Control setting Test equipment .	Equipment under test	Test procedure	Performance standard
1	AN/USM-207 -N/- SENSITIVITY: PLUG-IN FUNCTION: FREQ Time base switch to GATE TIME (SEC -1) - 10 2. Converter attenuator switches to 10V MAX. DIRECT-HETERODYNE: HETERODYNE. Mixing frequency selector	N/A	a. Record the test transmitter operating frequency setting on frequency synthesizer 1A14 controls. b. Set the controls on frequency synthesizer 1A14 to 4490.0 MHz. c. Disconnect. coaxial cable 1A16W6 from the OUTPUT J8 connector on frequency synthesizer 1A14. d. Connect the test equipment as shown in view A, fig. 3-1.	a. None. b. None. c. None. d. one.

Step No.	Control settings Test equipment	Equipment under test	Test procedure	Performance standard
	switch to 250. DISPLAY control to desired display time.		e. Observe the LEVEL METER on AN/USM-207. If meter indication is in the green zone, proceed to g below. Otherwise, perform f below.	e. None.
			f. Alternately set the upper and lower converter attenuator switches on AN/UISM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.	f. None.
			g. Observe digital display on AN/USM-207. Add 200 MHZ to this display. *Record*.	g. Frequency synthesizer should be 290MHz ± 3 kHz. If it is not, refer to the transmitter troubleshooting chart (item 34, para 3-3d) for corrective action.
			h. Disconnect the test equipment --------	h. None.
			i. Reconnect coaxial cable 1A16W6 to the OUTPUT J8 connector on frequency synthesizer 1A14 and then reset its controls to the original transmitter operating frequency recorded in a above.	i. None.
2	Same as above except set mixing frequency selector switch to 100.	N/A --------	a. Disconnect coaxial cable 1A6W2 from the J1 connector on modulator 1A8.	a. None.
			b. Disconnect coaxial cable 1A8W1 from A1J1 connector on frequency mixer 1A9.	b. None.
			c. Connect the equipment as shown in view B, fig. 3-1.	c. None.
			d. Observe the LEVEL METER on AN/USM-207. If meter indication is in the green zone, proceed to step f below. Otherwise, perform e below.	d. None.
			e. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.	e. None.
			f. Observe digital display on AN/USM-207. Add 100 MHz to this indication. *Record*.	f. Modulator 1A8 frequency accuracy should be 150 MHz 9:20 kHz. If it is not, perform the transmitter modulator 1A8 frequency adjustment (para 3-42).
			g. Disconnect the test equipment -----	g. None.
			h. Connect coaxial cable 1A6W2 to the J1 connector on modulator 1A8.	h. None.
			i. Connect coaxial cable 1A8W1 to the A1J1 connector on frequency mixer 1A9.	i. None.

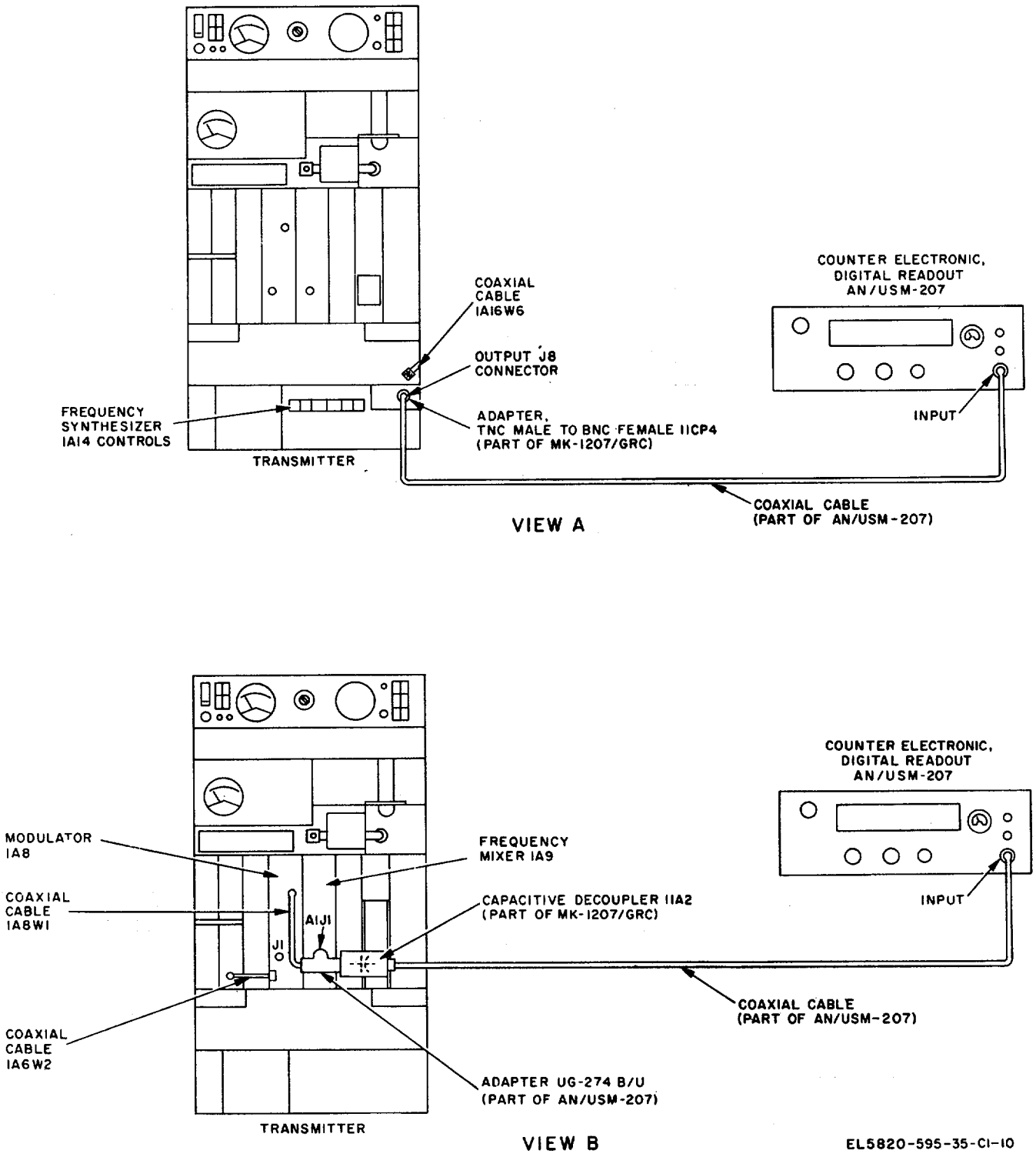


Figure 3-1. Transmitter frequency accuracy test setup.

3-9. Transmitter Output Power and Metering Test

a. General. The transmitter output power and metering test is used to determine the transmitter's RF output level and check the calibration accuracy of its RF power metering circuits. The test must be performed at the periodic maintenance interval specified in paragraph 2-4 and when indicated in the transmitter troubleshooting chart (para 3-3*d*). The performance standards listed in the chart (e below) indicate the minimum requirements for equipment maintained in the field and the corrective action to be taken if the performance standards are not met. This test will interrupt transmit radio communications.

b. Test Equipment Required.

(1) Test Set, Radio Frequency Power AN/USM-161.

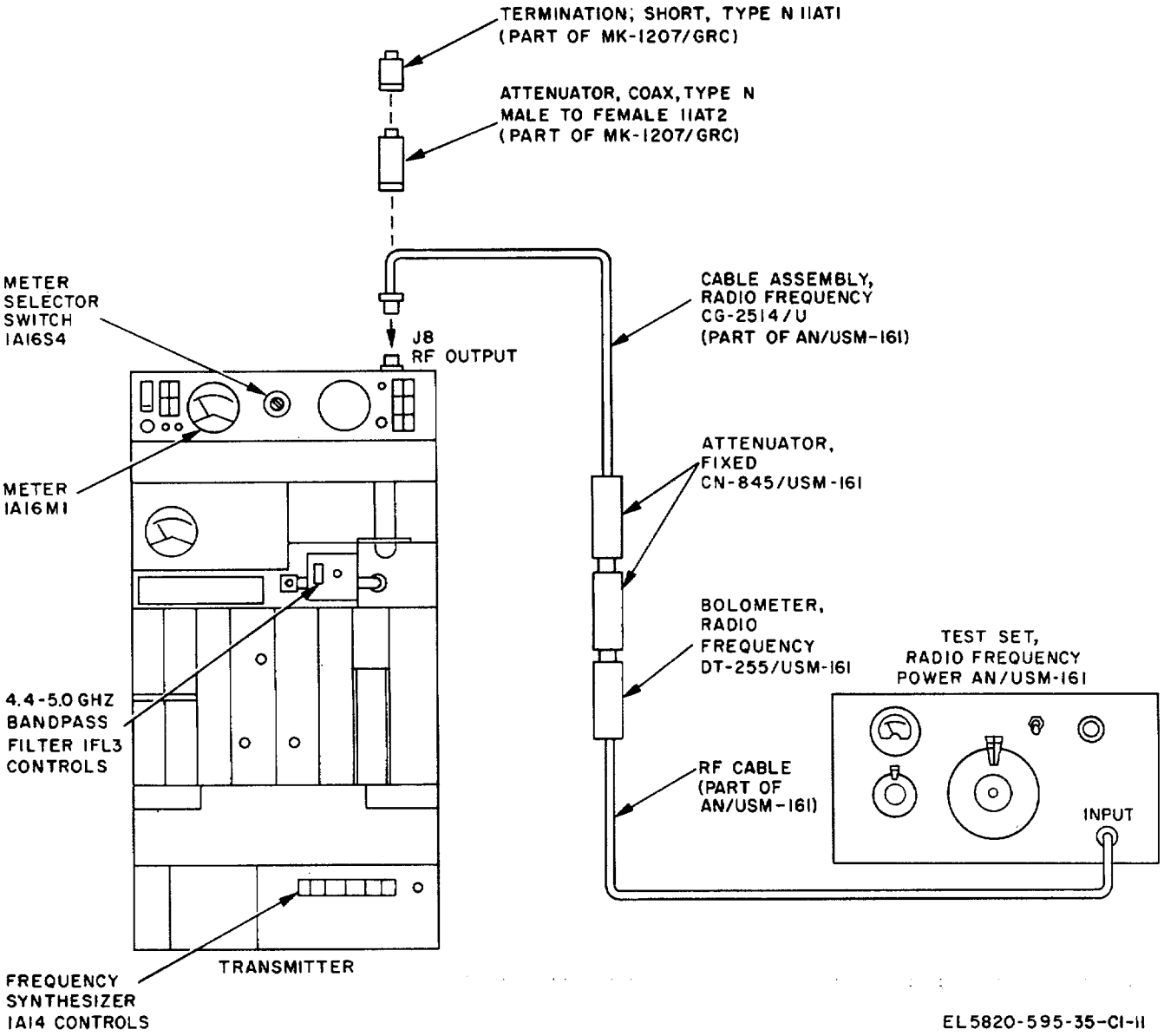


Figure 3-2. Transmitter output power and metering test setup.

(2) Attenuator, Coax, Type N Male to Female ,1AT2, (part of MK-1207/GRC).

(3) Termination, Short, Type N,11AT1, (part of MK-1207/GRC),

c. Test Conditions. This procedure assumes that the radio set is turned on and connected for normal operation at the start of the test. Prior to performing the test, the maintenance man should notify the Multiplexer TD-204/U and distant TM 11-5820-59535 radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

d. Initial Test Equipment Turn-on and Calibration. Turn the AN/USM-161 on and allow a 30-minute warm-up period. After the warmup period is over, calibrate the AN/USM-161 using the procedure given in TM 11-6625-498-12.

e. Procedure.

Step No.	*Control settings* *Test equipment*	*Equipment under test*	*Test procedure*	*Performance standard*
1	AN/USM-161---------- BIAS-READ: READ POWER RANGE: 10 MW +10 DBM. POWER indicator dial to 1.0 on outermost scale.	N/A-------	a. Record the transmitter operating frequency setting on frequency synthesizer 1A14 controls. Then set the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to 4800 MHz.	a. None.
			b. Disconnect the coaxial cable connected to RF OUTPUT J8 connector on top of the transmitter cabinet.	b. None.
			c. Connect the equipment as shown in fig. 3-2.	c. None.
			d. Calculate the calibration plate correction factors for the two CN-845/USM-161's and CG-2514/U for a 4800 MHz input (TM 11-6625-498-12, RF power measurement). Algebraically add the correction factors noting the plus or minus sign. *Record*.	d. None.
			e. Set the COMP ATTENUATOR dial on AN/USM-161 to the value recorded in step d above.	e. None.
			f. Adjust POWER indicator dial on AN/USM-161 until a null is obtained on the AN/USM-161 NULL INDICATOR metes. Multiply the indication on outermost scale of AN/USM-161 POWER indicator dial by 1,000. *Record*.	f. Transmitter output power should be 150 milliwatts minimum. If it is not, refer to the transmitter troubleshooting chart (item 36, para 3-3d) for corrective action.
			g. Turn transmitter meter selector switch to AMPL-MULT.	g. Indication on transmitter meter 1A16M1 should be 100 minimum. If it is not, calibrate the transmitter frequency multiplier metering circuit (para. 3-40).
			h. Turn transmitter meter selector switch to 2ND MULT.	h. Same as g above.
			i. Turn transmitter meter selector switch to 3RD MULT (LOCAL OSC).	i. Same as g above.

Step No.	Control settings Test equipment	Equipment under test	Test procedure	Performance standard
			j. On the AN/USM-161, set the POWER RANGE switch to 3.0 MW +5 DBM, and set POWER indicator dial to .75 on the center scale.	a. None.
			k. Adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter - 1FL3 until a null is obtained on the AN/USM-161 NULL INDI-CATOR meter.	k. None.
			l. Turn transmitter meter selector switch to RF POWER.	l. Indication on transmitter meter 1A16M1 should be 30±10. If it is not, calibrate the transmitter rf power metering circuit (para. 3-38).
			m. Set the POWER indicator dial on AN/USM-161 to 1.5 on center scale.	m. None.
			n. Adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter 1FL3 until a null is obtained on the AN/USM-161 NULL INDI-CATOR meter.	n. None.
			o. Disconnect the test equipment from RF OUTPUT connector J8 on top of the transmitter cabinet.	o. None.
			p. Connect coax attenuator 11AT2 and Type N short l1ATl to RF' OUT-PUT connector J8 on top of the transmitter cabinet (fig. 3-2).	p. None.
			q. Turn transmitter meter selector switch 1A16S4 to transmitter meter panel to REFL RF POWER.	q. Indication on transmitter meter 1A16M1 should be 209:5. If it is not, calibrate the transmitter reflected rf power metering circuit (para. 3-39).
			r. Disconnect the test equipment-----	r. None.
			s. Connect the coaxial cable removed in step b to RF OUTPUT connector J8 on top of the transmitter cabinet.	s. None.
			t. Reset the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to the original operating frequency recorded in step a.	t. None.

Section II. TRANSMITTER REPAIRS

3-10. Scope of Transmitter Repairs

a. The sequence of events listed below should be followed when replacing any part in the transmitter to minimize potential personnel hazards and optimize restoring the radio set to an operational state.

(1) Deenergize radio set.

(2) Part replacement.

(3) Energize radio set.

(4) Performance check.

(5) Confirm radio set operational status.

b. Equipment malfunctions are generally

corrected by replacing the known defective item with its equivalent new part. Part replacement, however, does not assure the operational integrity of the radio s-t and must include performing an operational check. The operational check will confirm correction of the equipment malfunction prior to reestablishing the radio sets operational status.

c. Procedures for deenergizing the radio set are provided in paragraph 3-12. Detailed procedures for specific part removal are provided in paragraph 3-15 through 3-33. When replacing any part, specific precautions and practices should be observed and are itemized in paragraph 3-11.

3-11. Transmitter Parts Replacement Techniques

The following precautions apply when removing, replacing, or repairing parts in the transmitter.

a. Replacement of components with rigid coaxial cables require care when removing or replacing the coaxial cable connectors to prevent damage to connector pin alignment. Instructions for removal and replacement of the rigid coaxial cable with mating connectors are provided in paragraph 3-14.

b. Tag all hardware and components during removal procedures for correct identification during replacement procedures. Before a part is unsoldered, note the position of the leads. If the part has several leads, tag each of the leads before unsoldering any of them.

c. When removing a defective part, be careful not to damage leads or other parts by pulling or pushing them out of the way.

d. Whenever replacing a part, install the new part in the same position as the original. Use an exact duplicate whenever possible.

e. Use a pencil-type soldering iron with a 25watt maximum heating capacity. If the iron must be used with ac, use an isolating transformer between the iron and the ac line. Do not use a soldering gun; damaging voltages can be induced in the equipment parts.

f. If wiring must be replaced, use leads of the same length and gauge if possible. Do not use replacement wire with a higher gauge number (small diameter). With the exception of harness cabling, run the leads in the same manner as the original wiring. For harness cabling, cut the old conductor as short as possible without removing it TM 11-5820595-35 from the harness. Dress the new conductor and spot tie it to the outside of the harness. Make connections to the same terminals used in the original wiring, even where there are alternatives which appear electrically equivalent.

g. Make well-soldered connections, using no more solder than is necessary. A carelessly soldered connection may create a new fault and is one of the most difficult faults to find.

h. Do not allow drops of solder to fall into the unit. Do not allow a soldering iron to come into contact with insulation or parts that might be injured by excessive heat.

i. Do not disturb the setting of any uncalibrated control without predetermining its proper setting prior to reenergizing the radio set.

3-12. Deenergize Radio Set

To deenergize the radio set or any unit in the radio set, the following procedures must be performed.

a. Set the POWER ON/OFF switch on the transmitter meter panel to OFF.

b. Set the POWER ON/OFF switch on the receiver meter panel to OFF.

CAUTION

Do not set the MAIN POWER, KLYSTRON BLOWER, or CABINET FANS circuit breakers on the power amplifier interlock panel to OFF while the cabinet fans and blower are operating. The cabinet fans and blower must continue to circulate air through the power amplifier cabinet to prevent damage to the klystron tube.

c. Press the BEAM SWITCH and MAIN POWER SWITCH on the power amplifier meter panel. The BEAM SWITCH indicator will light red and extinguish when the MAIN POWER SWITCH is pressed. The MAIN POWER SWITCH indicator will light white.

NOTE

The cabinet fans and blower will continue to run for approximately 4 minutes after the MAIN POWER SWITCH has been deactivated.

d. When the cabinet fans and blower stop operating, set the five circuit breakers on the power amplifier circuit breaker panel to OFF.

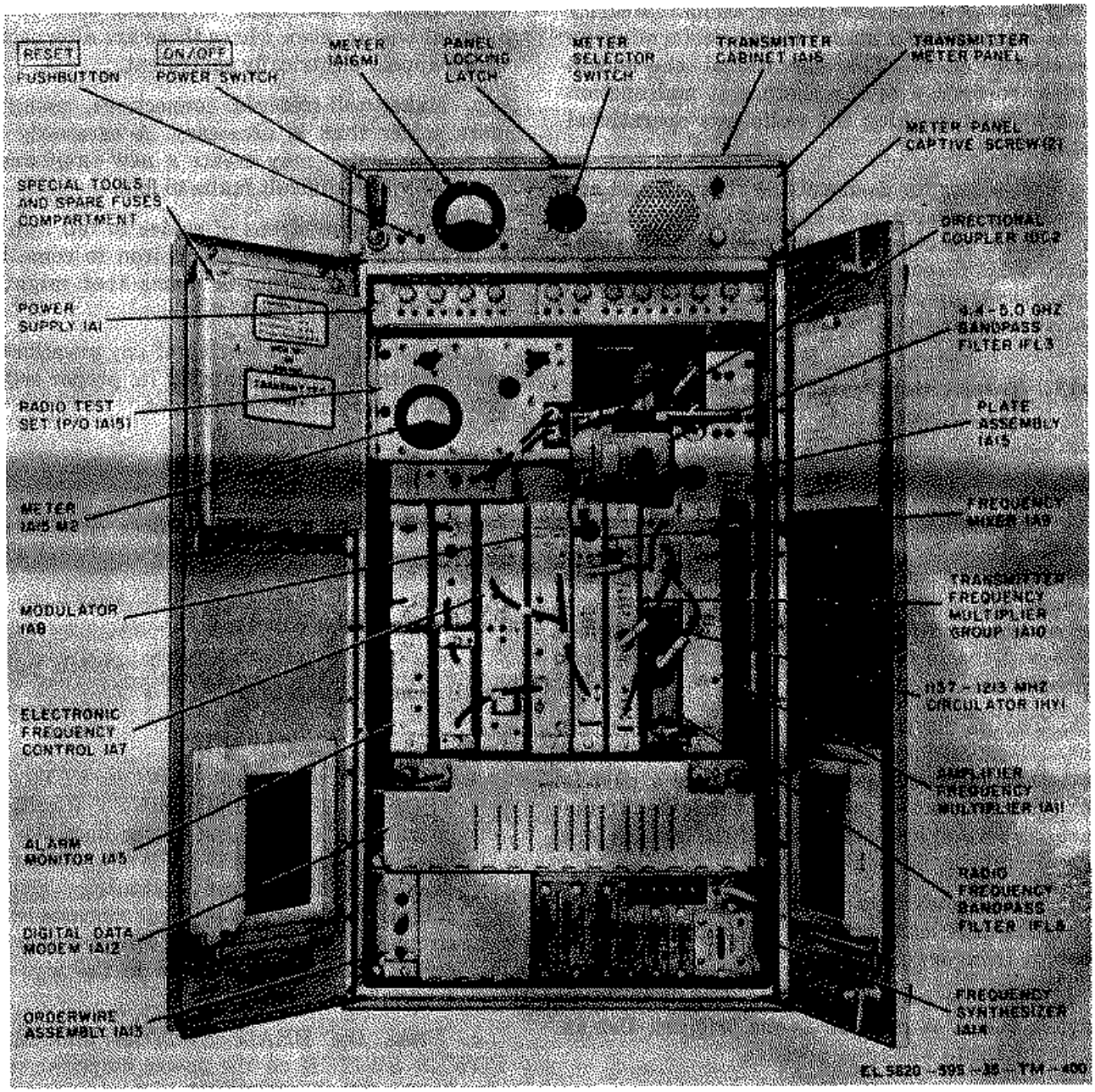


Figure 3-3. Transmitter, front view with cabinet doors open, parts location.

e. Disconnect external ac power input cable to AC POWER INPUT connector J7 on top of transmitter cabinet.

f. Disconnect external ac power input cable to AC POWER INPUT connector J5 on top of receiver cabinet.

g. Disconnect external ac power input cable AC POWER INPUT connector J1 on top of power amplifier cabinet.

3-13. Energize Radio Set

NOTE

Audible alarms will be generated during the starting procedure. To silence the audible alarm, press the RESET pushbutton (fig. 3-3) on the transmitter meter panel each time the audible alarm is heard.

a. Reconnect the transmitter external ac power input cable to AC POWER INPUT connector J7 (fig. 3-12); set the POWER ON'"OFF switch (fig. 3-3) to ON; and make the following transmitter checks:

(1) The 5 AMPS SLO-BLO neon fuse indicator on the transmitter meter panel is not lighted.

(2) All power supply 1A1 indicator lamps are lighted.

(3) The 5v and 28v indicator lamps on frequency synthesizer 1A14 are lighted.

b. Reconnect the receiver external ac power input cable to AC POWER INPUT connector J5; set the POWER ON'OFF switch (fig. 4-4) to ON; and make the following receiver checks:

(1) The meter panel POWER 8 AMPS, TDA A 1 AMP, and TDA B 1 AMP neon fuse indicators are not lighted.

(2) All power supply 2A3 indicator lamps are lighted.

(3) The 5v and 28v indicator lamps on frequency synthesizer 2A21 are lighted.

WARNING
ELECTROMAGNETIC RADIATION

Electromagnetic radiation hazards exist at the power amplifier waveguide output and within the directional path of the antenna! Do not energize the power amplifier until you are sure the shelter mounted waveguide switch is set to dummy load, the antenna is correctly positioned and that its radiation path is clear.

c. Set the shelter mounted waveguide switch to dummy load, if it is not in that position.

d. Reconnect the power amplifier external ac power input cable to AC POWER INPUT connector J1 and set the MAIN POWER, KLYSTRON BLOWER, CONTROL POWER, and CABINET FANS circuit breakers on the circuit breaker panel to ON.

e. On inverter regulator control 3A1, set the BEAM VOLT ADJ control fully counterclockwise.

f. If the MAIN POWER SWITCH on the power amplifier meter panel is not lighted green press the MAIN POWER SWITCH to light it green. The BEAM SWITCH should be lighted; red, if not, press the BEAM SWITCH to light it red.

NOTE

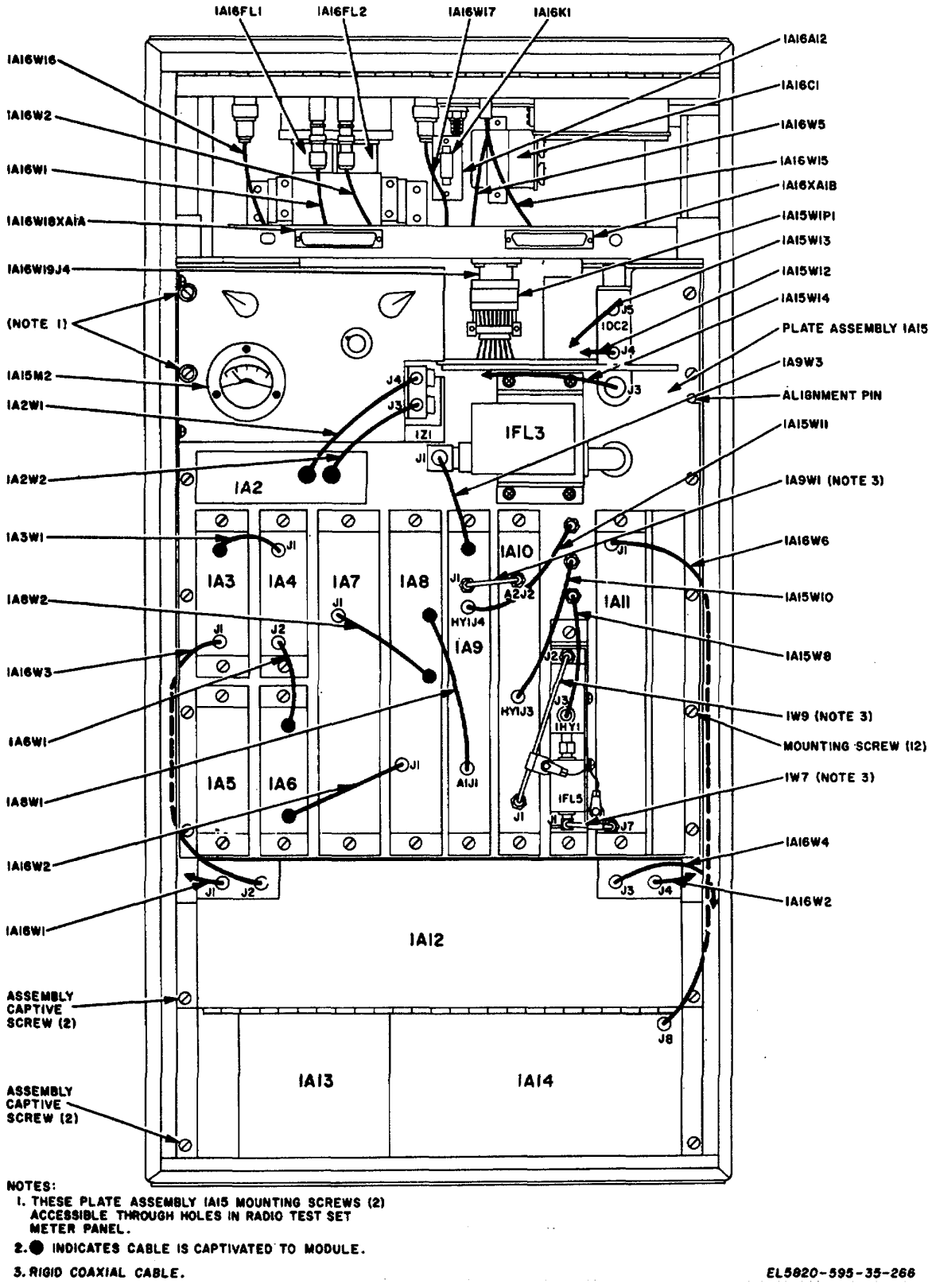
A time period of approximately 4 minutes will pass before the TIME DELAY indicator on the power amplifier meter panel lights green.

g. After the TIME DELAY indicator lights green, set the BEAM POWER circuit breaker on the power amplifier circuit breaker panel to ON.

h. Press the BEAM SVITCH on the power amplifier meter panel to light it green.

i. Check that BEAM VOLTAGE meter reads 300 to 600 volts. Slowly adjust the BEAM VOLT ADJ control clockwise until the BEAM VOLTAGE meter indicates approximately 7.5KV (green color area). If any instability or jumping of the BEAM CURRENT or BEAM. VOLTAGE meter is noticed, reduce the BEAM ADJ VOLTAGE to a level just below the point of instability and allow approximately five minutes of warm-up. Continue to increase the BEAM VOLTAGE ADJ control and warm up, If required, until a stable 7. 5KV beam voltage has been achieved.

j. Press the BEAM SWITCH on the power amplifier meter panel off and on. BEAM



NOTES:
1. THESE PLATE ASSEMBLY 1A15 MOUNTING SCREWS (2) ACCESSIBLE THROUGH HOLES IN RADIO TEST SET METER PANEL.
2. ● INDICATES CABLE IS CAPTIVATED TO MODULE.
3. RIGID COAXIAL CABLE.

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Figure 3-4. Transmitter, front view, locating modules, assemblies, coaxial cables, and piece parts.

SWITCH changes from green to red to green and BEAM VOLTAGE meter reading changes from 7500 volts to zero to 7500 volts.

k. Check that all power amplifier meter panel indicators except the LOW RF are lighted green. The LOW RF indicator may be lighted red or green.

l. Close and latch any open cabinet doors.

m. Notify the radio set operator that the radio set repairs are completed. Advise the radio set operator to confirm that the radio set is operational by performing the operator daily preventive maintenance checks and services (TM 11-5820-595-12).

3-14. Modules with Rigid Coaxial Cables (fig. 3-4)

CAUTION

Care must be exercised when removing or replacing any rigid coaxial cable to prevent bending or damaging the rigid coaxial cable.

Replacement of modules with rigid coaxial cables are covered in TM 11-5820-595-12.

3-15. Replacement of Parts on Transmitter Meter Panel

Prior to removing and replacing parts on the transmitter meter panel, deenergize the radio set (para 3-12).

a. Removal of Meter 1A16M1 (fig. 3-5).

(1) Loosen the two meter panel captive screws and lock the meter panel in its upward position using the panel locking latch.

(2) Remove the two self-locking nuts and washers from the meter terminals.

(3) Remove and tag the leads from the meter terminals.

(4) While holding the meter in place, loosen and remove the three self-locking nuts, washers and screws which secure the meter to the meter panel. Remove meter from the meter panel.

(5) Short the removed meter terminals with several turns of bus wire, to protect the meter movement, until the shorting bar of the new meter can be used.

b. Replacement of Meter 1A16M1.

(1) Place the new meter in position on the meter panel and use the hardware removed in a (4) to secure new meter 1A16M1 to the meter panel.

(2) Remove the two self-locking nuts, washers, and shorting bar from the meter terminals.

(3) Replace the tagged leads on their respective meter terminals and fasten lugs to terminals with hardware removed in step a(2).

(4) Replace the bus wire used to short the old meter terminals with the shorting bar removed from the new meter.

(5) Release the meter panel from its upright position and secure it in operational position with the two meter panel captive screws.

(6) Energize the radio set (para 3-13) and calibrate the new meter (para 3-35).

c. Removal of Indicator Light Assembly 1A16XDS1, XDS5, XDS10, XDS14, and XDS18 (fig. 3-5).

(1) Using finger nail slots on sides of lens assembly, pull lens assembly out approximately 5 8-inch (A, figure 3-6) and rotate the lens assembly 90°.

(2) Push lens inward against lens assembly to release tension on index keys, then pull complete lens assembly out of housing (B and D, figure 3-6).

(3) Unscrew two screws until the captive nuts reach rear of their travel range releasing housing from cover (C, figure 3-6).

(4) Loosen the two meter panel captive screws and swing the meter panel outward and upward and lock it into an upright position with the panel locking latch.

(5) Slide cover 6ff the housing away from the rear of the panel (D, figure 3-6).

(6) Release the meter panel locking latch and rotate meter panel downward until it rests against transmitter cabinet.

(7) Remove switch housing from meter panel, tag and unsolder each wire lead from each of the indicator assembly terminals (E, figure 3-6).

d. Replacement of Indicator Light Assembly 1A16XDS1, XDS5, XDS10, XDS14 and XDS18 (fig. 3-5).

(1) Solder leads removed in step c (7) above to terminals of replacement indicator light assembly.

(2) Insert housing of indicator lamp assembly in position through front of meter panel.

(3) Swing the meter panel upward and lock it into an upright position with the meter panel locking latch.

NOTE

Exercise care to prevent housing from slipping out of meter panel.

(4) Slip cover over housing from rear of meter panel until cover and housing fit snug against meter panel (D, figure 3-6).

(5) Release meter panel from the upright position and rotate it downward until it rests against transmitter cabinet.

(6) Tighten the two screws from front of meter panel (C, figure 3-6) to secure the housing to the cover.

(7) If required, for the new indicator lamp assembly, replace the new lens and diffuser (B, figure 3-6) with the lens and diffuser of replaced indicator lamp assembly.

(8) Insert complete lens assembly (A, figure 3-6) into housing so that the bulb board slot aligns with the housing index key (D, figure 3-6).

(9) Rotate lens assembly 90° so that lens and legend index is on top of light, then push lens assembly into housing.

(10) Finger tighten the two meter panel captive screws to secure the meter panel to transmitter cabinet.

(11) Energize the radio set (para 3-13).

(12) Check that the replacement indicator light assembly is lighted. Provided in the chart below are the normal color indications for each indicator on the meter panel.

Name of Indicator	Color lighted
RADIO TEST SET	Green
INTERLOCK	Green
RING	Green or amber
CNTRL ALARM	Green
TRAF	Green
SYNTH LOCK	Green
RF POWER	Green
REFL RF POWER	Green
CABLE TO RADIO MODEM	Green
RADIO TO CABLE MODEM	Green

e. Replacement of Potentiometers (1A16R2 through 1A16R7 (fig. 3-5). If any of the potentiometers (1A16R2 through 1A16R7) located on the transmitter meter panel are to be replaced; first deenergize the radio set (para 3-12), replace the defective potentiometer, energize the radio set (para 3-13), and perform the required calibration indicated in the chart below.

POTENTIOMETER CALIBRATION

Potentiometer	*Calibration procedure*
1A16R2, 1A16R3, 1A16R4	Calibration of transmitter and frequency multiplier metering circuits (para 3-40).
1A16R5	Calibration of transmitter reflected rf power metering circuit (para 339).
1A16R6	Calibration of transmitter rf power metering circuit (para 3-38).
1A16R7	Calibration of transmitter traffic metering circuit (para 337).

f. Removal of Meter Selector Switch 1A16S4 (fig. 3-5 and 8-14).

(1) Loosen, but do not remove, two allenhead set screws securing selector knob to meter selector switch 1A16S4 shaft, and remove knob from selector switch shaft.

(2) Loosen the two meter panel captive screws to release the meter panel from the transmitter cabinet and lock the meter panel in an upward position using the meter panel locking latch.

NOTE

When unsoldering leads to the selector switch, remove leads from the top switch deck first. Bend the removed leads out of the way to provide access ,to lower switch deck and prevent damage to wire insulation when unsoldering leads to the lower switch deck.

(3) Unsolder, remove and tag each lead routed from a cable harness or piece part on the meter panel to the terminals on the meter selector 3-26 switch 1A16S4 (fig. 8-14). Do not remove jumper leads between terminals.

(4) Release the meter panel from the upright position and rotate it downward until it rests against the transmitter cabinet.

(5) Remove hex nut and starwasher securing meter selector switch 1A16S4 to meter panel and remove the selector switch from the panel.

g. Replacement of Meter Selector Switch 1A16S4 (fig. 3-3, 3-5 and 8-14).

(1) Place replacement meter selector switch along side the removed meter selector switch. Prepare jumper leads for the lower and upper meter selector switch decks using the removed switch as a guide and solder the prepared jumper leads in their identical positions on the replacement meter selector switch.

(2) Mount replacement meter selector switch on meter panel aligning guide pin with guide hole on meter panel.

NOTE

Support replacement meter selector switch while releasing and lowering meter panel from its upright position.

(3) Secure meter selector switch to meter panel using starwasher and hex-nut removed in step f (5).

NOTE

When soldering leads to the meter selector switch, start reconnecting leads to the lower deck of meter selector switch first.

(4) Lock the meter panel in an upward position with the meter panel locking latch.

(5) Reconnect and solder the leads removed in step f(3) to their respective terminals on the meter selector switch.

(6) Release meter panel locking latch and rotate meter panel downward until resting against transmitter cabinet.

(7) Replace and secure the knob removed in step f(1).

(8) Rotate the meter selector switch and check that replaced leads do not interfere with the switch movement.

(9) Secure meter panel to transmitter cabinet with the two meter panel captive screws.

(10) Energize the radio set (para 3-13) and.: perform the transmitter metering checks (TM 11-5820-595-12).

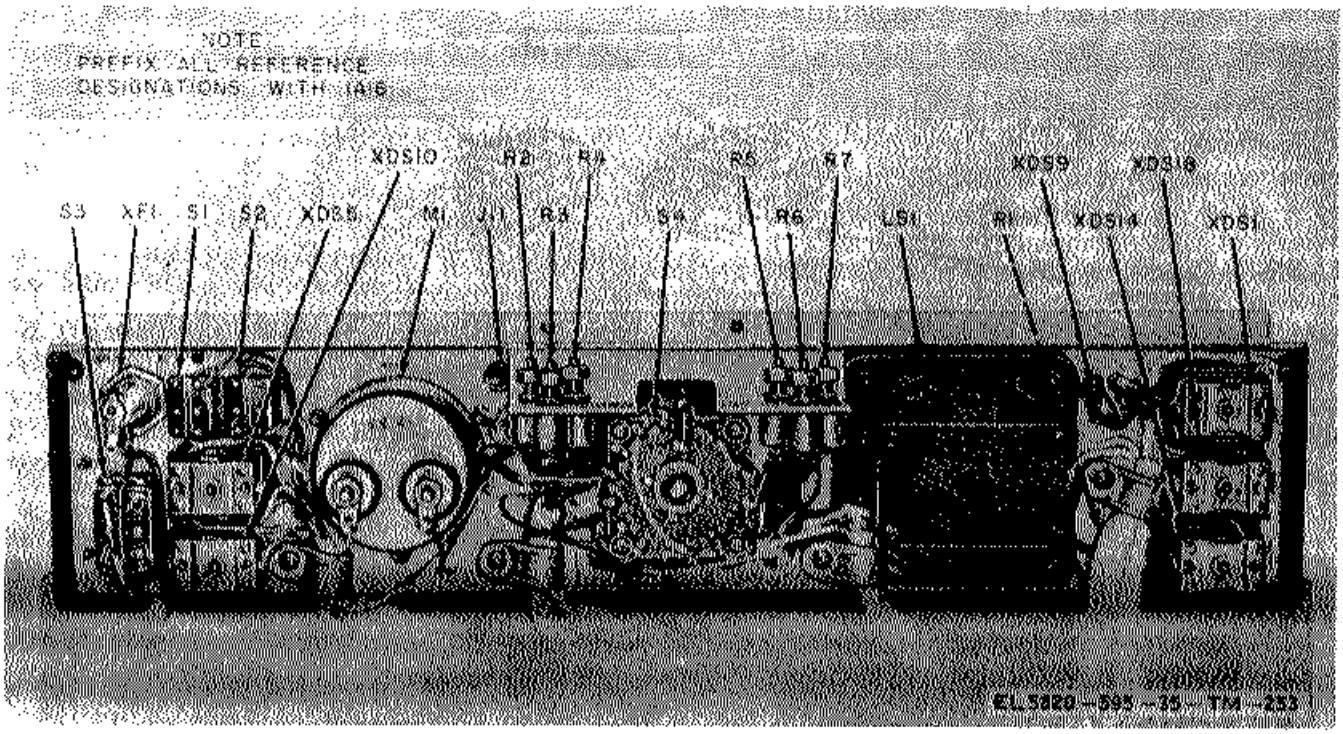

Figure 3-5. Transmitter meter panel, rear view, parts location.

3-16. Replacement of Power Supply Chassis 1A1A13

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Loosen the two meter panel captive screws and lock the meter panel in its upward position using the panel locking latch.

(3) To release power supply 1A1 from the transmitter cabinet; loosen the two power supply 1A1 captive screws (fig. 3-7) by alternately unscrewing each captive screw one or two turns at a time to prevent power supply 1A1 from binding against the transmitter cabinet walls.

(4) Slide power supply 1A1 out of transmitter cabinet approximately three inches by grasping the two power supply captive screws and bottom cover as shown in figure 3-7.

(5) Slide power supply 1A1 forward while tilting downward (fig. 3-7) to prevent damage to meter panel cables located above power supply 1A1. Continue this removal technique until power supply 1A1 is removed from transmitter cabinet.

(6) Alternately loosen, the two captive screws on 5/6v regulator 1A1A1 releasing it from power supply chassis 1A1A13, and then remove 1A1A1 from chassis (fig. 3-7).

(7) Repeat step (7) for: 5/6v regulators 1A1A2, 1AIA3 and 1AlA4; 12v regulators 1A1A6, 1A1A7, 1A1A8, and 1A1A9; and 15/28v regulators 1A1A10, 1A1A11, and 1A1A12.

(8) Remove the two screws securing blank panel 1A1A5 to power supply chassis (fig. 3-7) and remove blank panel 1A1A5.

b. Replacement.

(1) Insert 5/6v regulator 1A1A1 into replacement' power supply chassis 1A1A13 aligning printed wiring board on 1A1A1 with guide rails located on upper and lower portions of power supply chassis. Then slowly push the plug in component into the power supply chassis until the connectors are mated.

(2) Alternately tighten the two captive screws on 5/6 regulator 1A1A1 to secure the plug-in component to replacement power supply chassis.

(3) Repeat steps (1) and (2) for 5/6v regulator 1A1A2, 1A1A3 and 1A1A4.

(4) Mount blank panel 1A1A5 on power supply chassis and secure in place using the original mounting hardware.

(5) Repeat steps (1) and (2) for 12v regulators 1A1A6, 1A1A7, 1A1A8, and 1A1A9, and 15/

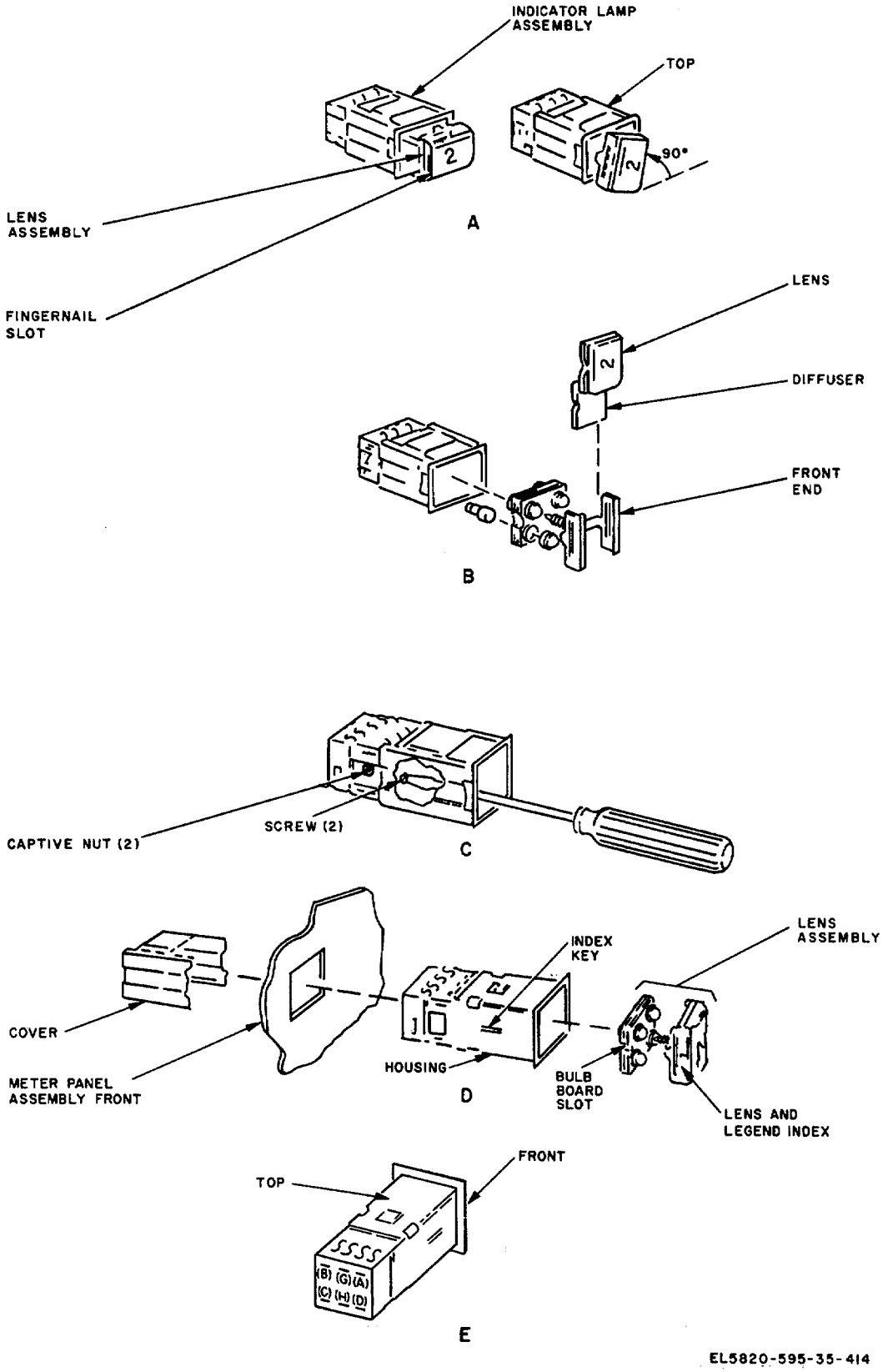

Figure 3-6. Removing indicator lamp assemblies from transmitter meter panel, typical.

28v regulators 1A1A10, 1A1A11 and 1A1A12 (fig. 3-7).

(6) Reinstall power supply 1A1 into transmitter cabinet by initially tilting power supply as shown in figure 3-7. Slowly slide power supply 1A1 into transmitter cabinet exercising care not to damage meter panel cables.

(7) Tilt power supply 1A1 upward to a level position when approximately three inches remain of the front part of power supply 1A1. Then push power supply 1A1 into transmitter cabinet until guide pins and connectors are mated.

(8) Alternately tighten the two power supply captive screws a few turns each until power supply 1A1 is securely fastened to transmitter cabinet.

(9) Release the meter panel from its upright TM 11-5820-595-35 position and secure it to the transmitter cabinet with the two meter panel captive screws.

(10) Energize the radio set (para 3-13).

3-17. Replacement of Parts in Power Supply Chassis 1A1A13

To replace any part in power supply chassis 1A1A1.3; remove power supply 1A1 from transmitter cabinet (para 3-16a) and refer to the following applicable replacement procedure for the part to be replaced. After the part has been replaced, replace power supply 1A1 in transmitter cabinet (para 3-16b). Parts located on terminal boards 1A1A13TB1 and 1A1A13TB2 (figs. 3-9 and 3-10) are removed using standard soldering techniques (para 3-11).

a. Removal of Power Supply Chassis Mounted

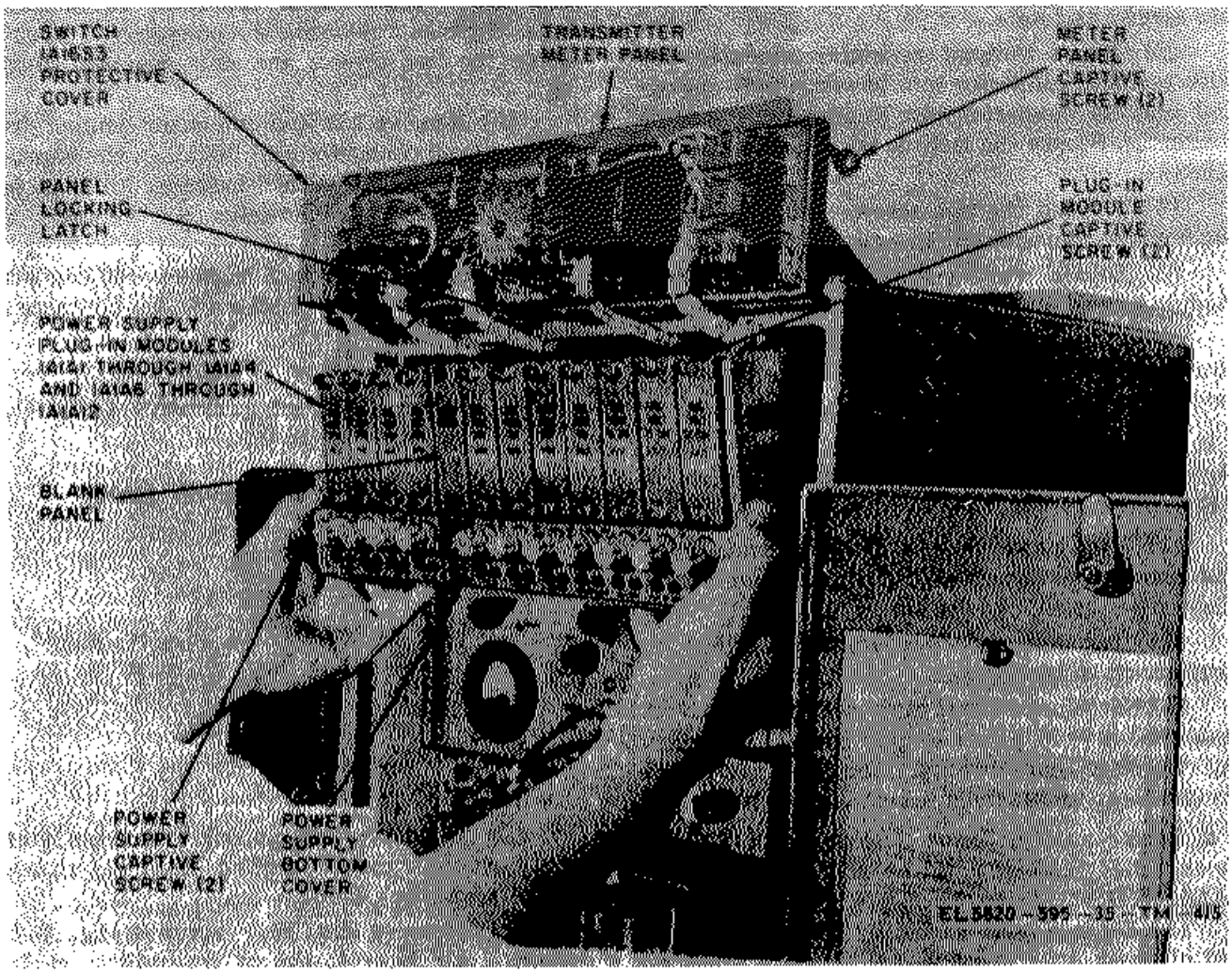

Figure 3-7. Removing power supply 1A1 from transmitter cabinet 1A16.

Module Connectors 1A1A13XA1 through 1A1A 13XA4 and 1A1A13XA6 through 1A1A13XA12 (fig. 3-8).

(1) Remove the ten screws and associated washers securing rear shield to power supply chassis.

(2) Tag and unsolder wires connected to module connector terminals of the connector to be replaced.

(3) Remove the two screws and nuts securing module connector to power supply chassis and remove the connector.

b. Replacement of Power Supply Chasis Mounted Module Connectors 1A1A13XAl through 1A13A1XA4 and 1A1A13XA6 through 1A1A1S XA12 (fig. 3-8).

(1) Mount replacement module connector in place of removed connector using the two screws and nuts removed in step a(3). Do not tighten the two screws and nuts.

(2) Insert voltage regulator module used with replaced connector into power supply chassis and seat its connector into replacement module connector. Secure the module with its two captive screws.

(3) Tighten the two screws and nuts securing module connector to power supply chassis.

(4) Solder wires removed in step a(2) to module connector terminals.

(5) Mount and secure the rear shield to power supply chassis using the' ten screws and associated' washers removed in step a(1l).

c. Removal of Lamp Sockets 1A1A13XDS1 through 1A1A13XDS4 and 1A1A13XDS6 through 1A1A13XDS12 (fig. 3-8).

(1) Turn power supply chassis upside down and remove the 15 screws securing bottom access plate to power supply chassis.

(2) Tag and unsolder wires connected to lamp socket to be replaced.

(3) Force press fitted lamp socket through its mounting hole in power supply chassis by pressing terminal end toward mounting hole and remove lamp socket from power supply chassis.

d. Replacement of Lamp Sockets 1A1A13XDS1 through 1A1A13XDS4 and 1A1A13XDS6 through 1A1A13XDS12 (fig. 3-8).

(1) Replace lamp socket by forcing terminal end of press fitted lamp socket through front of mounting hole in power supply chassis by pressing lamp end until mounted snugly against power supply chassis frame.

(2) Solder wires removed in step c(2) to lamp socket terminals.

(3) Mount and secure the bottom access plate to power supply chassis using the 15 screws removed in step *c*(1).

e. Removal and Replacement of Mounted Chassis Connectors 1A1A13P1 and 1A1A13P2 (fig. 3-8).

(1) Turn power supply chassis upside down and remove the 15 screws securing bottom access plate to power supply chassis.

(2) If a connector contact requires replacement refer to the procedures provided in paragraph 3-32c for removal and replacement of connector contacts and proceed to step (7).

(3) If the connector requires replacement remove the two screws and nuts securing connector to power supply chassis.

(4) Remove connector from mounting hole and insert replacement connector in mounting hole. Tighten replacement connector in position using the two screws and nuts removed in step (3).

(5) Remove a wired connector contact from the removed connector and install in the identical replaced connector contact location. Refer to paragraph 3-32c for connector pin removal and replacement.

(6) Repeat step (5) for each wired connector contact until transfer of all connector contacts are completed.

(7) Mount bottom access plate to power supply chassis using the 15 screws removed in step (1).

3-18. Replacement of Blower Motor 1A16B1
(fig. 3-11)

NOTE

115 vac is routed to blower meter 1A16B1. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector J7 before performing this procedure.

a. Removal.

(1) Remove power supply 1A1 from transmitter' cabinet by performing steps (1) through (5) of paragraph 3-16a.

(2) Remove the four screws (fig. 3-11) securing air filter to top of transmitter cabinet and remove air filter.

(3) While supporting blower motor 1A16B1 from inside of transmitter cabinet, loosen the four

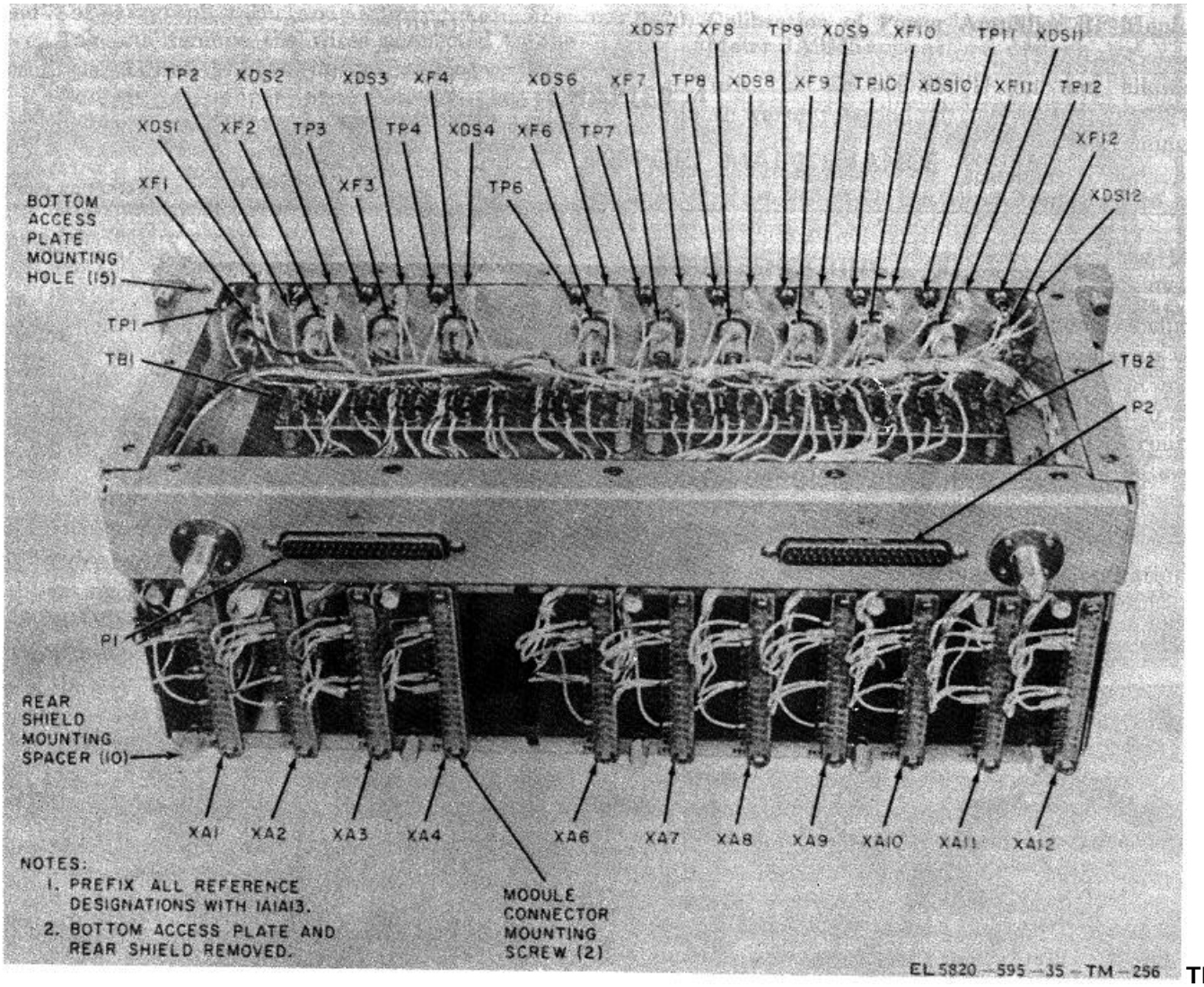

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Figure 3-8. Transmitter power supply chassis 1A1A1S, rear bottom view, partially disassembled, parts location.

synclamp screws (fig. 3-11) securing blower motor 1A16B1 to transmitter cabinet. Each screw has a synclamp which clamps the blower motor housing to the top of transmitter cabinet.

(4) Tilt blower motor housing upward and slide past the synclamps, then lower blower motor 1A16B1 into transmitter cabinet.

(5) Tag wires connected to blower motor 1A16B1 terminals (fig. 3-11). Remove three screws which secure the wire lugs to blower motor 1A16B1 terminals. The lugs are soldered to the tagged wires.

(6) Remove blower motor 1A16B1 from transmitter cabinet.

b. Replacement.

(1) Check that AIR FLOW arrow (printed on side of replacement blower motor 1A16B1) is pointing upward, and insert replacement blower motor 1A16B1 into upper right section of transmitter cabinet. Connect wire lugs to blower motor 1A16B1 terminals using three screws removed in step a(5).

(2) Position blower motor 1A16B1 against top wall of transmitter cabinet between the four synclamps. Align the synclamps with blower motor 1A16B1 as shown in figure 3-11.

(3) Secure blower motor 1A16B1 to transmitter

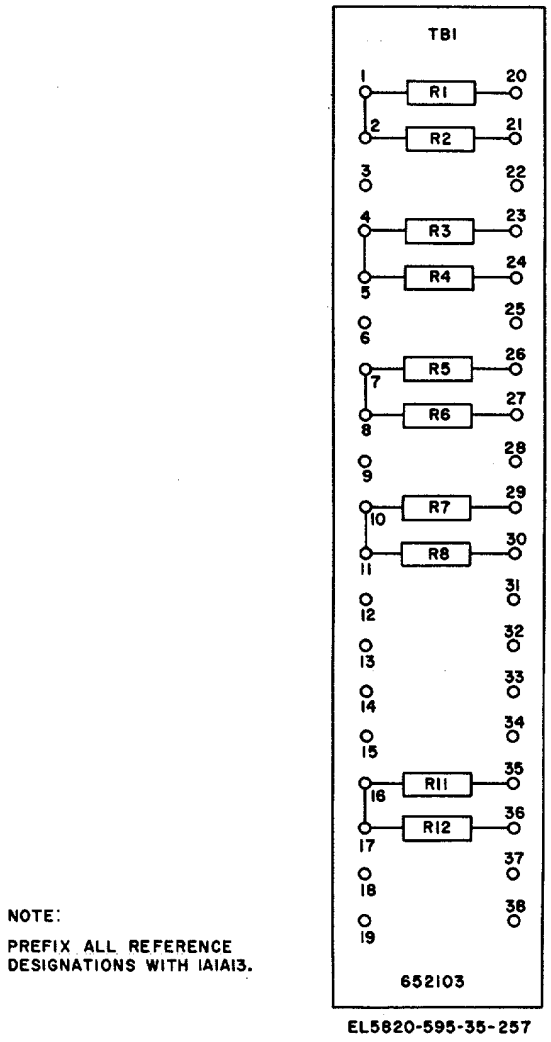


Figure 3-9. Transmitter power supply chassis terminal board 1A1A1STB1, top view, parts location.

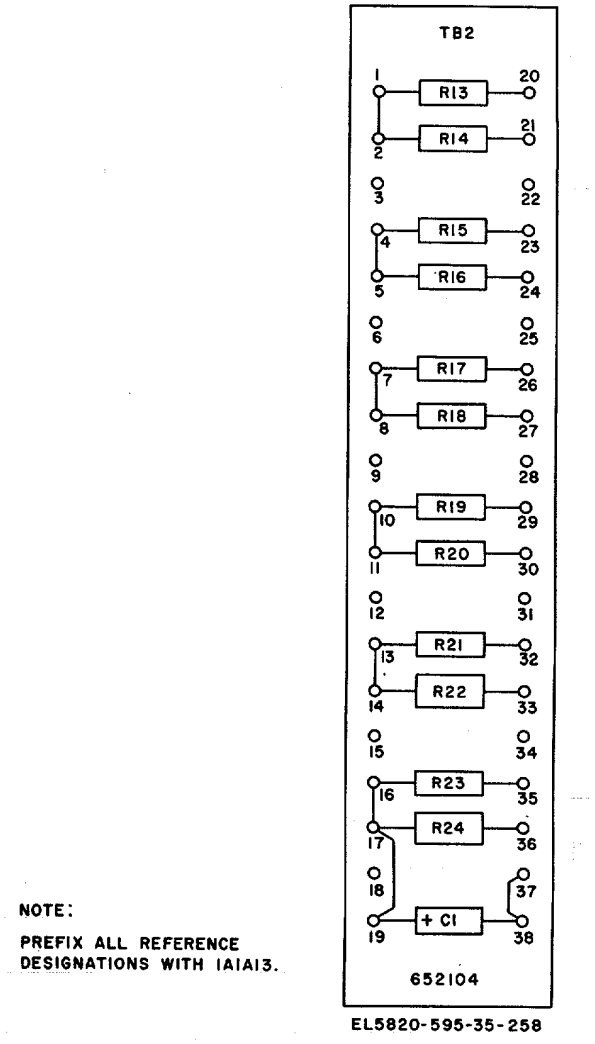


Figure 3-10. Transmitter power supply chassis terminal board 1A1A1STB1, top view, parts location.

cabinet by tightening the four screws connected to the synclamps.

(4) Mount air filter to top of transmitter cabinet and tighten in place using the four screws removed in step a(2).

(5) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (9) of paragraph 3-16b.

(6) Energize the radio set (para 3-13). Check blower motor of 1A16B1 operation after performing step a of paragraph 3-13 by placing a hand over the air filter on top of the transmitter cabinet to feel if air is being blown out of the transmitter cabinet through the air filter.

3-19. Replacement of Capacitor 1A16C1

WARNING

115 vac is routed to capacitor 1A16C1. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector J7 before performing this procedure.

a. Removal.

(1) Remove power supply 1A1 from transmitter cabinet by performing steps (1) through (5) of paragraph 3-16a.

(2) Remove the two nuts securing capacitor 1A16C1 mounting bracket to rear wall of transmitter cabinet (fig. 3-4).

(3) Tag and unsolder the two wires connected to capacitor 1A16C1 terminals.

b. Replacement.

(1) Insert replacement capacitor 1A16C1 into cabinet and solder the two wires removed in step a (3) to capacitor 1A16C1.

(2) Insert capacitor mounting bracket over

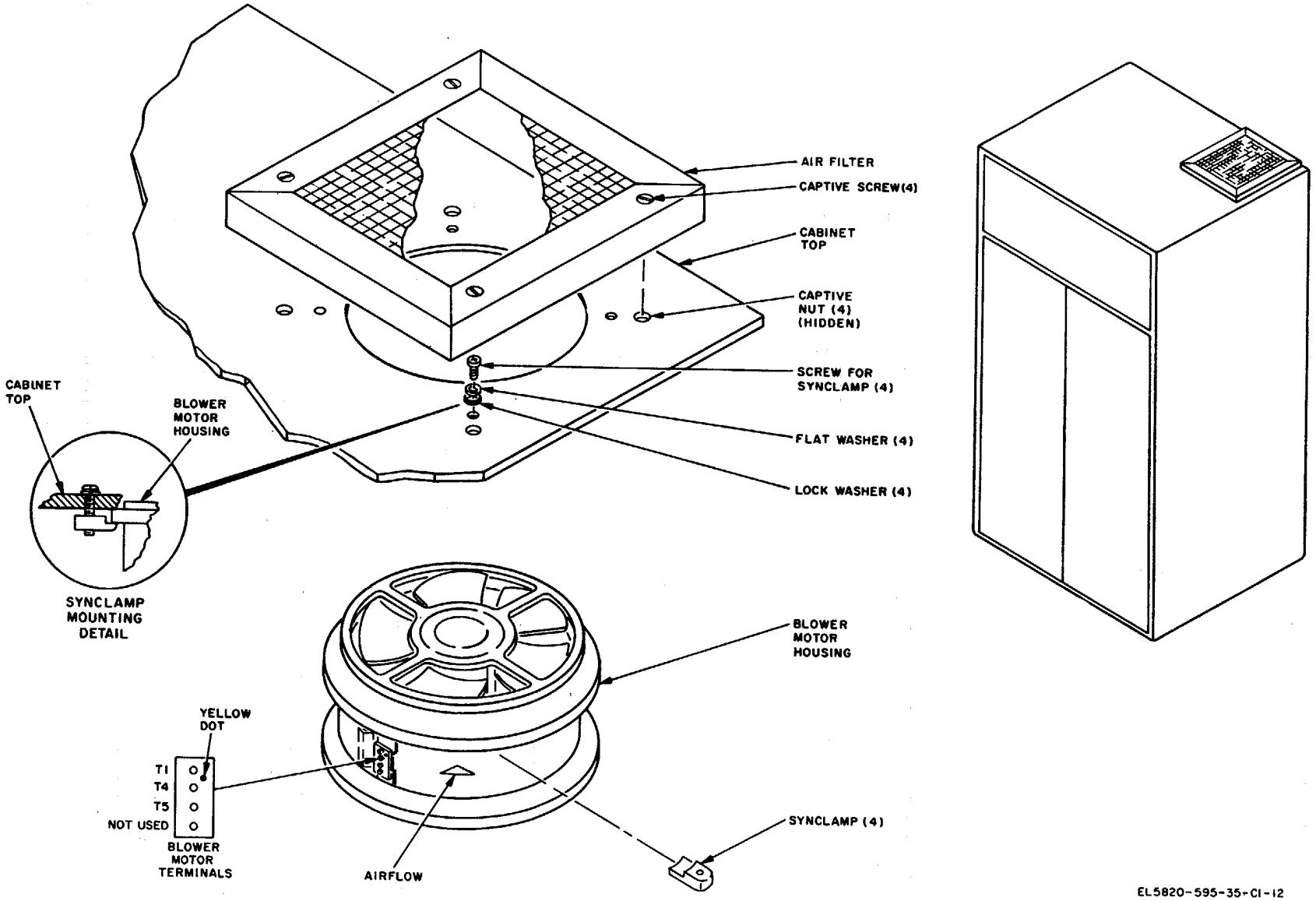


Figure 3-11. Removing blower motor 1A16B1 from transmitter cabinet 1A16, typical.

replacement capacitor 1A16C1, and then place the capacitor mounting bracket on the threaded studs on rear wall of transmitter cabinet (fig. 3-4).

(3) Replace and tighten the two nuts securing capacitor mounting bracket to rear wall of transmitter cabinet.

(4) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (9) of paragraph 3-16b.

(5) Energize the radio set (para 3-13). Check operation of blower motor 1A16B1 by placing a hand over the air filter on top of the transmitter cabinet to feel if air is being blown out of transmitter cabinet.

3-20. Replacement of Input Filter 1A16FL1 or 1A16FL2

WARNING

115 vac is applied to input filters 1A16FL1 and 1A16FL2. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector J7 (fig. 3-12) on top of the transmitter cabinet.

a. Removal.

(1) Remove power supply 1A1 from transmitter cabinet by performing steps (1) through (5) of paragraph 3-16a.

(2) Disconnect external coaxial cables from connectors J2 and J3 on top of transmitter cabinet (fig. 3-12).

(3) Remove the mounting hardware securing connectors J2 and J3 to top of transmitter cabinet (fig. 3-12).

(4) From inside transmitter cabinet lower connector assemblies of coaxial cables 1A16W1 and 1A16W2 (fig. 3-4). Replace mounting hardware removed in step (3), then tag cables and allow to rest on plate assembly.

(5) From inside transmitter cabinet disconnect coaxial cables 1A16W16 and 1A16W17 (fig. 3-4) from connectors J9 and J10 respectively and allow to rest on plate assembly.

(6) Remove the 4 mounting screws securing component clamp to bracket on rear wall of transmitter cabinet (fig. 3-12). Remove component clamp.

(7) From inside transmitter cabinet, unsolder, remove and tag wire lead to ground terminal El on right side of box (fig. 3-12).

(8) Remove 4 mounting screws from top of transmitter cabinet releasing filters and box into transmitter cabinet (fig. 3-12).

(9) Position input filters and box to provide access to bottom terminals on input filter 1A16FL1 and 1A16FL2. Then unsolder, remove and tag each lead to bottom terminals on input filter 1A16FL1 and 1A16FL2.

(10) Carefully remove input filters and box from transmitter cabinet.

(11) Remove the four screws securing cover to box and carefully raise cover from box to provide access to input filter 1A16FL1 and 1A16FL2 terminals. Unsolder and remove wire lead from the input filter to be replaced.

(12) Remove the nut and washer securing the input filter to be replaced to the cover and then remove the input filter.

b. Replacement.

(1) Remove mounting nut from replacement input filter, then install and secure replacement input filter to cover with nut just removed.

(2) Place cover with input filter 1A16FL1 and 1A16FL2 close' to upper half of box and solder wire lead removed in step a(11) to the input filter.

(3) Place cover on box being careful that the leads from input filter 1A16FL1 and 1A16FL2 to connector J7 are not crimped. Tighten cover to box using the four screws removed in step a(11).

(4) Carefully position box assembly in cabinet so that nomenclature on cover is visible when looking into the cabinet. Tilt box assembly providing access to bottom terminals of input filters 1A16FL1 and 1A16FL2 and solder the wire leads removed in step a(9) to each input filter terminal.

(5) Solder the lead removed in step a(7) to terminal El on right side of the box.

(6) Position and lift box aligning mounting holes with transmitter cabinet mounting holes.

Secure box to transmitter cabinet using hardware removed in step a(8).

(7) Replace component clamp and secure in place using the screws removed in step a(6).

(8) Remove connector mounting hardware, and mount and secure connectors J2 and J3 to top of transmitter cabinet.

(9) Reconnect coaxial cables J9 and J10 removed in step a(5).

(10) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (10) of paragraph 3-16b.

(11) Energize the radio set (para 3-13). Check that power supply 1A1 indicators are

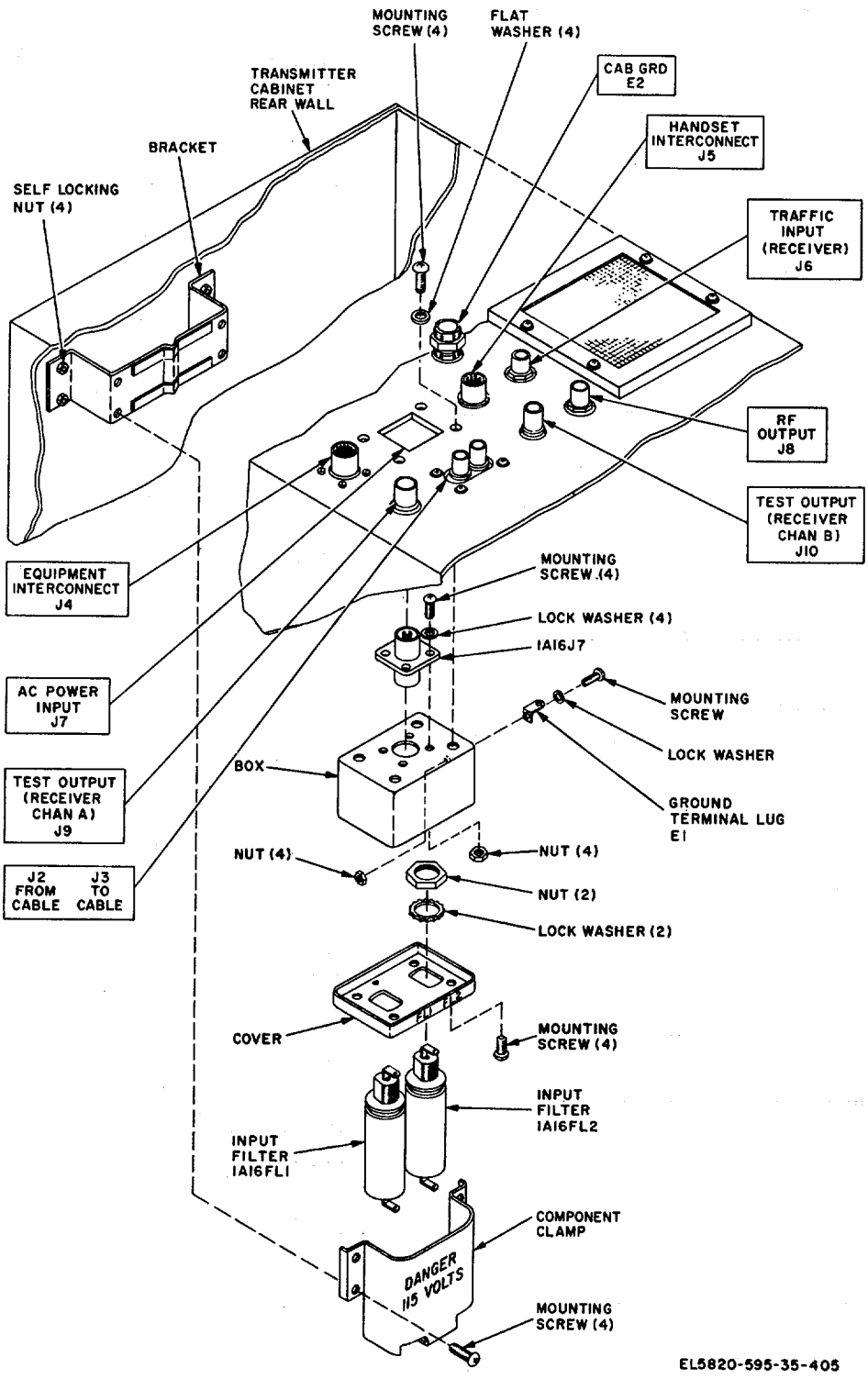


Figure 3-12. Removing input filters 1A16FL1 and 1A16FL2 from transmitter cabinet 1A16, typical.

lighted green in accordance with procedural step 3-13 a(2).

3-21. Replacement of Parts on Relay Plate 1A16A12

Piece parts mounted on relay plate 1A16A12 (fig. 3-4) which are replaceable are: relay 1A16K1, relay socket 1A16XK1, capacitor 1A16C2, and resistor 1A16R9. The following procedures will detail the steps necessary to remove all the piece parts as a single item.

a. Removal.

(1) Remove power supply 1A1 from transmitter cabinet by performing steps (1) through (5) of paragraph 3-16a.

(2) Loosen and remove the two relay mounting screws securing relay 1A16K1 to relay socket (fig. 3-13). Remove relay 1A16K1 from relay socket.

(3) Remove the two relay plate mounting screws securing relay plate 1A16A12 to the relay plate mounting studs on transmitter cabinet rear wall.

(4) Rotate relay plate to permit access to rear of relay socket 1A16XK1 mounted on relay plate.

NOTE

Save resistor R9 and capacitor C2 if the relay socket is to be replaced.

(5) Unsolder and remove resistor 1A16R9 leads from standoff terminal E10 and relay socket terminal pin 4.

(6) Unsolder and remove capacitor 1A16C2 leads from standoff terminal E10 and relay socket terminal pin 2.

(7) Unsolder and tag each lead from relay socket 1A16XK1 and remove relay plate with relay socket mounted on it from transmitter cabinet.

(8) Loosen and remove the two relay socket mounting screws securing relay socket to relay plate.

b. Replacement.

(1) Mount and secure replacement relay socket on relay plate using mounting hardware removed in step a(8).

(2) Position relay plate and relay socket inside transmitter cabinet to enable the leads removed in step a(7) to be resoldered to the relay socket terminals. Then solder each lead to their respective relay socket terminals. Replace and solder capacitor 1A16C2 and resistor 1A16R9 to correct terminals if they were saved. If either piece part was to be replaced, use an equivalent new part.

(3) Position the relay plate to align relay plate mounting holes with relay plate mounting studs and secure relay plate to mounting studs using hardware removed in step a(3).

(4) Insert relay 1A16K1 into relay socket carefully to prevent damaging or bending the relay terminal pins. Press relay into relay socket until relay is firmly seated in relay socket.

(5) Secure relay to relay socket using hardware removed in step a(2).

(6) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (9) of paragraph 3-16b.

(7) Energize the radio set (para 3-13). Check that INTERLOCK indicator on meter panel lights red and then green when the shelter mounted waveguide switch is rotated from dummy load position to antenna or vice versa.

3-22. Replacement of Parts within Radio Test Set Enclosure (fig. 3-3)

Meter 1A15M2 and switch 1A15S6 (fig. 3-15), which are mounted on the radio test set meter panel, are replaceable only when the radio test set meter panel is removed from plate assembly 1A15. Other piece parts that require the same meter panel removal are variable attenuators 1AT3 and 1AT4, directional coupler 1DC1, and crystal mixer 1Z1 (fig. 3-14). The following procedures will detail the steps necessary to remove all the piece parts.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Loosen the two allen head set screws in each selector knob and remove each knob.

(3) Remove the two left side mounting screws (fig. 3-14). Tag and identify all removed screws and hardware for replacement purposes.

(4) Remove the eight plate mounting screws, the two U clamp mounting screws and the two sets of the three attenuator mounting screws identified in figure 3-14.

(5) Disconnect coaxial cables 1A2W1 and 1A2W2 (fig. 3-4) from crystal mixer 1Z1 connectors J4 and J3 (fig. 3-14).

(6) Pull meter panel (fig. 3-15) away from radio test set enclosure until meter panel is clear; of shafts on variable attenuators 1AT3 and 1AT4, then lower the meter panel.

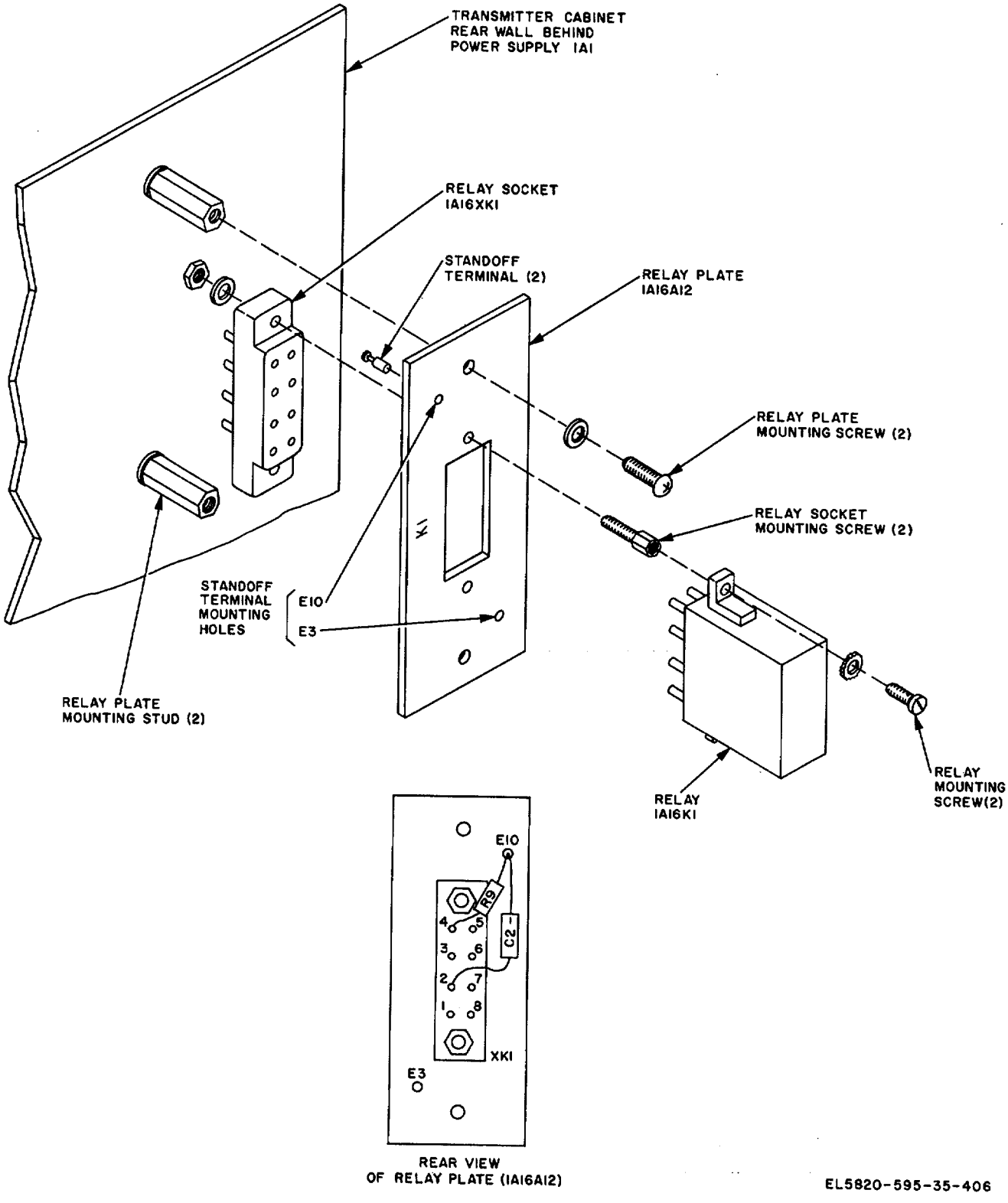


Figure 3-13. Disassembly of parts on transmitter relay plate 1A16A12.

(7) Remove the nut, lockwasher and wire lug connected to each terminal of meter 1A15M2. Tag each wire removed from meter terminals.

(8) Remove the three meter mounting screws, lockwashers and nuts securing meter 1A15M2 to radio test set meter panel and remove the meter.

(9) Short the meter terminals with several turns of bus wire or shorting bar to protect the meter movement. For meter replacement only, continue at step b(10).

(10) Tag and unsolder wires connected to rotary switch 1A15S6.

(11) Remove the nut and washer (from front of radio test set meter panel) securing rotary switch 1A15S6 shaft to meter panel and remove switch. For switch replacement only, continue at step b(8).

(12) Remove power supply 1A1 from transmitter cabinet by performing steps (2) through (5) of paragraph 3-16 a.

(13) Disconnect coaxial cables 1A16W16 and 1A16W17 (fig. 3-4) from connectors 1AT3J2 and 1AT4J2 (fig. 3-17) (located at rear of radio test set enclosure).

(14) Disconnect coaxial cable connector 1A1-5W14P2 from crystal mixer connector 1Z1J2 (fig. 3-15).

(15) Note the position of "U" clamp (fig. 3-14) around crystal mixer 1Z1 for replacement purposes. Pull variable attenuators 1AT3 and 1AT4, crystal mixer 1Z1 power divider 1DC1, and coupler 1CP3 forward out of radio test set enclosure (fig. 3-15) as a complete assembly and remove "U" clamp.

(16) Disconnect mating type N connectors (fig. 3-15) as required, to separate variable attenuators 1AT3 and 1AT4, power divider 1DC1, crystal mixer 1Z1, and coupler 1CP3 from each other.

b. Replacement.

(1) Assemble variable attenuators 1AT3 and 1AT4, power divider 1DC1, crystal mixer 1Z1 and coupler 1CP3 as a complete assembly (fig. 3-15).

(2) Place "U" clamp around crystal mixer 1Z1 in approximate position noted in step a(15).

(3) Insert the complete assembly of step (1) including "U" clamp into radio test set enclosure. Push the type N connector on rear of each variable attenuator through the rubber grommets mounted on plate assembly 1A15 until variable attenuator standoffs are flush with radio test set enclosure lips.

NOTE

The depth of the assembly within the radio test set enclosure is sufficient so that the variable attenuator standoffs (3 screw mounts each) are flush with radio test set enclosure lips. Check that the "U" clamp is properly positioned for the radio test set meter panel two screws used to secure crystal mixer 1Z1 in its correct assembled position.

(4) Connect coaxial cable 1A15W14P2 to crystal mixer connector 1Z1J2 (fig. 3-15).

(5) Connect coaxial cables 1A16W16 and 1A16W17 (fig. 3-4) to connectors 1AT3J2 and 1AT4J2 (fig. 3-17) respectively.

(6) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (9) of paragraph 3-16b.

(7) Rotate knob shafts on variable attenuators 1AT3 and 1AT4 until the red dot on variable attenuator knob shaft aligns with the red dot on the variable attenuator plate (T + 30 position). If variable attenuators 1AT3 and 1AT4, power divider 1DC1, and crystal mixer 1Z1 were the only piece parts replaced, continue replacement at step (14).

(8) Mount switch 1A15S6 to meter panel and secure to meter panel using hardware removed in step a(ll).

(9) Solder the wires removed in step a(10) to switch 1A15S6 terminals. For switch 1A15S6 replacement only, continue at step (14).

(10) Mount replacement meter 1A15M2 to meter panel and secure in place using hardware removed in step a(8).

(11) Remove the two self-locking nuts and washers from the meter terminals, then remove the shorting bar from the meter terminals.

(12) Connect the wire lugs, lockwashers and nuts removed from meter 1A15M2 in step a(7) to the replacement meter and then tighten nuts.

(13) Remove the bus wire used to short the replaced meter terminals. Place the shorting bar removed from the new meter on the terminal lugs of the old meter and fasten in place with its terminal hardware.

(14) Hold crystal mixer 1Z1 "U" clamp in place using needle nose pliers and align the radio test set meter panel mounting holes with those of the radio test set enclosure lips (fig. 3-15).

(15) Replace and finger tighten the two U clamp mounting screws securing crystal mixer 1Z1 "U" clamp to meter panel.

(16) Replace and finger tighten the remaining eight plate mounting screws and two sets of three attenuator mounting screws removed in step a (4).

(17) Replace and finger tighten the two left side mounting screws securing left side of radio test set meter panel to left side of transmitter cabinet wall.

(18) Tighten all radio test set meter panel mounting screws firmly in place.

(19) Position the two attenuator knobs to indicate T +30 and secure in place with the set screws (two per knob). Replace the radio test set meter selector switch knob checking that positions correlate with knob indications and secure it in place with the two set screws.

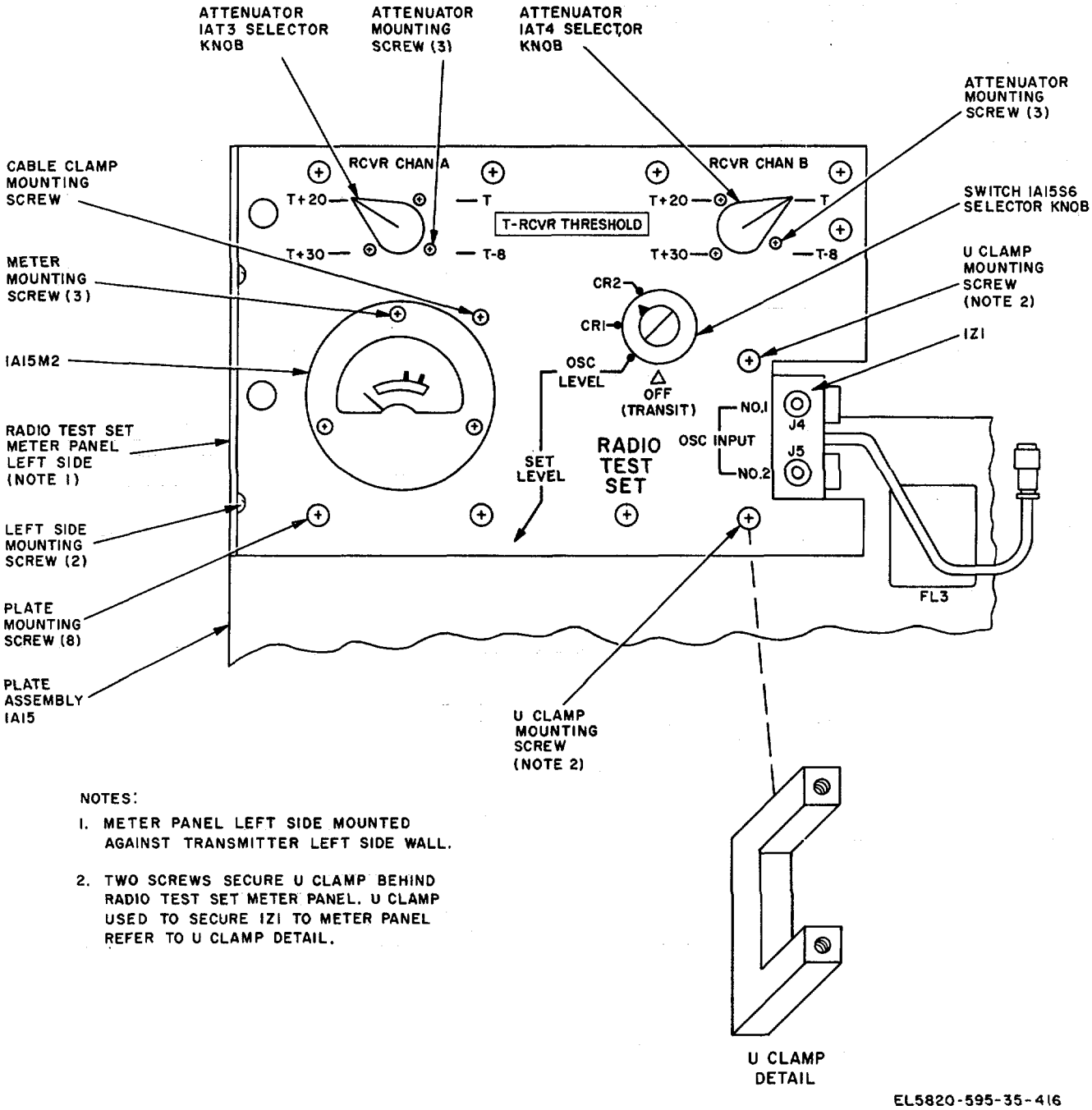


Figure 3-14. Transmitter radio test set, front view, partical cut-away view, showing U-clamp.

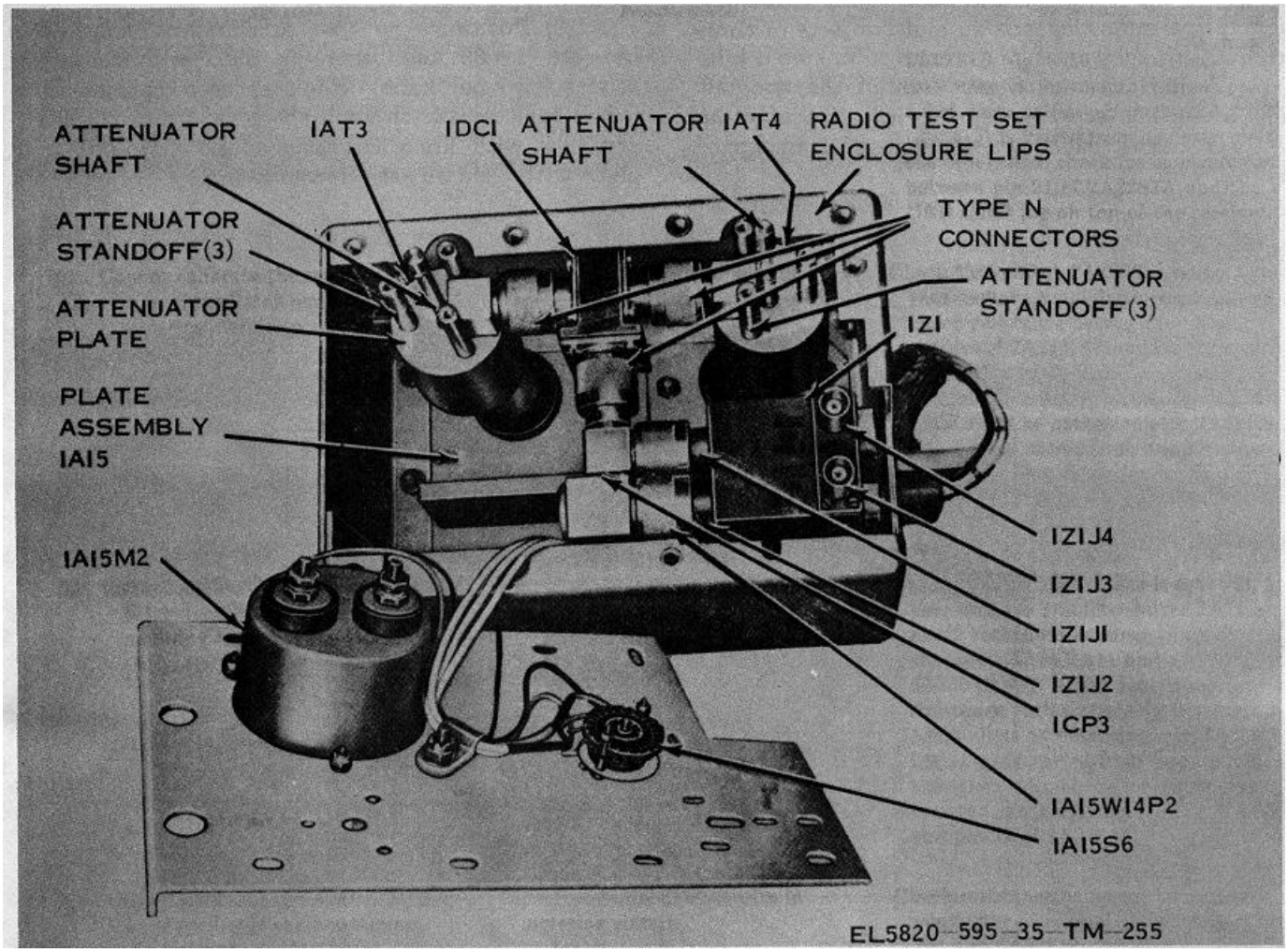


Figure 3-16. Transmitter radio test set, front view with meter panel removed, parts location.

(20) Connect coaxial cables 1A2W1 and 1A2W2 to crystal mixer 1Z1 connectors J4 and J3 respectively.

(21) Energize the radio set (para 3-13). Perform radio test set calibration (para 3-41).

3-23. Replacement of 4.45.0 GHZ Circulator 1A9HY1. (figs. 3-3 and 8-82).

a. Removal.

(1) Deenergize the radio set (para 3.12).

CAUTION

The steps referenced for removal of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(2) Remove frequency mixer 1A9 from plate assembly 1A15 (TM 11-5820-95-12).

(3) Loosen the two screws (rear side of 1A9 enclosure) securing crystal mixer 1A9A1 to frequency mixer 1A9 enclosure (TM 11-5820-595-12).

(4) Disconnect the mating type TNC connector between 4.4-5.0 GHz circulator 1A9HY1 and crystal mixer 1A9A1.

(5) Slide crystal mixer 1A9A1 away from 4.45.0 GHz circulator 1A9HY1 until it is free of the mating TNC connector, then remove crystal mixer 1A9A1 from the frequency mixer 1A9 enclosure.

(6) Remove the four screws (rear side of 1A9 enclosure) securing 4.4-5.0 GHz circulator 1A9HY1 to the frequency mixer 1A9 enclosure.

(7) Using a 56-inch open end wrench, loosen the nut securing rigid coaxial cable 1A9W2 to the INPUT J1 connector on 4.4-5.0 GHz circulator 1A9HY1.

(8) Carefully slide 4.4-5.0 GHz circulator 1A9HY1 toward the bottom of the frequency mixer 1A9 enclosure until the connector pin in coaxial cable 1A9W2 is free.

(9) Lift 4.4-5.0 GHz circulator 1A9HY1 for clearance and disconnect coaxial cable 1A9W3 from the OUTPUT J3 connector on 4.4-5.0 GHz circulator 1A9HY1.

(10) Remove 4.4-5.0 GHz circulator 1A9HY1 from the frequency mixer 1A9 enclosure.

b. Replacement.

(1) Insert replacement 4.4-5.0 GHz circulator 1A9HY1 into frequency mixer 1A9 enclosure and connect coaxial cable 1A9W3 to the OUTPUT J3 connector on 4.4-5.0 GHz circulator 1A9HY1.

(2) Carefully mate the connector pin on rigid coaxial cable 1A9W2 to the INPUT J1 connector on 4.4-5.0 GHz circulator 1A9HY1 and then tighten the connector nut on rigid coaxial cable 1A9W2.

(3) Install the four screws securing 4.4-5.0 GHz circulator 1A9HY1 to the frequency mixer 1A9 enclosure, but do not tighten the four screws at this time.

(4) Install crystal mixer 1A9A1 into frequency mixer 1A9 enclosure.

(5) Connect and tighten the mating type TNC connector between crystal mixer 1A9A1 and 4.4-5.0 GHz circulator 1A9HY1.

(6) Tighten the four screws securing 4.4-5.0 GHz circulator 1A9HY1 to frequency mixer 1A9 enclosure, then tighten the two screws securing crystal mixer 1A9A1 to the frequency mixer 1A9 enclosure.

(7) Replace frequency mixer 1A9 (TM 11-5820-595-12).

NOTE

Check that RF POWER indicator on transmitter meter panel is lighted green after performing step a of paragraph 3-13.

(8) Energize the radio set (para 3-13). Perform the calibration of transmitter frequency multiplier metering circuits (para 3-40).

3-24. Replacement of 2275-2425 MHz Circulator 1A10HY1 (fig. 3-3 and 8-83)

a. Removal.

(1) Deenergize the radio set (para 3-12).

CAUTION

The steps references for removal of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(2) Remove frequency multiplier group 1A10 from plate assembly 1A15 (TM 11-5820-595-12).

(3) Loosen the two screws (rear side of 1A10 enclosure) securing 3rd frequency multiplier 1A10A2 to the frequency multiplier group 1A10 enclosure (TM 11-5820-595-12).

(4) Disconnect the mating type TNC connector between 2275-2425 MHz circulator 1A10HY1 and 3rd frequency multiplier 1A10A2 and remove 1A10A2 from the enclosure.

(5) Loosen, but do not remove, the two screws -on the rear side of enclosure 1A10 securing 2nd frequency multiplier 1A10A1 to the frequency multiplier group 1A10 enclosure and disconnect the mating type TNC connector between 2275-2425 MHz circulator 1A10HY1 and 2nd frequency multiplier 1A10A1. Remove 1A10A1 from the enclosure.

(6) Remove the three screws securing 2275-2425 MHz circulator 1A10HY1 to the frequency multiplier group 1A10 enclosure and then remove 2275-2425 MHz circulator 1A10HY1 from the frequency multiplier group 1A10 enclosure.

b. Replacement.

(1) Insert replacement 2275-2425 MHz circulator 1A10HY1 into frequency multiplier group 1A10 enclosure and secure in place with the three mounting screws removed instep a(6).

(2) Insert 2nd frequency multiplier 1A10A1 into enclosure 1A10 and slide toward 2275-2425 MHz circulator 1A10HY1. Align and connect the mating type TNC connector between 2275-2425 MHz circulator 1A10HY1 and 2nd frequency multiplier 1A10A1.

(3) Insert 3rd frequency multiplier 1A10A2 to enclosure 1A10 and slide toward 2275-2425 MHz circulator 1A10HY1. Align and connect the mating type TNC connector between 2275-2425 MHz circulator 1A10HY1 and 3rd frequency multiplier 1A10A2.

(4) Tighten the four screws on rear side of enclosure 1A10 securing 2d frequency multiplier

1A10A1 and 3rd frequency multiplier 1A10A2 to enclosure 1A10.

(5) Replace frequency multiplier group 1A10 onto plate assembly 1A15 (TM 11-5820-595-12).

NOTE

Check that RF POWER indicator on transmitter meter panel is lighted green after performing step a of paragraph 313.

(6) Energize the radio set (para 3-13). Perform the calibration of transmitter frequency multiplier metering circuits (para 3-40).

3-25. Replacement of 1137-1213 MHz Circulator 1HY1 and 1137-1213 MHz Bandpass Filter 1FL5 (figs. 3-3 and 3-4)

Replacement of 1137-1213 MHz circulator 1HY1 or 1137-1213 MHz bandpass filter 1FL5 requires removal of a mounting bracket to plate assembly 1A15 upon which both modules are mounted.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cable 1A15W8 from 1137-1213 MHz circulator 1HY1 connector DC MONITOR J3 (fig. 3-4).

CAUTION

Care must be taken to prevent damage to the rigid, coaxial cables.

(3) Disconnect rigid coaxial cable 1W9 between 1HY1J2 and 1A10J, and 1W7 between 1FL5J1 and 1A11J7 (para 3-14).

(4) Remove the two screws securing the mounting bracket to plate assembly 1A15 (fig. 3-4) and remove mounting bracket with 1137-1213 MHz circulator 1HY1 and 1137-1213 MHz bandpass filter 1FL5 attached.

(5) Remove from the side and rear of the mounting bracket two screws and four screws securing 1137-1213 MHz bandpass filter 1FL5 to the mounting bracket.

(6) Loosen the mating type TNC connector between 1137-1213 MHz circulator 1HY1 and 1137-121.3 MHz bandpass filter 1FL5 and slide 1FL5 away from 1FL5. Remove 1FL5 from the mounting bracket.

(7) Remove three screws from the side of the mounting bracket releasing 1137-1213 MHz circulator 1HY1 from the mounting bracket.

b. Replacement.

(1) Place replacement 1137-1213 MHz circulator 1HY1 on mounting bracket. Align 1HY1 mounting holes with mounting slots on side of mounting bracket and loosely secure to mounting bracket with the three mounting screws.

(2) Place 1137-1213 MHz bandpass filter 1FL5 on mounting bracket and align mating type TNC connector with INPUT J1 connector on 1137-1213 MHz circulator 1HY1.

(3) Finger tighten the type TNC connector.

(4) Replace the six screws removed in step a(5) to loosely secure 1FL5 to the mounting bracket and then firmly tighten the mating type TNC connector.

(5) Tighten the four screws from rear of mounting bracket securing 1137-1213 MHz bandpass filter 1FL5 to the mounting bracket. Then tighten the five mounting screws on the side of the mounting bracket.

(6) Place the mounting bracket With 1FL5 and 1HY1 on plate assembly 1A15, and then tighten the two screws that secure the mounting bracket to plate assembly 1A15.

(7) Connect rigid coaxial cable 1W9 between 1HY1J2 and 1A10J1, and 1W7 between 1F15J1 and 1A11J7 (para 3-14).

(8) Connect coaxial cable 1A15W8 to 1137-1213 MHz circulator 1HY1 connector DC MONITOR J3 (fig. 3-4).

(9) Energize the radio set (para 3-13). Check that RF POWER indicator on the transmitter meter panel is lighted green after performing step a of paragraph 3-13. Perform the calibration of transmitter frequency multiplier metering circuits (para 3-40).

3-26. Replacement of Digital Data Modem Chassis 1A12A15 (figs. 3-3 and 3-4)

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cables connected to digital data modem 1A12A15J1 through 1A12A15J4 (fig. 3-4).

(3) Loosen the two assembly captive screws securing digital data modem 1A12 to transmitter cabinet 1A16 by alternately tuning each captive screw two turns at a time. Withdraw digital data modem 1A12 from the transmitter cabinet 1A16.

(4) Loosen the three captive screws securing the hinged front cover and lower front cover.

(5) Using a card extractor carefully remove plug-in components 1A12A2 through 1A12A13 from the defective digital data modem chassis 1A12A12 (TM 11-5820-595-12).

(6) Loosen the two captive screws securing each module 1A12A1 and 1A12A14 to digital data modem chassis 1A12A15 and remove the modules from the chassis.

(7) Close the hinged front cover of the defective 1A12A15, tighten the three captive screws securing the front cover and tag the chassis 1A12A15 for higher category maintenance repair.

b. Replacement.

(1) Loosen the three captive screws securing the front cover of the replacement digital data modem chassis 1A12A15 and lower the front cover.

(2) Carefully insert the plug-in components 1A12A1 through 1A12A14 removed in step a(S) and (6) into their respective positions as indicated on the hinged cover of digital data modem chassis 1A12A15.

(3) Tighten the four captive screws securing modules 1A12A1 and 1A12A14 to digital data modem chassis 1A12A15.

(4) Close the hinged front cover and tighten the three captive screws securing the hinged front cover.

(5) Insert replacement digital data modem 1A12 into transmitter cabinet 1A16.

(6) Alternately tighten each assembly captive screw until the digital data modem 1A12 is properly seated and secured in transmitter cabinet 1A16.

(7) Reconnect coaxial cables removed in step a(2).

(8) Energize the radio set (para 3-13). The following indicators on transmitter meter panel will light green: TRAF, RADIO TO CABLE MODEM, CABLE TO RADIO MODEM. All module indicators on digital data modem 1A12 are lighted. Perform the transmitter order-wire level adjustment (TM 11-5820-59512).

3-27. Replacement of Orderwire Chassis 1 A13A7 (figs. -3 and 3-4)

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cable 1A16W6 from connector J8 (fig. 3-4) on frequency synthesizer 1A14.

(3) Loosen the two assembly captive screws securing the orderwire-frequency synthesizer 1A13/1A14 to transmitter cabinet 1A16 by turning each captive screw two turns at a time.

(4) Grasp the two handles on orderwire-frequency synthesizer 1A13/1A14 and carefully remove 1A13/1A14 from transmitter cabinet 1A16.

(5) Alternately loosen the two captive screws securing daughter board assembly 1A13A1 to orderwire chassis 1A13A7.

(6) Using the two captive screws as hand grips slowly extract 1A13A1 from its position in 1A13A7.

(7) Loosen the two captive screws securing the hinged door 1A13A6 to the orderwire chassis 1A13A7 and lower hinged door.

(8) Using a card extractor, remove daughter board assemblies 1A13A2 through 1A13A5 from the defective orderwire chassis 1A13A7.

(9) Remove the 12 screws securing the rear cover to the chassis (fig. 3-16). Carefully place rear cover next to chassis rear to prevent damage to wire leads between plug P1 and the chassis connectors for the plug-in modules.

(10) Remove the socket head cap screw, one of eight (fig. 3-16) which is now accessible from the chassis rear, on the lower left side wall of the chassis.

(11) Using two of the **12** screws removed in step (9), carefully lift rear cover and loosely secure the cover to the chassis.

(12) From the front-of the chassis remove the seven socket head cap screws (4 located along the lower right side wall and 3 along the upper right side wall) that secure orderwire chassis 1A13A7 to frequency synthesizer chassis 1A14A10 (fig. 3-16).

NOTE

Save the eight socket head cap screws for reassembly of replacement order-wire chassis 1A 13A7 with frequency synthesizer 1A14.

(13) Secure the rear cover to the chassis using the remaining 10 screws removed in step 9 and tighten all]2 screws to secure rear cover to chassis.

(14) Close and secure the hinged door of the defective orderwire chassis 1A13A7 and indicate that higher category of maintenance is required.

b. Replacement.

(1) Insert two of the eight socket head cap screws (a (12) above) into the right side wall of

replacement orderwire chassis 1A13A7. Position align and loosely secure replacement orderwire chassis 1A13A7 with frequency synthesizer 1A14 using the two socket head cap screws as guides (fig. '3-16).

(2) Insert five socket head cap screws into the orderwire chassis 1A13A7 right side wall mounting holes and tighten the seven socket head cap screws securing orderwire chassis 1A13A7 to frequency synthesizer 1A14.

(3) Remove the **12** screws securing the rear cover to the orderwire chassis and carefully place rear cover next to chassis.

(4) Insert the last of the eight socket head cap screws into the chassis lower left side wall mounting hole and tighten. Check and tighten all eight socket head cap screws used to secure the orderwire chassis A13A7 to frequency synthesizer 1A14.

(5) Carefully lift, position and secure orderwire chassis rear cover to chassis with the **12** screws removed in step (3).

(6) Insert the combined 1A13A7/1A14 into transmitter cabinet 1A6. Alternately tighten the two captive screws on combined 1A13A7/1A14 (fig 3-4) until firmly seated and secured to transmitter cabinet 1A16.

(7) Insert daughter board 1A13A1 into its proper position in 1A13A7 and alternately tighten the two captive screws securing 1A13A1 to 1A13A7.

(8) Carefully insert daughter board assemblies 1A13A2 through 1A13A5 into position checking that each daughter board assembly is properly seated into the upper and lower guide rails located on orderwire chassis 1A13A7.

(9) Carefully push daughter board assembly 1A13A2 through 1A13A5 into 1A13A7 until each outer edge is aligned uniformly in 1A13A7.

(10) Close and secure hinged door 1A13A6 tightening two captive screws on 1A13A6.

(11) Reconnect coaxial cable 1A16W6 to connector J8 (fig. 3-4) on frequency synthesizer 1A14.

(12) Energize the radio set (para 3-13). Perform the wire module test and transmitter orderwire checks (TM 11-5820-595-12).

3-28. Replacement of Frequency Synthesizer Chassis 1A14A10 (figs. 3-3, 3-4 and 3-16) a. Removal.

(1) Apply steps (1) through (12), paragraph 3-27a.

(2) Alternately loosen captive screws securing plug-in modules 1A14A1 through 1A14A7 to frequency synthesizer 1A14 and remove from frequency synthesizer 1A14.

(3) Loosen the six captive screws securing plug-in module 1A14A8' to rear portion of frequency synthesizer chassis 1A14A10 (fig. 3-16) and remove 1A14A8. Tag chassis 1A14A10 for higher maintenance repair.

NOTE

Save plug-in modules 1A14A1 through 1A14A8 for reassembly into replacement frequency synthesizer chassis.

b. Replacement.

(1) Carefully insert plug-in module 1A14A8 into position on the rear of replacement 1A14A10. Check alignment of guide holes on 1A14A8 with guide pins located on rear portion of frequency synthesizer 1A14 (fig. 3-16).

(2) Carefully push plug-in module 1A14A8 until' it is properly seated with its mating connector on chassis 1A14A10. Secure 1A14A8 in place by tightening the six captive screws loosened in step a(3).

(3) Carefully insert frequency synthesizer plug-in modules 1A14A1 through 1A14A7 into 1A14. Check that the guide pins on the rear of each plug-in module is seated in their respective guide pin holes in frequency synthesizer 1A14.

(4) Push each plug-in module into its mating connector in frequency synthesizer 1A14 and alternately tighten the captive screws on plug-in modules 1A14A1 through 1A14A7.

(5) Apply steps (1) through (12), paragraph 3-27b.

(6) Energize the radio set (para 3-13) and check that: The SYNTH LOCK indicator on the transmitter meter panel is lighted green. The 5V and 28V indicators on frequency synthesizer 1A14 are lighted. The indicator lamps on plug-in modules 1A14A1 through 1A14A6 are not lighted. The indication on meter 1A16M1 is in the yellow band when the meter selector switch on meter panel is set to SYNTHESIZER.

(7) Perform the frequency synthesizer alarm check (TM 11-5820-595-12).

3-29. Removal of Plate Assembly 1A15 (figs. 3-3, 3-4, 3-14, 3-15 and 3-17)

a. Removal.

(1) Remove power supply 1A1 from transmitter cabinet 1A16 by performing step (1) through (5) of paragraph 3-16a.

(2) Disconnect main harness plug 1A15W1P1 from connector 1A16W19J1 (fig. 3-14).

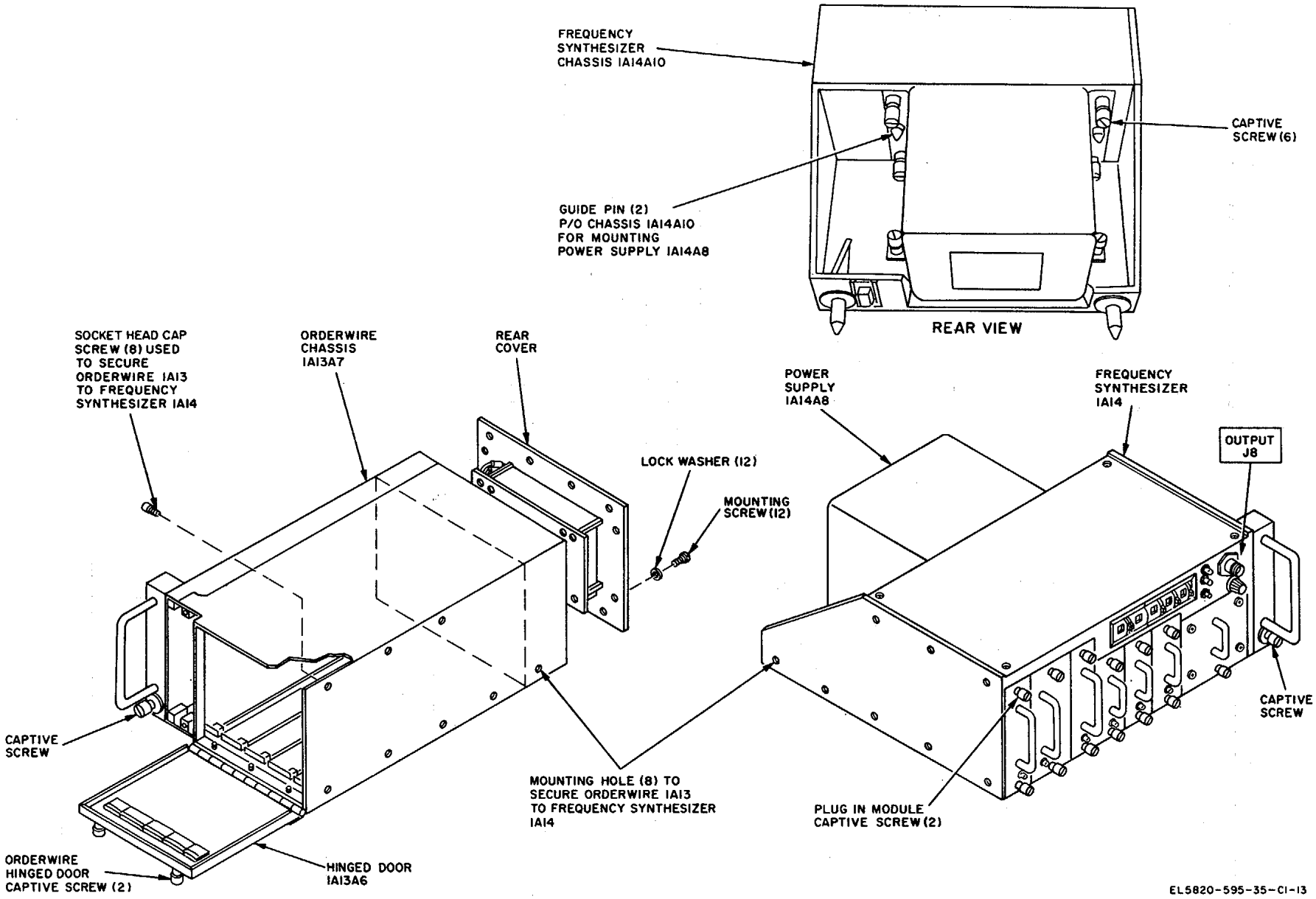


Figure 3-16. Disassembly of composite orderwire frequency synthesizer assembly 1A13/1A14.

CAUTION

The steps referenced for removal of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(3) Disconnect rigid coaxial cable 1W7 between 1HY1J1 and 1A11J7 (para 3-14).

(4) Remove plug-in modules 1A3, 1A5 and 1A11 from transmitter cabinet (TM 11-5820-595-12).

(5) Fasten coaxial cables 1A16W3 and 1A16W6 to sides of transmitter cabinet 1A16 with masking tape to prevent damage to coaxial cables.

(6) Disconnect coaxial cables 1A16W16 and 1A16W17 (fig. 3-4) from connectors 1AT3J2 and 1AT4J2 (fig. 3-17) respectively accessible from rear of radio test set.

(7) Disconnect coaxial cable 1A16W15 (fig. 3-18) from connector 1DC2J2.

(8) remove two left side mounting screws (fig. 3-14) securing left side of radio test set to transmitter cabinet left side wall.

(9) Loosen two captive mounting screws (note 1, fig. 3-4) accessible through holes in front of radio test set meter panel.

(10) Remove the remaining ten mounting screws securing plate assembly 1A15 to transmitter cabinet 1A16.

CAUTION

Exercise care when removing plate assembly 1A15 from transmitter cabinet 1A16 to prevent damage to plug-in modules still mounted on plate assembly and exposed coaxial cables and wiring harnesses. Fasten loose cables and wiring harness in place with masking tape or equivalent.

(11) Remove plate assembly 1A15 from guide pins in transmitter cabinet 1A16 and slowly pull plate assembly out of transmitter cabinet 1A15.

b. Replacement.

(1) Carefully insert and position plate assembly 1A15 against the mounting rails and guide pins in transmitter cabinet 1A16. Position left side of plate assembly checking that guide pin on upper left side is inserted first. If necessary remove modules on left side of plate assembly to allow easier handling of plate assembly before positioning against mounting rails. Ensure that plate assembly is flush against mounting rails and properly seated on the two guide pins. Check that all coaxial cables and wiring harness are correctly positioned before securing plate assembly 1A15 in place.

(2) Tighten the two captivated mounting screws loosened in step a(9) and replace and tighten the ten mounting screws removed in step a(10).

(3) Replace and tighten the two radio test set left side mounting screws removed in step a(8).

(4) Connect the following coaxial cables: 1A16W15 to 1DC2J2; 1A16W16 to 1AT3J2; 1A16W17 to 1AT4J2.

(5) Connect main harness plug 1A15W1P1 to connector 1A16W19J1.

(6) Replace plug-in modules 1A3, 1A5 and 1A11 on plate assembly 1A15 (TM 11-5820-595-12).

CAUTION

The step referenced for replacement of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(7) Connect rigid coaxial cable 1W7 between 1HY1J1 and 1A11J7 (para 3-14).

(8) Replace power supply 1A1 into transmitter cabinet by performing steps (6) through (9) of paragraph 3-16b.

(9) Energize the radio set (para 3-13).

c. Replacement of Parts on or behind Plate Assembly 1A15 (fig. 3-17). Plate assembly 1A15 must be removed from transmitter cabinet 1A16 to gain access to the following parts mounted on 1A15: cable harness 1A14W1; connectors 1A15W1P1, 1A15W1XA2, 1A15W1XA3, 1A15W1XA4, 1A15W1XA5A, 1A15W1XA5B, 1A15W1XA7, 1A15W1XA8, and 1A15W1XA11, terminal board 1A15TB1; 4.4-5.0 GHz bandpass filter 1FL3; 5.0 GHz low pass filter 1FL4; and directional coupler 1DC2. In addition access to the following transmitter cabinet parts (fig. 3-18) requires removal of plate assembly 1A15: power transformer 1A16T1; terminal board 1A16TB2; and cable harnesses 1A16W4 and 1A16W19.

Replacement procedures for specific parts are detailed in paragraphs 3-30, 3-31 and 3-32.

3-30. Replacement of Power Transformer 1A16T1 (fig. 3-18)

a. Removal.

(1) Remove plate assembly 1A15 (para 3-29a).

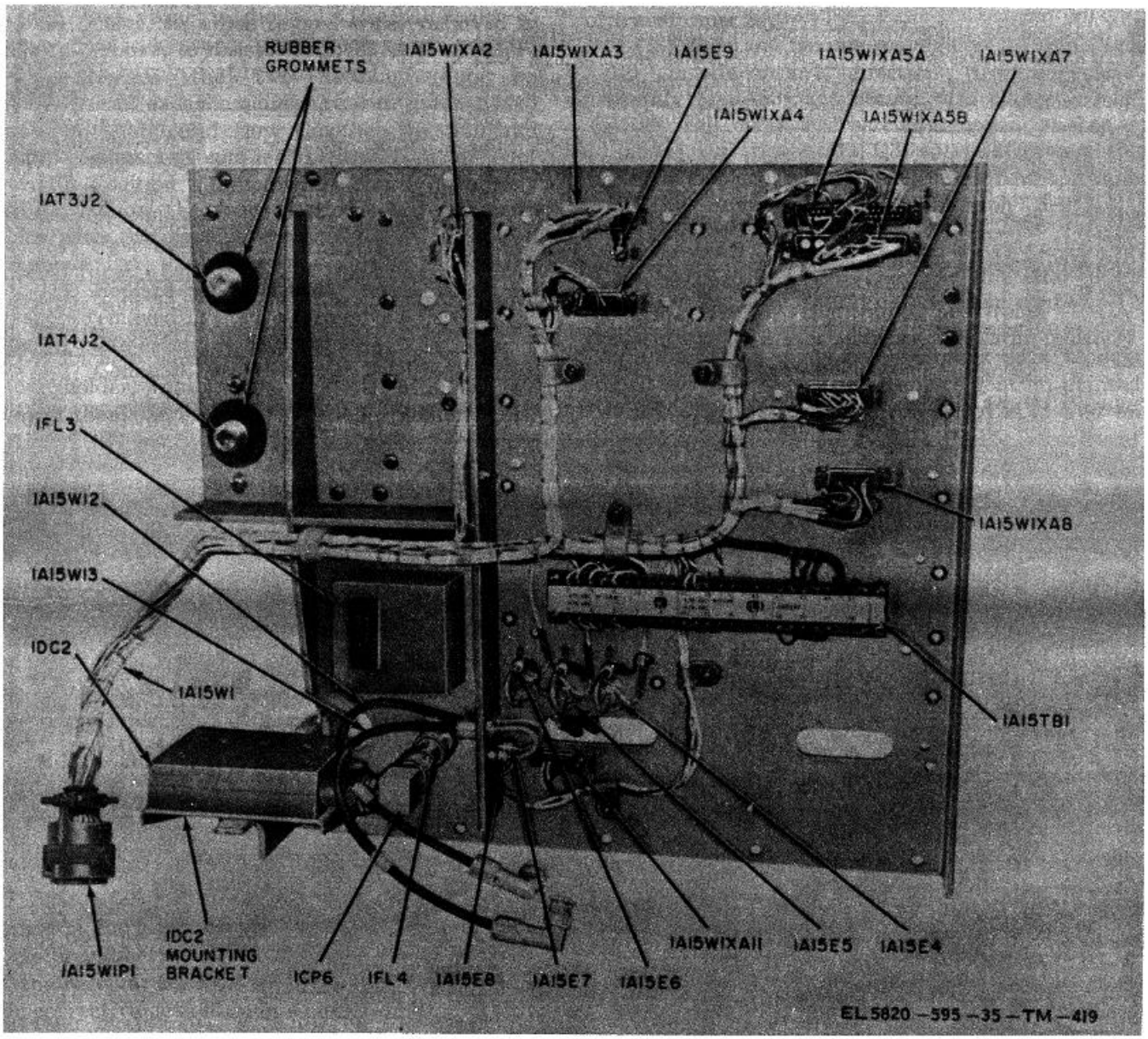


Figure 3-17. Transmitter plate assembly 1A15, rear view, parts location.

(2) Remove three plastic cable clamps (fig. 3-18) securing cable harness 1A16W18 to transmitter cabinet.

(3) Remove the two screws, washers and nuts securing power supply connector 1A16W18XA1A (fig. 3-18) to power supply receptacle bracket.

(4) Remove power supply connector 1A16W18XA1A from bracket to remove any stress to cable harness when removing power transformer 1A16T1.

(5) Tag and unsolder wires connected to terminals on the right side of power transformer 1A16T1. Terminal 6 is the top right front terminal and terminal 8 is the right rear top terminal.

(6) Remove the two screws, washers and nuts securing the right side of power transformer 1A16T1 to mounting bracket.

(7) Remove the left front screw, washer and nut securing power transformer to mounting bracket.

(8) To remove the left rear screw, washer and nut use a box wrench to loosen the nut and then slide power transformer to the right as far as possible. Use an angle mirror to align screwdriver with screw head to loosen and remove screw, washer and nut.

(9) Lift and rotate power transformer 900 exposing the left side terminals.

(10) Tag and unsolder wires connected to the exposed left hand-side terminals. Terminal 20 is the top left front terminal and terminal 15 is the top left rear terminal.

(11) Lift and remove power transformer 1A16T1 from mounting bracket.

b. Replacement.

(1) Place and position (refer to step a(9)) power transformer 1A16T1 to rest on transmitter cabinet 1A16 mounting bracket with left side terminals exposed. Terminal 20 is top left front terminal and terminal 15 is top left rear terminal.

(2) Connect and solder the wires removed in step a(10)to the left side terminals.

(3) Insert the two left side mounting screws removed in step a(7) and (8) into the exposed power transformer mounting holes.

(4) Lift and rotate power transformer 900 aligning and inserting two left side mounting screws into two mounting bracket holes adjacent to transmitter cabinet left side wall.

(5) Insert two right side screws removed in step a(6) through transformer mounting holes and transmitter cabinet mounting bracket.

(6) Replace and partially tighten the four washers and nuts on the four mounting screws.

(7) Tighten the left rear and front mounting hardware using an angle mirror to align screwdriver with screw head.

(8) Tighten the right side mounting hardware.

(9) Connect and solder the wires removed in step a(5) to the exposed terminals with right side. Terminal 6 is the top right front and terminal 8 is the top right rear terminal.

(10) Replace power supply connector (fig. 3-18) on power supply receptacle bracket and secure in place using mounting hardware removed in step a(3).

(11) Replace the three plastic cable stamps and secure cable harness 1A16W8 to transmitter cabinet. Perform the primary power isolation check (para 3-5) before replacing plate assembly 1A15.

(12) Replace plate assembly 1A15 (para 3-29b). Check that all power supply 1A1 indicator lamps are lighted green as noted in paragraph 3-13 a(2).

3-31. Replacement of 4.4-5.0 GHz Bandpass Filter 1FL3, 5.0 GHz Low Pass Filter 1FL4, and Directional Coupler 1DC2 (fig. 3-17)

The following procedures detail the steps necessary to remove all three components. Any single item can be further disassembled when removed from transmitter cabinet 1A16.

a. Removal.

(1) Remove plate assembly 1A15 (para 3-29a).

(2) Disconnect the following coaxial cables: 1A9W3 from 4.4-5.0 GHz bandpass filter 1FL3 connector J1 and 1A15W14 from directional coupler 1DC2 connector RF INCIDENT J3.

(3) Alternately loosen the four screws securing 4.4-5.0 GHz bandpass filter 1FL3 to plate assembly 1A15 and loosen the connector securing 5.0 GHz low pass filter 1FL4 to 4.4-5.0 GHz bandpass filter 1FL3 connector J2. Remove the 4.4-5.0 GHz bandpass filter 1FL3 from plate assembly 1A15.

(4) Loosen the 1CP6 connector securing 5.0 GHz low pass filter 1FL4 to directional coupler 1DC2 connector XMTRJ1, then remove 5.0 GHz low pass filter 1FL4.

(5) Loosen and remove three screws securing directional coupler 1DC2 to the 1DC2 mounting bracket.

b. Replacement.

(1) Place directional coupler 1DC2 against the mounting bracket, aligning the three mounting holes and secure it using the three screws removed in step a(5).

(2) Align 5.0 GHz low pass filter 1FL4 with directional coupler 1DC2 connector XMTRJ1 and connector access hole in plate assembly 1A15. Then tighten and securely mate 5.0 GHz low pass filter 1FL4 connector to directional coupler 1DC2 connector XMTRJ1.

(3) Place 4.4-5.0 GHz bandpass filter 1FL3 against plate assembly 1A15. Align the four mounting holes and mating connector J2 to 5.0 GHz low pass filter 1FL4 connector. Alternately tighten the four mounting screws and tighten the

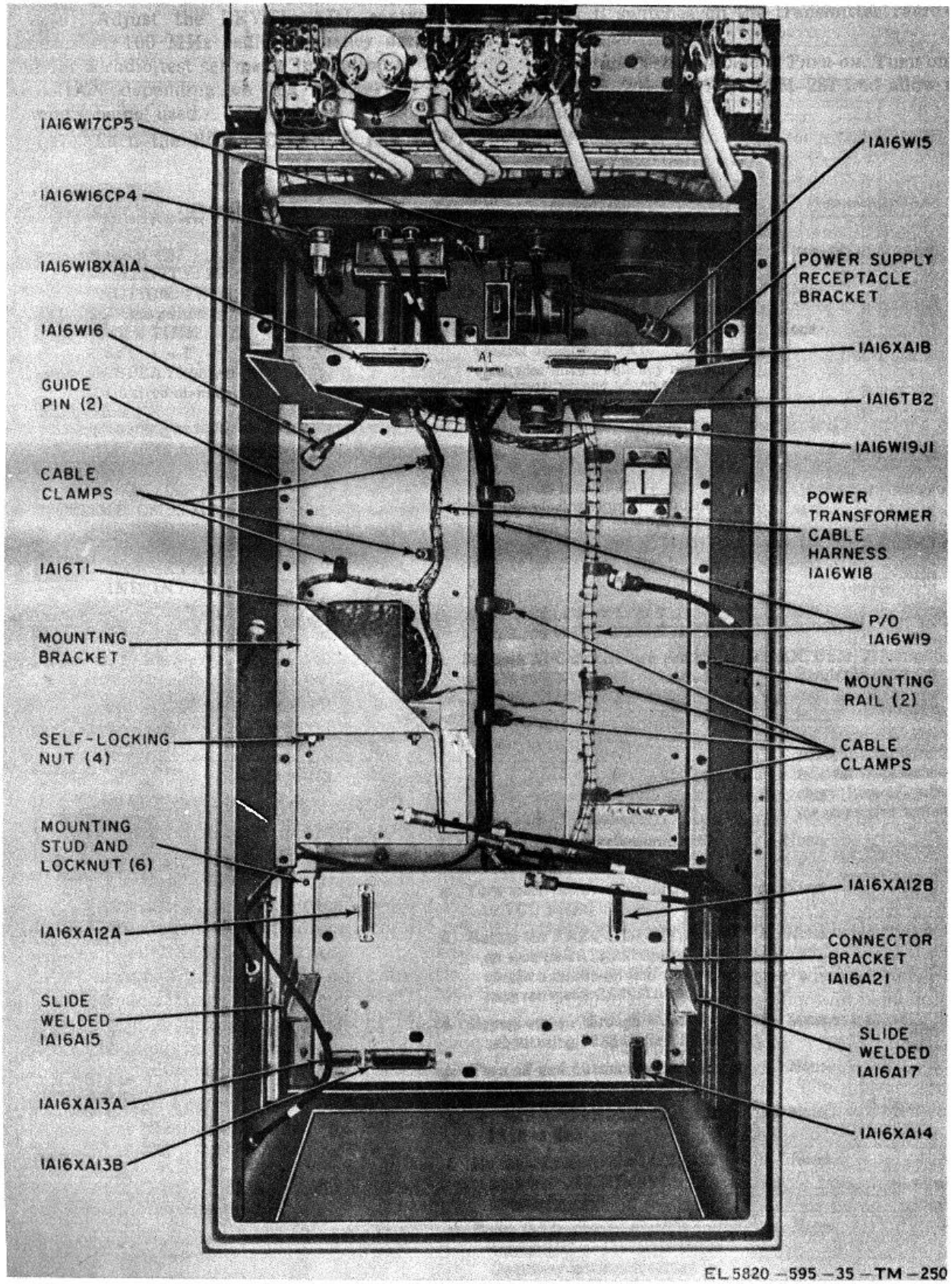


Figure 3-18. Transmitter cabinet 1A16, front view partially disassembled, parts location.

5.0 GHz low pass filter 1FL4 connector until 4.4-5.0 GHz bandpass filter 1FL3 is securely fastened to plate assembly 1A1S and the mating connectors between 1FL3 and 1FL4 are securely fastened.

(4) Connect coaxial cables 1A9W3 to-4.4-5.0 GHz bandpass filter 1FL3 connector J1 and 1A15W14 to directional coupler 1DC2 connector RF INCIDENT J3.

(5) Replace plate assembly 1A1 in transmitter cabinet 1A16 by performing the steps provided in paragraph 3-29b.

(6) If 4.4-5.0 GHz bandpass filter 1FL3 is replaced check that when PUSH TO TURN tuning knob is rotated in a clockwise direction the numbers appear in increasing order until the word STOP appears. A dial indication of 5000 will also be visible. Likewise, when PUSH TO TURN tuning knob is rotated in a counterclockwise direction, the numbers shall appear in decreasing order until the word STOP appears. A dial indication of 4000 will be visible at this time. Set the dial indication to the same frequency setting as frequency synthesizer 1A14. If 5.0 GHz low pass filter 1FL4 or directional coupler 1DC2, or both are replaced perform the transmitter output power and metering test (para 3-9).

3-32. Repair and Replacement of Transmitter Connectors (fig. 8-14)

a. General. Repair of connectors in the transmitter requires either; the replacement of the defective connector (solder type nonremovable contacts), or the replacement of defective connector contacts (crimp type removable contacts). A listing of transmitter connectors is provided in subparagraph b. This chart specifies connector type, the required repair procedure, the applicable tools and figure reference. Procedures for replacing the different type connector contacts are provided in subparagraphs c, d, e, and f. A continuity check should be performed after a connector or connector pin has been replaced. Crimping, extraction, and insertion tools are illustrated in figure 5-3.

b. Transmitter Connectors.

Connector	Extraction, insertion tool	Crimping tool	Procedure paragraph	Figure reference
1A1A13P1	MS 18278 Size 20 None	MS 3191-4 with Head Assy W25	3-32*c*	3-8
1A1A13P2	Same	Same	3-32*c*	3-8
1A151XA2	Same	Same	3-32*c*	3-14
1A15W1XA3	Same	Same	3-32*c*	3-14
1A15W11XA4	Same	Same	3-32*c*	3-14
1A15W11XA5A	Same	Same	3-32*c*	3-14
1A15W1XA	Same	Same	3-32*c*	3-14
1A15W1A8	Same	Same	3-32*c*	3-14
1A15WXA11	Same	Same	3-32*c*	3-14
1A16W18XA1A	Same	Same	3-32*c*	3-18
1A16SXA1B	Same	Same	3-32*c*	3-18
1A16XA12A	Same	Same	3-32*c*	3-18
1A16XA12B	MS 18278 Size 20 None	MS 3191-4 with Head Assy W25	3-32*c*	3-18
1A16XA13B	Same.	Same.	3-32*c*	3-18
1A15W1XA5B	CET-C6B None	None	3-32*d*	3-14
1A16XA13A	CET-C6B None	None	3-32*d*	3-18
1A16XA14	CET-C6B None	None	3-32*d*	3-18
1A15WP1	MS 24256 R20 A20	MS 31914 with Head Assy W1	3-32*e*	3-4
1A16W19J1	MS 2456 R20 A20	MS 31914 with Head Assy W1	3-32*e*	3-4
1A1A13XA1 through 1A1A13XA4	None required	None required	3-17*e*	3-8
1A1A13XA6 through 1A1A13XA12	None required	None required	3-17*e*	3-8
1A16W19J4	None required	None required	3-32*f*	3-12
1A16W19J5	None required	None required	3-32*f*	3-12
1A16W19J7	None required	None required	3-32*f*	3-12

c. Crimp Type Removable Contact Rectangular Connectors. This type of connector incorporates crimp type removable contacts. The procedure for extracting contacts is given in (1) below. Replacement of the contact pin requires stripping of the wire to the proper length, crimping of the new contact to the wire and insertion of the contact into the connector using the contact insertion tool. The procedure for stripping, crimping and inserting contacts is given in (2) below.

(1) Contact extracting.

(a) Place wire to be removed into the tip of extraction tool MS 18278 size 20 (fig. 5-3).

(b) Insert tool tip into contact cavity until tip bottoms against contact shoulder, releasing the retaining clip lines; hold wire against the tool with your finger and withdraw tool and contact from the rear of the connector.

(2) Contact replacement.

(a) Strip wire back 3/16-inch.

(b) Insert contact and wire into locator head of crimping tool MS 3191-4 with head assembly W25 (fig. 5-3). Use pin contacts 330-5291-000 or socket 031-10007-000 (whichever is applicable).

(c) Squeeze tool handles firmly and completely to insure a proper crimp.

NOTE

Tool will not release unless the crimp indentors in the tool head have been fully actuated.

(d) Insert crimp connection, check that crimped area is between the inspection hole and the extreme rear of the crimp barrel. Bare wire strands should be visible through the inspection hole.

(e) Insert contact into the connector.

(f) Reassemble connector hardware.

d. Solder Type With Removable Coaxial Contact Rectangular Connections. This type of connector incorporates captivated solder pot contacts in combination with snap-in coaxial contacts. The two types of coaxial contacts used, straight coaxial shell and right angle coaxial shell are removable. The following procedure describes how to extract and insert the two types of coaxial contacts. Refer to figure 3-19 for identification of the various connector parts and specific coaxial shell mentioned in the steps.

(1) Straight coaxial shell.

(a) Extract the defective coaxial contact from the connector using extraction tool CET-C6B (fig. 5-3).

(b) Unsolder the outer ring from the braid through the cross drilled solder hole and slide outer ring back over the cable jacket.

(c) Unsolder the coaxial center conductor separating the coaxial cable from the coaxial shell.

(d) Insert the cable dielectric and center conductor through the new coaxial contact inner sleeve with the braid on outside of sleeve.

(e) Solder the cable center conductor to the coaxial shell center contact.

(f) Slide outer ring forward until flush with coaxial shell confining the braid between outer ring and inner sleeve.

(g) Soft solder the coaxial shell outer ring to the braid through the cross drilled soler hole.

(h) Reconnect replaced straight coaxial shell contact to connector.

(2) Right angle coaxial shell.

(a) Extract the defective coaxial contact from the connector using extraction tool CET-C6B (fig. 5-3).

(b) Unsolder the outer ring from the braid through the cross drilled solder hole and slide outer ring back over the cable jacket.

(c) Unsolder and remove the access cap, and unsolder the coaxial center conductor; separate the coaxial cable from the coaxial shell.

(d) Insert the cable dielectric and center conductor through the new coaxial contact inner sleeve with the braid on the outside of sleeve.

(e) Soft solder the cable center conductor to the coaxial shell center contact.

(f) Slide outer ring forward until flush with coaxial shell confining the braid between outer ring and inner sleeve.

(g) Soft solder the outer ring to the braid through the cross drilled solder hole.

(h) Soft solder (or stake) the cap in place on the connector.

(i) Reconnect replaced right angle coaxial shell contact to connector.

e. Crimp Type Removable Contact Round Connectors. The military specification (MS) connectors use MIL-C-26482 type hardware. These connectors incorporate crimp style removable contacts. The pin contacts adhere to military standard MS 3192 (A20A); the socket contacts adhere to military standard MS 3193 (A20A), The following procedure describes how to extract, crimp and insert contacts in the MS type connectors.

(1) Contact extraction. Hold connector securely, pull plunger of extraction tool MS 24256R20 (fig. 5-3) back and center tool tube over contact from the front of the insulator. Using moderate pressure, insert tube into contact cavity. Steadily press plunger handle with palm of hand until the contact is released; then, pull contact free from rear of connector.

CAUTION

Do not rotate or twist the extraction tool in the connector.

(2) Contact replacement.

(a) Strip wire back 3/'16-inch.

(b) Insert stripped wire into contact crimp pot, wire must be visible thru inspection hole.

(c) Cycle the crimping tool once to be sure the indentors are open. Insert the contact and wire into the locator. Squeeze tool handles firmly and completely to insure a proper crimp.

NOTE

Tool will not release unless the crimp indentors in the tool head have been fully actuated.

(d) Release crimped contact and wire from tool. Inspect the crimped contact; be certain that the wire is visible through the contact inspection hole.

(e) Insert the wired contact into the rear of connector insulator. Holding the connector securely, position insertion tool MS 24256A20 (fig. 5-3) behind the contact. Butt shoulder in tool against the back of contact in barrel. Push tool straight into contact cavity until contact snaps into position. Assure that contact is locked by pulling lightly on the wire.

(f) Reassemble connector hardware.

f. Solder Type Non-removable Contact Rectangular or Round Connectors. These connectors must be replaced when any of the connector contacts or pins, or the connector is defective or damaged. Replacement of the connector is accomplished by transferring each lead from the defective connector to the identical terminal contact on the replacement connector. The general information provided in the parts replacement techniques, paragraph 3-11, should be reviewed before replacing this type of connector. Care should be exercised when unsoldering individual wire leads from the connector terminals to prevent scorching or burning through the insulation of adjacent wire leads. Do not over heat the connector terminal and wire lead which would cause solder to flow upward along the individual strands of wire resulting in a stiff and brittle lead that could easily break or snap when used with the replacement connector.

3-33. Removal and Replacement of Connector Bracket 1A16A21

(fig. 3-18)

Connector bracket 1A16A21 must be removed from transmitter cabinet 1A16 to provide access to the following connectors; 1A16XA12A, 1A12XA12B, 1A12XA13A, 1A12XA13B and 1A12XA14.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Remove plate assembly 1A15 from transmitter cabinet 1A16 (para 3-29a).

(3) Remove digital data modem 1A12 from transmitter cabinet 1A16 by performing steps (2) and (3) of paragraph 3-26a.

(4) Remove orderwire /frequency synthesizer (1A13 1A14) from transmitter cabinet by performing steps (2), (3) and (4) of paragraph 3-27a.

(5) Loosen and remove two hex head screws and two machine screws securing right slide welded 1A16A17 (fig. 3-18) to right side wall of transmitter cabinet 1A16. Remove right slide welded 1A16A17 and mounting hardware from transmitter cabinet 1A16 and save for reassembly.

(6) Loosen and remove four cable clamps (fig. 3-18) securing cable harness 1A1CW19.

(7) Loosen and remove six self locking nuts securing connector bracket 1A16A21 to lower rear wall of transmitter cabinet 1A16.

CAUTION

When moving connector bracket in any direction, exercise care to prevent stressing cable and wire harness leads to connectors mounted on 1A16A21.

(8) Slide connector bracket 1A16A21 away from the six studs on rear transmitter cabinet wall. Swing right side of connector bracket forward to clear right side plate assembly mounting rail.

(9) Lift and tilt upper edge of connector bracket 1A16A21 forward to provide access to rear of mounted connectors.

(10) When a connector contact must be replaced, refer to paragraph 3-32" to identify procedure to be used. Remove and replace specific connector contacts and proceed to subparagraph

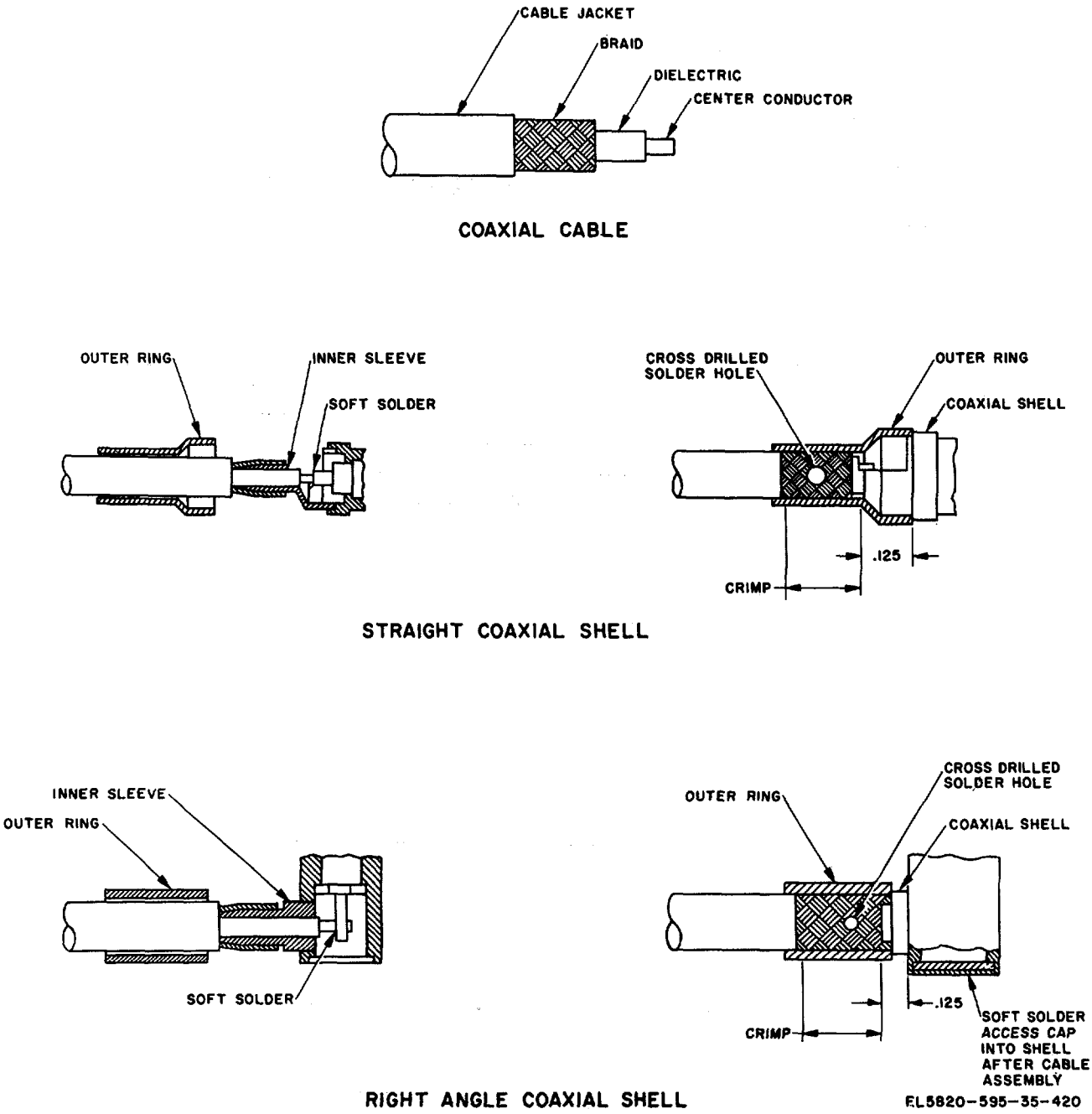


Figure 3-19. Repair of coaxial contacts on multiple pin connectors.

(b) If a connector required replacement continue with the following steps.

(11) Loosen, remove and save the mounting hardware of the connector to be replaced.

(12) Remove cable clamp(s) closest to connector to be replaced from rear of connector bracket 1A16A21.

(13) Remove connector from connector bracket 1A16A21 and mount new connector in its place.

(14) Transfer wired connector contacts from removed connector to its identical terminal position on the new connector (para 3-32). Repeat for the remaining connector contacts.

(15) Secure cable harness in place with cable clamps removed in step (12).

b. Replacement.

(1) Position connector bracket 1A16A21 against transmitter cabinet rear wall by lowering,

tilting and mounting connector bracket on transmitter cabinet six studs.

(2) Partially secure connector bracket, 1A16A21 to transmitter cabinet rear wall using hardware removed in step a *(7)*.

(3) Remount the four cable clamps removed in step a*(6)* securing the two cable harnesses to transmitter cabinet rear wall.

(4) Mount right slide welded 1A16A17 to transmitter cabinet right side wall and secure in place using hardware removed in step a*(5)*.

(5) Insert digital data modem 1A12 into transmitter cabinet 1A16 and alternately tighten each captive screw until digital data modem is properly seated against connector bracket 1A16A21.

(6) Tighten the lower four self-locking nuts securing connector bracket 1A16A21 firmly against transmitter cabinet rear wall.

(7) Remove digital data modem 1A12 from transmitter cabinet by alternately loosening each assembly captive screw.

(8) Tighten all self-locking nuts securing connector bracket 1A16A21 firmly against transmitter cabinet rear wall.

NOTE

Perform a continuity check for each connector contact of the new connector and the other connectors on connector bracket 1A16A21. Refer to fig. 8-14 for wire routing.

(9) Insert order wire/frequency synthesizer (1A13 1A14) in transmitter cabinet 1A16. Alternately tighten the two assembly captive screws until 1A13/1A14 is firmly seated and secured to transmitter cabinet 1A16.

(10) Connect coaxial cable 1A16W6 to OUTPUT connector 1A14J8 on frequency synthesizer 1A14.

(11) Insert digital data modem 1A12 into transmitter cabinet 1A16. Alternately tighten each assembly captive screw until digital data modem is properly seated and secured in transmitter cabinet 1A16.

(12) Replace plate assembly 1A15 in transmitter cabinet 1A16 by performing steps *(1)* through *(9)* of paragraph 3-29b.

(13) Reconnect coaxial cables 1A16W1, 1A16W2, 1A16W3 and 1A16W4 to digital data modem connectors 1A12A15J1, 1A12A15J4, ,1A12A15J2, and 1A12A15J3 respectively.

(14) Energize the radio set (para 3-13). Perform the checks provided at the end of paragraphs 3-26b, 3-27b, and 3-28b to confirm radio set operational status.

Section III. TRANSMITTER CALIBRATION AND ADJUSTMENT

3-34. General

a. This section contains procedures for calibrating the transmitter meters, the transmitter metering circuits, and adjusting the transmitter modulator frequency. The calibration procedures (para 3-35 through 3-41) are performed at periodic maintenance intervals (para 2-4) to maintain the calibration accuracy of the transmitter metering circuits, or when transmitter tests (para 3-9 and 3-8) or troubleshooting (para 3-3d) indicates that calibration is required. The adjustment procedure (para 3-42) is performed when the transmitter frequency accuracy test (para 3-8) or troubleshooting chart (para 3-3d) indicates that a transmitter modulator frequency adjustment is required.

b. All of the procedures contained in this section assume that the radio set is turned on and connected for normal operation at the start of each procedure. Prior to performing any of the procedures, the maintenance man should notify the Multiplexer TD-204/U operator and distant radio set operator that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

c. If trouble is encountered during performance of a procedure, or if the indications specified in the procedure are not obtained, refer to the transmitter troubleshooting chart (para 3-3d) for corrective action.

3-35. Calibration of Transmitter Meter 1A16M1

a. Turn the TS-656/U on and allow a 5-minute warmup period.

b. Set POWER ON/OFF switch 1A16S3 (fig. 3-20) to OFF.

c. Turn meter selector switch 1A16S4 to OFF (TRANSIT).

d. Adjust the meter zero screw on front of meter 1A16M1 for a zero meter indication.

e. Turn meter selector switch 1A16S4 to TEST LEAD (+).

f. On the TS. 656/U, set FUNCTION switch to DIR CUR, set CURRENT switch to 100 MICROAMP, and rotate DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS-656 U between the DIR CUR terminal on TS-656 U and the TEST LEAD jack (fig. 3-20) on top of the transmitter.

h. Connect the black test lead supplied with TS-656 U between the COMMON terminal on terminal on TS-656 U and the E2 CAB GRD lug (fig. 3-20) on top of the transmitter.

i. Hold the TEST switch on TS-656/U in the raised (TEST} position while performing steps *j* and *k* below.

j. Rotate the DECREASE INCREASE control on TS-656 U clockwise until meter 1A16A1 indicates 150.

k. Record meter indication on TS-656/U and then release the TEST switch.

I. Turn the TS-656/U off and disconnect the test leads.

m. Meter indication recorded in step k should be 37.56 1.5 microamperes. If it is not, replace meter 1A16M1 (para 3-15).

n. Set POWER ON/OFF switch 1A16SS (fig. 3-20) to ON.

3-36. Calibration of Transmitter Radio Test Set Meter 1A15M2

a. Turn the TS-656/U on and allow a 5-minute warmup period.

b. Set POWER ON/OFF switch 1A1683 (fig. 3-20) to OFF.

c. Turn meter switch 1A15S6 (fig. 3-0) to OFF (TRANSIT).

d. Adjust the meter zero screw on front of meter 1A15M2 (fig. 3-20) until meter pointer rests over the thin black line located to the left of the yellow band.

e. Remove 100-MHz OSC 1A2.

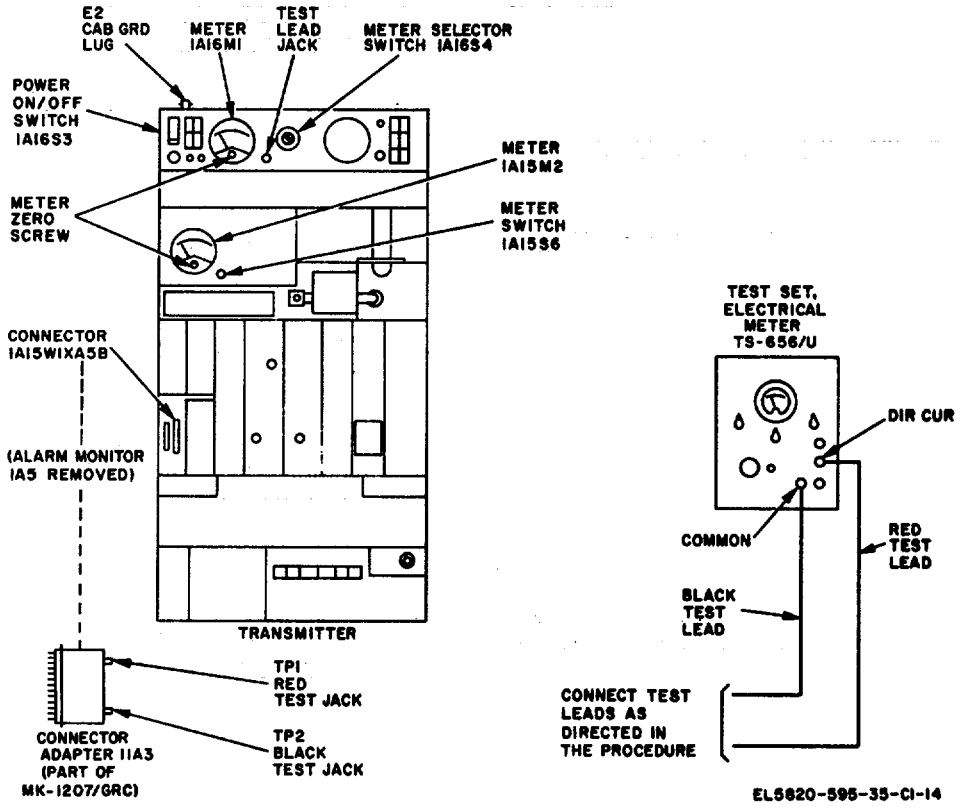


Figure 3-20. Transmitter meter 1A16M1 and 1A16M2, calibration test set up.

f. Set meter switch 1A15S6 to OSC LEVEL.

g. On the TS-656/U, set FUNCTION switch to DIR CUR, set CURRENT switch to 100 MICROAMP, and rotate the DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

h. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the + (positive) terminal meter 1A15M2.

i. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and pin 9 of 1A15W1XA2.

j. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing steps *k* and l below.

k. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter on TS-656/U indicates 40 microamperes.

l. Record indication on meter 1A15M2 and then release the TEST switch.

m. Turn the TS-656/U off and disconnect the test leads.

n. Replace 100-MHz OSC 1A2.

o. Meter indication recorded in step *l* should be in the 24 CHAN black range. If it is not, replace meter 1A15M2 (para 3-22) and repeat the calibration procedure.

p. Set POWER ON/OFF switch 1A16S3 (fig. 3-20) to ON.

3-37. Calibration of Transmitter Traffic Metering Circuit

a. Turn the TS-656/U on and allow a 5-minute warmup period.

b. Set POWER ON/OFF switch 1A16S3 (fig. 3-20) to OFF.

c. Remove alarm monitor 1A5 (TM 11-5820-595-12) from plate assembly 1A15.

d. Connect the connector adapter 11A3 (part of MK-1207/GRC) to connector 11A15-W1XA5B (fig. 3-20).

e. Turn meter selector switch 1A16S4 (fig. 3-20) to TRAFFIC.

f. On the TS-656/U, set FUNCTION switch to DIR CUR, set CURRENT switch to 100 MICROAMP, and rotate DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the red test jack TP1 on the connector adapter 11A3.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the black test jack TP2 on the connector adapter 11A3.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing steps *j* and *k* below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter on TS-656/U indicates 50 microamperes.

k. Indication on meter 1A16M1 should be 90. If it is not, perform the adjustment given in step *l* below. Otherwise, release the TEST switch on TS-656/U and proceed to step m below.

l. Remove the protective plate over the potentiometer bracket, unlock potentiometer 1A16R7 (fig. 3-5). With the TEST switch on TS-656/U in the TEST position, adjust 1A16R7 for a 1A16M1 meter indication of 90. If a meter indication of 90 cannot be obtained, refer to the transmitter troubleshooting chart (para 3-3d) for corrective action upon completion of this procedure.

m. Turn the TS-656/U off and disconnect the test leads.

n. Remove the connector adapter 11A3 from connector 1A15W1XA5B (fig. 3-20) and reinstall alarm monitor 1A5 on plate assembly 1A15.

o. Set transmitter POWER ON/OFF switch 1A16S3 (fig. 3-20) to ON.

3-38. Calibration of Transmitter RF Power Metering Circuit

a. Turn the AN/USM-161 on and allow a 30-minute warmup period.

NOTE

Steps *b* through *f* below can be performed during the warmup period.

b. Record the transmitter operating frequency.

and then set the controls on frequency synthesizer 1A14 to 4800.0 MHz.

c. Observe that RF POWER alarm indicator on the transmitter meter panel is lighted red. If it is not, adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter 1FL3 until it lights red.

d. Disconnect the coaxial cable connected to the J8 RF OUTPUT connector (fig. 3-21) on top of the transmitter cabinet.

e. Connect the test equipment as shown in figure 3-21, but do not connect the test equipment to the J8 RF OUTPUT connector on top of the transmitter cabinet.

f. Calculate the calibration plate correction factors for the CN-845/USM-161 and CG-2514/U for a 4800 MHz input. Algebraically add the correction factors noting the plus or minus sign. *Record.*

g. Calibrate the AN/USM-161 using the procedure given in TM 11-6625-498-12.

h. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 10 MW +10 DBM, set the COMP ATTENUATOR dial to the value recorded in step f above, and set the POWER indicator dial for a dial scale indication of .75 on the outermost scale.

i. Connect the test equipment to the J8 RF OUTPUT connector (fig. 3-21) on top of the transmitter cabinet.

j. Adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter 1FL3 until a null is obtained on the AN/USM-161-NULL INDICATOR meter.

k. Turn meter selector switch 1A16S4 (fig. 3-21) to RF POWER.

l. Indication on meter 1A16M1 should be 30. If it is not, perform the adjustment given in step *m* below. Otherwise, proceed to step *n* below.

m. Remove the protective plate over the potentiometer bracket, unlock potentiometer 1A16R6 (fig. 3-5) and adjust it for a 1A16M1 meter indication of 30. If a meter indication of 30 cannot be obtained, refer to the transmitter troubleshooting chart (para 3-3d) for corrective action upon completion of this procedure.

n. Turn the AN/USM-161 off and disconnect the test equipment.

o. Connect the coaxial cable removed in step *d.*

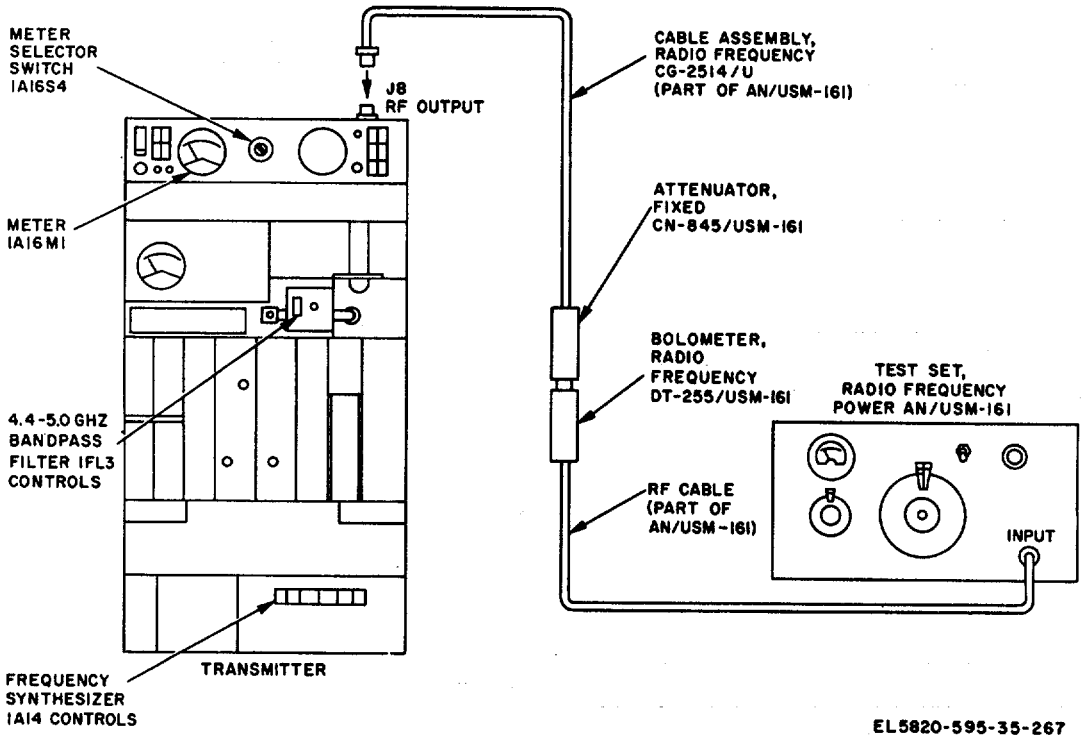


Figure 3-21. Transmitter RF power metering circuit, test set up.

to the J8 RF OUTPUT connector on top of the transmitter cabinet.

p. Set the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to the original operating frequency recorded in step *b* above.

3-39. Calibration of Transmitter Reflected RF Power Metering Circuit

(fig. 3-2)

a. Turn the AN/USM-161 on and allow a 30-minute warmup period.

b. Record the transmitter operating frequency and then set the controls on frequency synthesizer 1A14 to 4800.0 MHz.

c. Observe that RF POWER alarm indicator on the transmitter meter panel is lighted red. If it is not, adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter 1FL3 until it lights red.

d. Disconnect the coaxial cable connected to the J8 RF OUTPUT connector on top of the transmitter.

e. Connect the test equipment as shown in figure 3-2, but do not connect the test equipment to the J8 RF OUTPUT connector on top of the transmitter.

f. Calculate the calibration plate correction factors for the two CN-845/USM-161's and the CG-2514/U for a 4800 MHz input. Algebraically add the correction factors noting the plus or minus sign. *Record.*

g. Calibrate the AN/USM-161 using the procedure given in TM 11-6625-498-12.

h. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DBM, set the COMP ATTENUATOR dial to the value recorded in step *f* above, and set the POWER indicator dial for a dial scale indication of 1.5 on the center scale.

i. Connect the test equipment to the J8 RF OUTPUT connector (fig. 3-2) on top of the transmitter.

j. Adjust the PUSH TO TURN knob on 4.4-5.0 GHz bandpass filter 1FL3 until a null is obtained on the AN /USM-161 NULL INDICATOR meter.

k. Disconnect the test equipment from the J8 RF OUTPUT connector on top of the transmitter.

I. . Connect the coax attenuator 11AT2 and Type N short termination 11AT1 (fig. 3-2) to The J8 RF OUTPUT connector on top of the transmitter.

m. Turn meter selector switch 1A16S4 (fig. 3-2) to REFL RF POWER.

n. Indication on meter 1A16M1 should be 20. If it is not, perform the adjustment given in *o* below. Otherwise, proceed to step *p* below.

o. Remove the protective plate over the potentiometer bracket, unlock potentiometer 1A16R5 (fig. 3-5) and adjust it for a 1A16M1 meter indication of 20. If a meter indication of 20 cannot be obtained, refer to the transmitter troubleshooting chart (para 3-3d) for corrective action upon completion of this procedure.

p. Turn the AN/USM-161 off and disconnect the test equipment.

q. Remove the attenuator and termination connected in step l above and connect the coaxial cable removed in step d to the J8 RF OUTPUT connector on top of the transmitter.

r. Set the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to the original operating frequency recorded in step *b* above.

3-40. Calibration of Transmitter Frequency Multiplier Metering Circuits

NOTE

Do not calibrate any of the transmitter frequency multiplier metering circuits when the transmitter's output power is less than 150 milliwatts. If transmitter output power level is not known, use the transmitter output power and metering test (para 3-9) to determine the transmitter's output power.

To calibrate any of the transmitter frequency multiplier metering circuits, turn meter selector switch 1A16S4 (fig. 3-2) to the circuit to be calibrated and observe the indication on meter 1A16M1. No test equipment is required. If meter indication is not 100, remove the protective plate over the potentiometer bracket, unlock the potentiometer listed below and adjust it for a 1A16M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the transmitter troubleshooting chart (para 3-3d) for corrective action.

Meter selector switch 1A16S4 position	*Potentiorneter adjusted*
AMPL-MULT	A16R4
2ND MULT	1A16R3
3RD MULT (LOCAL OSC)	1A16R2

3-41. Calibration of Transmitter Radio Test Set

a. Turn the AN/USM-161 and AN/URM-52B on and allow a 30-minute warmup period.

b. Record the transmitter and receiver operating frequencies.

c. On the transmitter, set the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to 4800 MHz.

d. On the transmitter, disconnect coaxial cable 1A16W3 (fig. 3-4) from the J1 connector on attenuator assembly 1A3, and observe whether a 12 or 24 channel attenuator assembly is being used. *Record.*

e. On the receiver set the controls on frequency synthesizer 2A21, preselector 2FL4, and 2FL5, post selectors 2FL6- and 2FL7, local oscillator filters 2FL8 and 2FL9 to 4700 MHz.

f. On the receiver, set both SQUELCH ON/OFF switches on combiner 2A16 to OFF, set the AGC SEL switches on IF amplifier 2A12 and 2A15 to TEST, and set the meter selector switch on receiver meter panel to CARRIER (IF) COMBINED.

g. Remove the dust cover from the ATTEN ADJ control on directional couplers 4A5 and 4A6. Using a screwdriver, turn the ATTEN ADJ control on directional couplers 4A5 and 4A6 clockwise until the mechanical stop is engaged.

h. Calibrate the AN/USM-161 using the procedures given in TM 11-6625-498-12 and calibrate the AN/URM-52B at 4700 MHz using the procedures given in TM 11-6625-214-10.

i. Connect the equipment as shown in fig. 3-22.

j. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 1.0 MW 0 DBM, set the COMP ATTENUATOR dial to 0, and set the POWER indicator dial for a dial scale indication of 1.0 on the center scale.

k. Adjust the OUTPUT ATTEN control on AN/URM-52B until a null is obtained on the AN/USM-161 NULL INDICATOR meter.

l. Adjust the POWER SET control on AN/URM-52B for an index indication of 0 dBm on the OUTPUT ATTEN dial.

m. Turn the AN/USM-161 off and disconnect CG-92D/U from type N, female to female adapter (fig. 3-22).

n. Set the OUTPUT ATTEN control on AN/URM-52B for a dial scale indication of -80 dBm if 12 channel operation is being used (step *d* above), or -77 dBm if 24 channel operation is being used.

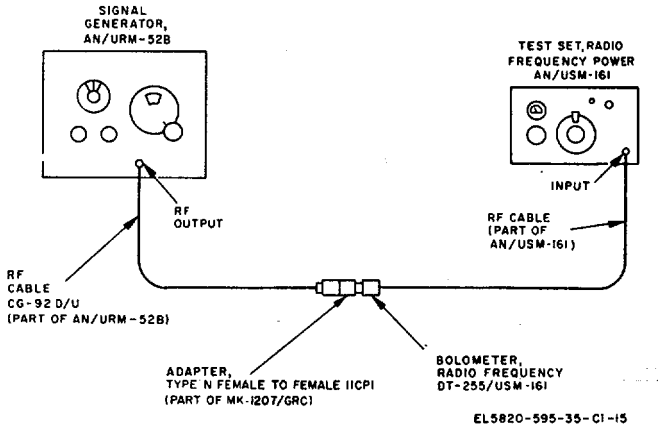


Figure 3-22. Signal Generator AN/URM-152B, calibration test set up.

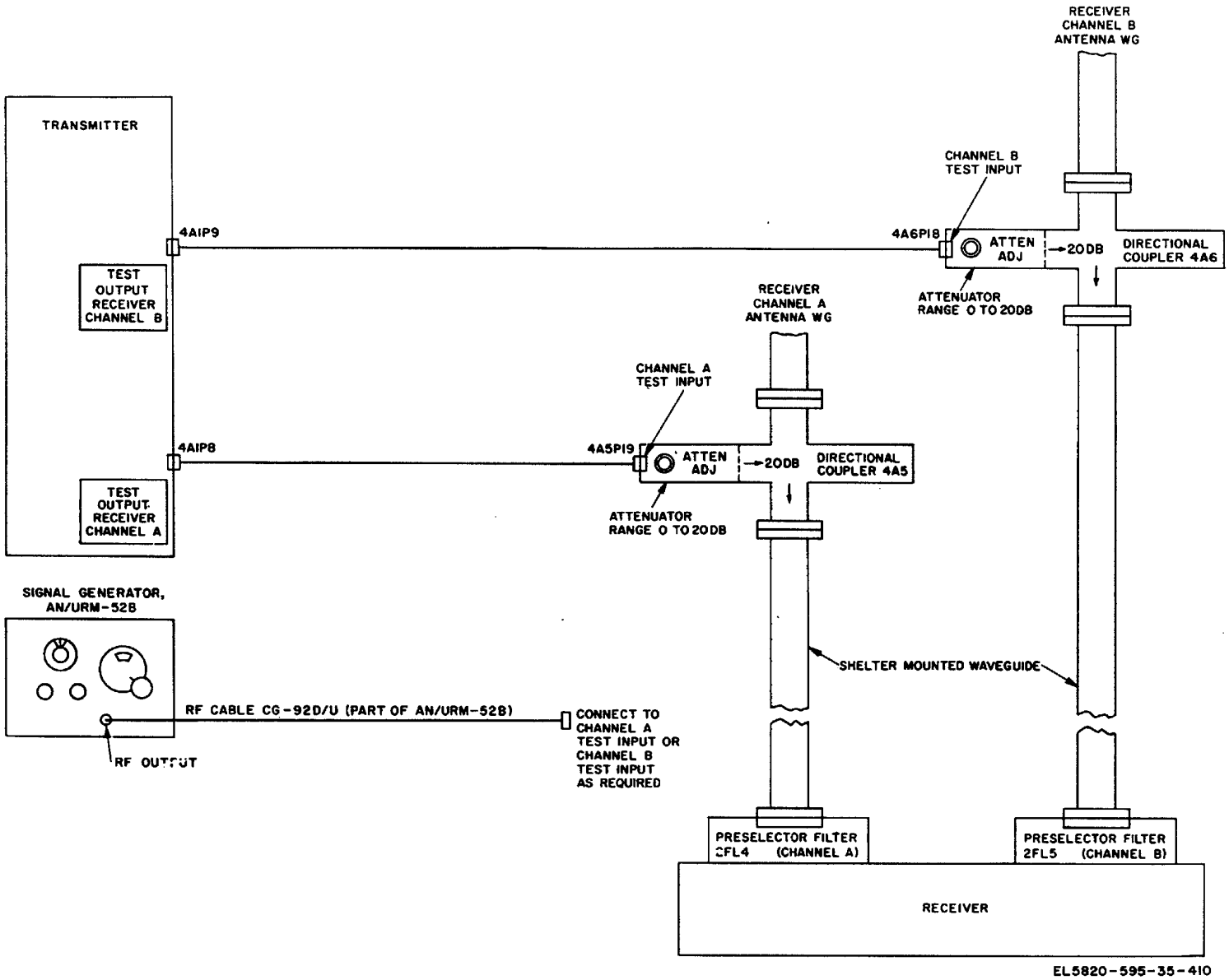


Figure 3-23. Transmitter radio test set, calibration test set up.

o. Disconnect coaxial connectors 4A5P19 and 4A6P18 (fig. 3-23) from directional couplers 4A5 and 4A6.

p. On the receiver, disconnect coaxial cable 2A15W1 from the J2 connector on 70 MHz IF filter 2A10 (fig. 4-12).

q. Connect the free end of CG-92D/U to the channel A test input (fig. 3-23).

r. Fine tune the SIGNAL FREQUENCY control on AN/URM-2B for a peak indication on receiver meter 2A22M1.

s. On the receiver, remove the green cap from the IF GAIN control of IF amplifier 2A12 and use the tuning tool to adjust the control for a receiver meter indication of 100. Replace green cap.

t. On the receiver, disconnect coaxial cable 2A12W1 (fig. 4-12) from the J2 connector on 70 MHz IF filter 2A5 and connect coaxial cable 2A15W1 to the J2 connector on 70 MHz IF filter 2A10.

u. Disconnect CG-92D/U from the channel A test input (fig. 3-23) and connect it to the channel B test input.

v. Repeat steps r and s above, except adjust IF GAIN control on IF amplifier 2A15 for a receiver meter indication of 100.

w. Disconnect CG-92D/U from the channel B test input (fig. 3-23) and turn the AN/URM-2B off.

x. Using a screwdriver, turn the ATTEN ADJ control on directional couplers 4A5 and 4A6 counterclockwise until mechanical stop is engaged.

y. Connect coaxial connector 4A5P19 and 4A6P18 (fig. 3-23) to directional couplers 4A5 and 4A6, respectively.

z. On the transmitter, set the RCVR CHAN A and RCVR CHAN B switches on the radio test set to T.

aa. On the transmitter, set the ON/OFF switch on 100 MHz rf oscillator 1A2 to ON.

ab. On the transmitter, turn the meter switch on the radio test set meter panel to OSC LEVEL and adjust the LEVEL AJD control on 100 MHz rf oscillator 1A2 for a 12 CHAN or 24 CHAN radio test set meter indication depending on the number of channels being used (step d above).

ac. Using a screwdriver, turn the ATTEN ADJ control on directional coupler 4A6 in a clockwise direction until receiver meter 2A22M1 indicates 100.

ad. On the receiver, disconnect coaxial cable 2A15W1 (fig. 4-12) from the J2 connector on 70 MHz IF filter 2A10 and connect coaxial cable 2A12W1 to the J2 connector on 70 MHz IF filter 2A5.

ae. Using a screwdriver, turn the ATTEN ADJ control on directional coupler 4A5 in a clockwise direction until receiver meter 2A22M1 indicates 100.

af. Replace the dust covers removed in step *g* above.

ag. On the receiver, connect coaxial cable 2A15W1 (fig. 4-12) to the J2 connector on 70 MHz IF filter 2A10, set both SQUELCH ON/OFF switches on combiner 2A16 to ON, turn the AGC SEL switches on IF amplifiers 2A12 and 2A15 to DIV ON, and reset the receiver controls (*e* above) to the original operating frequency recorded in step *b* above.

ah. On the transmitter, connect coaxial cable 1A16W3 (fig. 3-4) to the J1 connector on attenuator assembly 1A3, set the ON/OFF switch on 100 MHz rf oscillator 1A2 to OFF, and reset the transmitter controls (*c* above) to the original operating frequency recorded in step b above.

3-42. Transmitter Modulator 1A8 Frequency Adjustment

a. Turn the AN/USM-207 on and allow a 15-minute warmup period.

b. Set the controls on AN/USM-207 as follows:

(1) SENSITIVITY switch to PLUG-IN.

(2) FUNCTION switch to FREQ.

(3) rime base switch to GATE TIME-(SEC-^{1})-10^{3}

(4) Converter attenuator switches (upper and lower) to 10V MAX.

(5) DIRECT-HETERODYNE switch to HETERODYNE.

(6) Mixing frequency selector switch to 100.

(7) DISPLAY control to the desired display time.

c. Disconnect coaxial cable 1A6W2 view B, figure 3-1 from the J1 connector on modulator 1A8.

d. Disconnect coaxial cable 1A8W1 view B, figure 3-1 from the A1J1 connector on frequency mixer 1A9m

e. Connect the equipment as shown in view B, figure 3-1. Note that adapter UG-274B/U is also connected to 1A9A1J1.

f. Observe the LEVEL METER on AN/USM-207. If it indicates in the green zone, proceed to step h below. Otherwise, perform step *g* below.

g. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.

h. On the front of modulator 1A8, remove the blue caps on switch S1 and capacitor C15.

i. Press switch S1 and hold it depressed. Using the tuning tool, adjust capacitor C15 (clockwise to reduce frequency; counterclockwise to increase frequency) until the digital display on AN/USM-207 indicates 50 MHz +20 kHz. If repeated adjustment attempts fail to bring the frequency within the specified tolerance refer to the transmitter troubleshooting chart (para 3-3d) for corrective action upon completion of this procedure.

j. Replace the blue caps removed in step *h.*

k. Turn the AN/USM-207 off and disconnect the test equipment.

l. Connect coaxial cable 1A6W2 to the J1 connector on modulator 1A8.

m. Connect coaxial cable 1A8W1 to the A1J1 connector on frequency mixer 1A9.

CHAPTER 4
RECEIVER DIRECT SUPPORT MAINTENANCE

Section I. RECEIVER TROUBLESHOOTING

WARNING

115 vac is present in the receiver. Do not remove or replace parts or perform continuity or resistance checks while primary power is applied to the equipment.

4-1. Scope of Receiver Maintenance

This chapter contains direct support maintenance procedures for troubleshooting, testing, repairing, calibrating and adjusting the receiver. Paragraph 4-2 specifies receiver preventive maintenance. Detailed procedures are provided for troubleshooting (para 4-3 through 4-10), repairs (para 4-11 through 4-30), and calibration and adjustments (para 4-31 through 4-36). Procedures for deenergizing and energizing the radio set are provided in paragraphs 3-12 and 3-13.

4-2. Receiver Periodic Calibration Checks and Tests

Periodic calibration checks and tests must be performed as periodic preventive maintenance on the receiver to verify the calibration accuracy of metering circuits and check operating condition. Paragraph 2-4 lists the calibration checks and tests that must be performed on each unit of the radio set, and specifies the maintenance interval in which they should be performed.

4-3. Receiver Troubleshooting Chart

WARNING

Removal and replacement of parts, or continuity and resistance checks must not be performed while primary power is applied to the radio set.

a. General. The receiver troubleshooting chart is supplied as an aid in localizing troubles in the receiver. The chart lists the symptoms that may be observed when sectionalizing a trouble to the receiver. The chart also lists the probable trouble and includes or references procedures to be used to locate and correct the trouble.

b. Use of the Chart. The receiver troubleshooting chart d below) supplements the operational checks and corrective measures contained in TM 11-5820-595-12. Apply the operational checks and corrective measures in TM 11-5820-595-12 before using the troubleshooting chart in this manual. If the corrective measures for the operational checks in TM 11-5820-595-12 fail to correct the trouble or indicate that higher category maintenance is required, apply the corrective measures listed in the chart below. To use the chart, read down the symptom column of the chart until the abnormal indication or condition is found. Then perform the corrective measures indicated in the chart for that item.

c. Conditions for Troubleshooting. In general, receiver troubleshooting begins with the radio set turned on and connected for normal operation. During performance of the troubleshooting procedure, it is often necessary to check a part by substitution or to perform continuity or resistance checks. Instructions for performing continuity and resistance checks are provided in paragraph 4-4, and instructions for removal and replacement of parts are provided in paragraph 4-11. Figures 4-4 through 4-14 are parts location diagrams which will aid the repairman in locating parts in the receiver.

d. Receiver Troubleshooting Chart.

Item	*Symptom*	*Probable trouble*	*Corrective measures*
1	POWER 8 AMPS SLO-BLO fuse on receiver meter panel blows when replaced.	*a.* Blower 2A22B1 defective.....	*a.* Remove blower 2A22B1 (para 4-16) and check its resistance as follows: T1 to T4 should be 500 -100 ohms. T1 to T5 should be 800 +100 ohms.

Item	Symptom	Probable trouble	Corrective measures
		b. Capacitor 2A22C1 defective...	*b.* Check capacitor 2A22C1 by substitution (para 4-17).
		c. Defective wiring in primary power distribution circuits	*c.* Perform the receiver primary power distribution checks (para 4-5).
		d. Power transformer 2A22T1 defective	*d.* Check power transformer 2A22T1 by substitution (para 4-27).
2	TDA A 1 AMP SLO-BLO fuse on receiver meter panel blows when replaced.	Defective wiring in primary power distribution circuits.	Perform check steps 7, 8, and 9 of the receiver primary power distribution checks (para 4-5).
3	TDA B 1 AMP SLO-BLO fuse on receiver meter panel blows when replaced.	Defective wiring in primary power distribution circuits.	Perform check steps 10, 11, and 12 of the receiver primary power distribution checks (para 4-5).
4	Any indicator on power supply 2A3 not lighted.	*a.* Power supply chassis 2A3A5 defective	*a.* Check power supply chassis 2A3A5 by substitution (para 4-14). If indicator lights after 2A3A5 is replaced, use the power supply chassis 2A3A5 checks (para 4-7) to isolate the trouble.
		b. Defective component or wire in dc power distribution circuits.	*b.* Use the receiver dc power distribution checks (para 4-6) to isolate the trouble.
		c. Defective component or wire in primary power distribution circuits	*c.* Use the receiver primary power distribution checks (para 4-5) to isolate the trouble.
5	5V and 28V indicators on frequency synthesizer 2A21 not lighted.	*a.* Defective wiring	*a.* Remove frequency synthesizer 2A21 (para 4-25) and check for continuity between pins 5 and 6 of connector 2A22XA21 (fig. 8-59).
		b. Frequency synthesizer main chassis 2A21A10 defective.	*b.* Replace frequency synthesizer main 2A21A10 (para 4-25).
6	28V indicator on frequency synthesizer 2A21 not lighted.	Frequency synthesizer main chassis 2A21A10 defective.	Replace frequency synthesizer main chassis 2A21A10 (para 4-25).
7	5V indicator on frequency synthesizer 2A21 not lighted.	Same as item 6 above.....	Same as item 6 above.
8	TDA A OVEN indicator on receiver meter panel does not cycle on and off.	*a.* Defective wiring	*a.* Check for continuity between: pin 2 of 2A22XDS1 (fig. 8-59) and pin C of connector 2A22W1P2; and pin 1 of 2A22XDS1 and pin D of connector 2A22W1P2. Also check resistance between pin 3 of 2A22XDS1 and pin A of connector 2A22W1P2. Resistance should be 2200 ±220 ohms.
		b. Indicator light 2A22XDS1 defective.	*b.* Check indicator light 2A22XDS1 by substitution.
9	TDA B OVEN indicator on receiver meter panel does not cycle on and off.	*a.* Defective wiring	*a.* Check for continuity between: pin 2 of 2A22XDS2 (fig. 8-59) and pin C of connector 2A22W1P3; and pin 1 off 2A22XDS2 and pin D of connector 2A22W1P3. Also check resistance between pin 3 of 2A22XDS2 and pin A of connector 2A22W1P3. Resistance should be 2200 $\pm$220 ohms.

Item	Symptom	Probable trouble	Corrective measures
		b. Indicator light 2A22XDS2 defective.	*b.* Check indicator light 2A22XDS2 by substitution.
10	MULT OSC A OVEN indicator on receiver meter panel not lighted.	*a.* Defective wiring	*a.* Check for continuity between: pin 1 of 2A22XDS15 and pin G of 2A22A5XDS3 (fig. 8-59); and pin 2 of 2A22XDS15 and pin 6 of connector 2A24W1XA13.
		b. Indicator light 2A22XDS15 defective.	*b.* Check indicator light 2A22XDS15 by substitution.
11	MULT OSC B OVEN indicator on receiver meter panel not lighted.	*a.* Defective wiring	*a.* Check for continuity between: pin 1 of 2A22XDS16 and pin G of 2A22A5XDS3 (fig. 8-59); and pin 2 of 2A22XDS16 and pin 6 of connector 2A24W1XA14.
		b. Indicator light 2A22XDS16 defective.	*b.* Check indicator light 2A22XDS16 by substitution.
12	SYNTH OVEN indicator on receiver meter panel not lighted.	*a.* Defective wiring	*a.* Check for continuity between: pin 2 of 2A22XDS17 (fig. 8-59) and pin 1 of connector 2A22XA21; pin 1 of 2A22XDS17 and pin G of 2A22A5XDS3; and pin 3 of 2A22XDS17 and the E2 CAB GRD lug on top of the receiver cabinet.
		b. Indicator light 2A22XDS17 defective.	*b.* Check indicator light 2A22XDS17 by substitution.
13	Blower 2A22B1 not operating	*a.* Blower 2A22B1 defective	*a.* Remove blower 2A22B1 (para 4-16) and check its resistance as follows: T1 to T4 should be 500+100 ohms. T1 to T5 should be 800+100 ohms.
		b. Capacitor 2A22C1 defective	*b.* Check capacitor 2A22C1 by substitution (para 4-17).
14	Any module fault indicator lamp on frequency synthesizer 2A21 lighted.	Frequency synthesizer main chassis 2A21A10 defective.	Replace frequency synthesizer main chassis 2A21A10 (para 4-25).
15	Any step of the receiver power supply voltage checks (TM 11-5820-595-12) fails.	Same as item 4 in this chart	Refer to item 4 in this chart.
16	Any step of the receiver module test point checks (TM 11-5820-595-12) fails.	Defective component or wire in the dc power distribution circuits.	Use the receiver dc power distribution checks (para 4-6) to isolate the trouble.
17	All status and alarm indicators on the receiver meter panel not lighted.	*a.* POWER 8 AMPS SLO-BLO fuse 2A22F1 defective.	*a.* Check POWER 8 AMPS SLO-BLO neon fuse indicator on receiver meter panel. If lighted, refer to item 1 in this chart.
		b. Same as item 4 in this chart	*b.* Check indicators on power supply 2A3. If any indicator not lighted, refer to item 4 in this chart.
18	CARR (IF) A indicator on receiver meter panel lighted red.	*a.* Defective module in channel A local oscillator circuits.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to *A.* If 2A22M1 indication is not in yellow band, refer to item 43.

Item	Symptom	Probable trouble	Corrective measures
		b. Defective wiring	*b.* Turn meter selector switch 2A22S1 to CARRIER (IF) A. If 2A22M1 indication is between 10 and 100 and is varying, remove alarm monitor 2A20 and check resistance between pin 5 and 15 of connector 2A24W1XA20B (fig. 8-59). Resistance should be greater than 10 ohms. Also check for continuity between pin 14 of connector 2A24W1XA16 and pin 20 of connector 2A24W1XA20A; and pin 15 of connector 2A24W1XA16 and pin 22 of connector 2A24W1XA20A
		c. Coaxial cable 2W1 or 2W2 defective.	*c.* One at a time, check coaxial cables 2W1 and 2W2 by substitution (fig. 4-12).
		d. 4.4-5.0 GHz circulator 2HY1 defective.	*d.* Check 4.4-5.0 GHz circulator 2HY1 by substitution (para 4-20).
		e. Post selector 2FL6 defective..	*e.* Check post selector 2FL6 by substitution (para 4-21).
		f. Preselector 2FL4 defective	*f.* Check preselector 2FL4 by substitution (para 4-19).
		g. Elbow coupler 2CP1 defective	*g.* Check Elbow coupler 2CP1 (fig. 4-10) by substitution.
19	CARR (IF) B indicator on receiver meter panel lighted red.	*a.* Defective module in channel B local oscillator circuits.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to B. If 2A22M1 indication is not in yellow band, refer to item 44.
		b. Defective wiring	*b.* Turn meter selector switch 2A22S1 to CARRIER (IF) B. If 2A22M1 indication is between 10 and 100, and is varying, remove alarm monitor 2A20 and check resistance between pin 5 and 20 of connector 2A24W1XA20B (fig. 8-59). Resistance should be greater than 10 ohms. Also check for continuity between pin 16 of connector 2A24W1XA16 and pin 16 of connector 2A24W1XA20A
		c. Coaxial cable 2W3 or 2W4 defective.	*c.* One at a time, check coaxial cables 2W3 and 2W4 by substitution (fig. 4-12).
		d. 4.4-5.0 GHz circulator 2HY2 defective.	*d.* Check 4.4-5.0 GHz circulator 2HY2 by substitution (para 4-20).
		e. Post selector 2FL7 defective..	*e.* Check post selector 2FL7 by substitution (para 4-21).
		f. Preselector 2FL5 defective	*f.* Check preselector 2FL5 by substitution (para 4-19).
		g. Elbow coupler 2CP2 defective	*g.* Check elbow coupler 2CP2 (fig. 4-10) by substitution.
20	CARR (IF) A and CARR (IF) B indicators on receiver meter panel lighted red.	*a.* Defective module in receiver local oscillator circuits.	*a.* Turn meter selector switch 2A22S1 to SYNTHESIZER. If this meter indication is not in the yellow band,

Item	Symptom	Probable trouble	Corrective measures
			refer to item 25 in this chart. One at a time, check each of the meter switch positions and troubleshoot based on abnormal meter indication.
		b. Defective wiring	*b.* Remove alarm monitor 2A20 and perform continuity checks on Connectors 2A24W1XA20A and 2A24W1XA20B (fig. 8-59) wiring.
21	VCO LOCK indicator on receiver meter panel lighted red.	*a.* Defective wiring	*a.* Turn meter selector switch 2A22S1 to VCO FREQ DIFF. If 2A22M1 indication is in blue band, remove alarm monitor 2A20 and check resistance between pin 5 and 29 of connector 2A24W1XA20B (fig. 8-59).
		b. Coaxial cable 2A24W10 or 2A24W13 defective	*b.* If VCO FREQ DIFF meter indication is not in blue band, and CARR (IF) A and CARR (IF) B indicators on receiver meter panel are lighted green: Remove alarm monitor 2A20; disconnect non-captivated ends of coaxial cables 2A24W10 and 2A24W13 (fig. 4-12) and check for continuity between the center conductor of 2A24W10 and pin A1 of connector 2A24W1XA20A Also check for continuity between the center conductor of 2A24W13 and pin A2 of connector 2A24W1XA20A
22	SYNTH LOCK indicator on receiver meter panel lighted red.	*a.* Frequency synthesizer main chassis 2A21A10 defective.	*a.* Check frequency synthesizer main chassis 2A21A10 by substitution (para 4-25).
		b. Defective wiring	*b.* Remove frequency synthesizer 2A21 (para 4-25) and alarm monitor 2A20, and check for continuity between pin 7 of connector 2A22XA21 and pin 17 of connector 2A24W1XA20A (fig. 8-59). Also check resistance between pin 5 and 9 of connector 2A24W1XA20B. Resistance should be greater than 10 ohms.
23	TRAF indicator on receiver meter panel lighted red.	Defective wiring	Remove modules 2A17, 2A19, and 2A20. Make continuity checks from terminals of connector 2A24XA17 to associated terminals on connector 2A24W1P1 (fig. 4-4 and 8-59). Make continuity checks from terminals of connector 2A24W1XA19 to associated terminals on connector 2A24W1P1. Make continuity checks from terminal 12 of connector 2A24W1XA20A and terminals 10 and 11 of connector 2A24W1XA20B to associated terminals of connector 2A24W1P1. Make a continuity check between pin 13 of connector 2A24W1XA20A to pin 9 of connector 2A24W1XA19.

Item	Symptom	Probable trouble	Corrective measures
24	No indication on meter 2A22M1 when meter selector switch 2A22S1 is set to each of its positions.	*a.* Meter selector switch 2A22S1 defective.	*a.* Set meter selector switch 2A22S1 to TEST LEAD (+) and check for continuity between pins C (wiper arm contact) and 24 of 2A22S1B (fig. 8-59). Also check for continuity between pin C (wiper arm contact) of 2A22S1A and the E2 CAB GRD lug on top of the receiver.
		b. Meter 2A22M1 defective	*b.* Check meter 2A22M1 using the calibration procedure given in paragraph 4-32.
25	SYNTHESIZER meter indication not in yellow band	*a.* Frequency synthesizer main chassis 2A21A10 defective	*a.* Check frequency synthesizer main chassis 2A21A10 by substitution (para 4-25).
		b. Defective metering circuit.....	*b.* Remove frequency synthesizer 2A21 (para 4-25) and check for continuity between pin Al of connector 2A22XA21 and pin 2 of 2A22S1B (fig. 8-59). Also check for continuity between pin 2 of 2A22S1A and the E2 CAB GRD lug on top of receiver.
26	AMPL-MULT meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A2261 to LOCAL OSC POWER. If 2A22M1 indication is in yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Same as item 25 in this chart	*b.* Turn meter selector switch 2A22S1 to SYNTHESIZER. If 2A22M1 indication is not in yellow band, refer to item 25 in this chart.
		c. Coaxial cable 2A22W5 defective	*c.* Check coaxial cable 2A22W5 by substitution (fig. 4-12).
		d. Defective wiring	*d.* Remove amplifier-multiplier 2A8 (TM 11-5820-595-12) and make continuity checks from 2A24XA8 terminals to the connections at 2A24W1P1 (fig. 8-59).
		e. 1137-1213 MHz circulator 2HY3 or 1137-1213 MHz bandpass filter 2FL10 defective.	*e.* Check 1137-1213 MHz circulator 2HY3 and 1137-1213 MHz bandpass filter 2FL10 by substitution (para 4-30).
27	2ND MULT meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER. If 2A22M1 indication is in yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Same as item 26 in this chart	*b.* Turn meter selector switch 2A22S1 to AMPL-MULT. If 2A22S1 indication is not in yellow band, refer to item 26 in this chart.
		c. 2275-2425 MHz circulator 2A7HY1 defective.	*c.* Check 2275-2425 MHz circulator 2A7HY1 by substitution (para 4-24).

Item	Symptom	Probable trouble	Corrective measures
		d. 1137-1213 MHz circulator 2HY3 or 1137-1213 MHz bandpass filter 2FL10 defective.	*d.* Check 1137-1213 MHz circulator 2HY3 and 1137-1213 MHz bandpass filter 2 FL10 by substitution (para 4-30).
28	MULT OSC A meter indication not in black band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set A-B switch 2A22S3 to A. If 2A22M1 indication is in the yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Defective wiring	*b.* Remove module 2A13 (para 3-12) and check continuity from 2A24W1XA13 terminals to the connections at 2A24W1P1 (fig. 8-59).
29	MULT OSC B meter indication not in black band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to B. If 2A22M1 indication is in the yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Defective wiring	*b.* Remove module 2A14 (para 3-12) and check continuity from 2A24W1XA14 terminals to connections at 2A24W1P1 (fig. 8-59).
30	FREQ MIXER CURRENT (3RD MULT) A1 meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to A If 2A22M1 indication is in the yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Same as item 28 in this chart.	*b.* Turn meter selector switch 2A22S1 to MULT OSC A. If 2A22M1 indication is not in black band, refer to item 28 in this chart.
		c. Same as item 27 in this chart.	*c.* Turn meter selector switch 2A22S1 to 2ND MULT. If 2A22M1 indication is not in yellow band, refer to item 27 in this chart.
		d. 2275-2425 MHz circulator 2A7HY1 defective.	*d.* Check 2275-2425 MHz circulator 2A7HY1 by substitution (para 4-24).
		e. 4550-4950 MHz power divider 2A7HY2 defective.	*e.* Check 4550-4950 MHz power divider 2A7HY2 by substitution (para 4-24).
31	FREQ MIXER CURRENT (3RD MULT) A2 meter indication not in yellow band.	Same as item 30 in this chart	Refer to item 30 in this chart.
32	FREQ MIXER CURRENT (3RD MULT) B1 meter indication not in yellow band.	*a.* Metering circuit requires calibration.	*a.* Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to B. If 2A22M1

Item	Symptom	Probable trouble	Corrective measures
			indication is in the yellow band, perform the receiver local oscillator chain output power and metering test (para 4-10).
		b. Same as item 29 in this chart	*b.* Turn meter selector switch 2A22S1 to MULT OSC B. If 2A22M1 indication is not in black band, refer to item 29 in this chart.
		c. Same as item 27 in this chart.	*c.* Turn meter selector switch 2A22S1 to 2ND MULT. If 2A22M1 indication is not in yellow band, refer to item 27 in this chart.
		d. 2275-2425 MHz circulator 2A7HY1 defective.	*d.* Check 2275-2425 MHz circulator 2A7HY1 by substitution (para 4-24).
		e. 4550-4950 MHz power divider 2A7HY2 defective.	*e.* Check 4550-4950 MHz power divider 2A7HY2 by substitution (para 4-24).
33	FREQ MIXER CURRENT (3RD MULT) B2 meter indication not in yellow band.	Same as item 32 in this chart	Refer to item 32 in this chart.
34	AMPL-MIXER CURRENT A1 meter indication not in yellow band.	Same as item 43 in this chart	Refer to item 43 in this chart.
35	AMPL-MIXER CURRENT A2 meter indication not in yellow band.	Same as item 43 in this chart	Refer to item 43 in this chart.
36	AGC meter indication continuously exceeds 150.	Same as item 20 in this chart	Refer to item 20 in this chart.
37	AMPL-MIXER CURRENT B1 meter indication not in yellow band.	Same as item 44 in this chart	Refer to item 44 in this chart.
38	AMPL-MIXER CURRENT B2 meter indication not in yellow band.	Same as item 44 in this chart.	Refer to item 44 in this chart.
39	CARRIER (IF) A meter indication does not vary and is less than 10 or greater than 150.	Same as item 8 in this chart	Refer to item 18 in this chart.
40	CARRIER (IF) B meter indication does not vary and is less than 10 or greater than 150.	Same as item 19 in this chart	Refer to item 19 in this chart.
41	CARRIER (IF) COMBINED meter indication not in orange band.	Same as item 20 in this char	Check CARR (IF) A and CARR (IF) B indicators on receiver meter panel. If both of these indicators are lighted red, refer to item 20 in this chart.
42	TRAFFIC meter indication not in orange band.	*a.* Same as item 23 in this chart	*a.* Check TRAF indicator on receiver meter panel. If this indicator is lighted red, refer to item 23 in this chart.
		b. Metering circuit requires calibration.	*b.* Calibrate the receiver traffic metering circuit (para 4-33).

Item	Symptom	Probable trouble	Corrective measures
43	LOCAL OSC POWER meter indication is not in yellow band when switch 2A22S3 is set to A.	*a.* Metering circuit requires calibration.	*a.* Calibrate the receiver local oscillator output power metering circuits (para 4-34).
		b. Coaxial cable 2W11 or 2W12 defective.	*b.* Check coaxial cables 2W11 and 2W12 by substitution (fig. 4-12).
		c. Local oscillator filter 2 FL8 defective.	*c.* Check local oscillator filter 2 FL8 by substitution (para 4-22).
44	LOCAL OSC POWER meter indication is not in yellow band when switch 2A22S3 is set to B.	*a.* Metering circuit requires calibration.	*a.* Calibrate the receiver local oscillator output power metering circuits (para 4-34).
		b. Coaxial cable 2W14 or 2W15 defective	*b.* Check coaxial cables 2W14 and 2W15 by substitution (fig. 4-12).
		c. Local oscillator filter 2 FL9 defective.	*c.* Check local oscillator filter 2 FL9 by substitution (para 4-22).
45	Frequency synthesizer 2A21 frequency error greater than 48 kHz as determined by test (para 4-8)	*a.* Standard RF oscillator 2A21A7 defective.	*a.* Check standard RF oscillator 2A21A7 by substitution.
		b. RF oscillator 2A21A1 defective.	*b.* Check RF oscillator 2A21A1 by substitution.
		c. Frequency synthesizer 2A21 defective.	*c.* Check frequency synthesizer 2A21 by substitution (para 4-25).
46	Receiver frequency error greater than 50 kHz as determined by test (para 4-8).	220 MHz vco's 2A13 and 2A14 require frequency adjustment.	Perform the receiver VCO frequency adjustment (para. 4-36).
47	Receiver APC circuit will not lock as determined by test (para 4-9)	*a.* 220 MHz vco's 2A13 and 2A14 require frequency adjustment.	*a.* Perform the receiver VCO frequency adjustment (para 4-36).
		b. Combiner 2A16 defective	*b.* Check combiner 2A16 by substitution.
48	Receiver channel A local oscillator output power less than 0.5 milliwatts as determined by test (para 4-10)	*a.* Frequency synthesizer 2421 defective.	*a.* Check frequency synthesizer 2A21 by substitution (para 4-25).
		b. Amplifier-multiplier 2A8 defective	*b.* Check amplifier-multiplier 2A8 by substitution (TM 11-5820-595-12).
		c. 220 MHz vco 2A13 defective	*c.* Check 220 MHz vco 2A13 by substitution.
		d. Frequency multiplier group 2A7 defective.	*d.* Check frequency multiplier group 2A, by substitution (TM 11-5820-595-12).
		e. Frequency mixer 2A6 defective	*e.* Check frequency mixer 2A6 by substitution.
49	Receiver Channel B local oscillator output power less than 0.5 milliwatts as determined by test (para 4-10)	*a.* Frequency synthesizer 2A21 defective.	*a.* Check frequency synthesizer 2A21 by substitution (para 4-25).
		b. Amplifier-multiplier 2A8 defective	*b.* Check amplifier-multiplier 2A8 by substitution (TM 11-5820-595-12).
		c. 220 MHz vco 2A14 defective	*c.* Check 220 MHz vco 2A14 by substitution.
		d. Frequency multiplier group 2A7 defective.	*d.* Check frequency multiplier group 2A7 by substitution (TM 5820-595-12).
		e. Frequency mixer 2A9 defective	*e.* Check frequency mixer 2A9 by substitution.
50	Cannot calibrate the TRAFFIC metering circuit (para 4-33).	Defective component or wire in metering circuit.	Remove alarm monitor 2A20 (para 3-12) and check resistance between pin 12 of connector 2A24W1XA20A and pin 21 of

Item	Symptom	Probable trouble	Corrective measures
			2A22S1B (fig. 8-59). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A22R11 (fig. 4-5) is varied from one extreme to the other. Also check for continuity between pin 21 of 2A22S1A and the E2 CAB GRD lug on top of the receiver.
51	Cannot calibrate the receiver channel A local oscillator power output metering circuit (para 4-34).	Defective component or wire in metering circuit.	Check that switch 2A22S3 is set to A, and then remove amplifier mixer 2A4 and check resistance between pip 8 of connector 2A24XA4 and pin 22 of 2A22S1B (fig. 8-59). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A22R9 (fig. 4-5) is varied from one extreme to the other. Also check for continuity between pin 9 of connector 2A24XA4 and pin 22 of 2A22S1A.
52	Cannot calibrate the receiver channel B local oscillator power output metering circuit (para 4-34).	Defective component or wire in metering circuit.	Check that switch 2A22S3 is set to B, and then remove amplifier-mixer 2A11 and check resistance between pin 8 of connector 2A24XA11 and pin 22 of 2A22S1B (fig. 8-59). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A22R10 (fig. 4-5) is varied from one extreme to the other. Also check for continuity between pin 9 of connector 2A24XA11 and pin 22 of 2A22S1A.
53	Cannot calibrate the AMPL-MULT local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Check resistance between the center conductor of coaxial cable 2A24W7 and pin 3 of 2A22S1A (fig. 8-59). Note that resistance varies smoothly from zero to 1,000 ohms as potentiometer 2A22R1 (fig. 4-5) is varied from one extreme to the other. Make the same resistance check between pin 3 of 2A22S1A and the E2 CAB GRD lug on top of the receiver.
54	Cannot calibrate the 2ND MULT local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Check resistance between the center conductor of coaxial cable 2A24W8 and pin 4 of 2A22S1A (fig. 8-59). Note that resistance varies smoothly from zero to 1,000 ohms as potentiometer 2A22R2 (fig. 4-5) is varied from one extreme to the other. Make the same resistance check between pin 4 of 2A22S1A and the E2 CAB GRD lug on top of the receiver.
55	Cannot calibrate the MULT OSC A local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Remove 220 MHz vco 2A13 and check resistance between pin 9 of connector 2A24W1XA13 and pin 5 of 2A22S1B (fig. 8-59). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A22R3 (fig. 4-5) is varied from one extreme to the other. Make the same resistance check between pin 5 of 2A22S1B and the E2 CAB GRD lug on top of the receiver.

Item	*Symptom*	*Probable trouble*	*Corrective measures*
56	Cannot calibrate the MULT OSC B local oscillator chain metering circuit (para 4-35)	Defective component or wire in metering circuit.	Remove 220 MHz vco 2A14 and check resistance between pin 9 of connector 2A24W1XA14 and pin 6 of 2A22S1B (fig. 8-59). Note that resistance varies smoothly from zero to 5,000 ohms as potentiometer 2A22R4 (fig. 4-5) is varied from one extreme to the other. Make the same resistance check between pin 6 of 2A22S1B and the E2 CAB GRD lug on top of the receiver.
57	Cannot calibrate the FREQ MIXER CURRENT (3RD MULT) A1 local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Remove frequency mixer 2A6 and check resistance between pin 8 of connector 2A24W1XA6 and pin 7 of 2A22S1A (fig. 8-59). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A22R5 (fig. 4-5) is varied from one extreme to the other.
58	Cannot calibrate the FREQ MIXER CURRENT (3RD MULT) A2 local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Remove frequency mixer 2A6 and check resistance between pin 9 of connector 2A24W1XA6 (fig. 4-14) and pin 8 of 2A22S1A (fig. 4-5). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A22R6 (fig. 4-5) is varied from one extreme to the other.
59	Cannot calibrate the FREQ MIXER CURRENT (3RD MULT) B1 local oscillator chain metering circuit (para 4-35)	Defective component or wire in metering circuit.	Remove frequency mixer 2A9 and check resistance between pin 8 of connector 2A24W1XA9 (fig. 4-14) and pin 9 of 2A22S1A (fig. 4-5). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A22R7 (fig. 4-5) is varied from one extreme to the other.
60	Cannot calibrate the FREQ MIXER CURRENT (3RD MULT) B2 local oscillator chain metering circuit (para 4-35).	Defective component or wire in metering circuit.	Remove frequency mixer 2A9 and check resistance between pin 9 of connector 2A24W1XA9 and pin 10 of 2A22S1A (fig. 8-59). Note that resistance varies smoothly from zero to 50,000 ohms as potentiometer 2A22R8 (fig. 4-5) is varied from one extreme to the other.

4-4. Receiver Continuity and Resistance Checks

WARNING

115 vac is present in the receiver. Do not perform any continuity or resistance check while the radio set is energized.

To perform any continuity or resistance check given in the receiver troubleshooting chart, proceed as follows:

a. deenergize the radio set (para 3-12).

b. Connect the TS-352B/U test leads between the two points given in the troubleshooting chart.

c. For continuity checks observe that the meter indication on TS-352B/U is less than 5 ohms. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

d. For resistance checks observe that the indication is within the tolerance specified in the troubleshooting chart. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

e. After the trouble has been corrected, energize the radio set (para 3-13) and check that the corrective action taken has corrected the trouble.

4-5. Isolating Troubles in Receiver Primary Power Distribution Circuits

WARNING

115 vac is present in the receiver. Do not perform any trouble isolation check given in this paragraph while the radio set is energized.

To isolate a trouble in the primary power distribution circuit of the receiver, proceed as follows:

a. Remove power supply 2A3 from the receiver (para 4-14).

b. Remove switch 2A22S2 protective cover (fig. 4-10) by removing the four nuts and two screws securing it to the receiver meter panel.

c. Remove frequency synthesizer 2A21 from the receiver (para 4-25).

d. Remove connectors 2A22W1P2 and 2A22W1P3 from their mating connectors on the rear of tunnel diode amplifiers 2A1 and 2A2 (fig 4-8).

e. On the, TS-352B/U, turn the FUNCTION switch on OHMS, and connect the two test leads supplied with TS-352B/U to the OHMS terminals.

f. Refer to the primary power distribution check point chart provided in step *i.* Set the range switch on TS-352B/U to the position indicated for check step 1, and connect the TS-352B/U test leads between receiver check points 1 and 2 for the same check step.

g. Observe that TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If not, use the receiver interconnecting diagram (fig. 859) to trace and isolate the trouble.

h. Repeat steps f and g information for each successive check step listed in the chart.

i. Primary Power Distribution Check Point Chart.

Check step	Range switch position on TS-352B /U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
1	RX1	2A22J5-A	2A22S2-4	Less than 1
2	RX1	-A	2A22S2-3	Less than 1'
3	RX10000	-A	2A22E2 (CAB GRD)	Infinity
4	RX1	-B	2A22E2 (CAB GRD)	Less than 1
5	RX1	-C	2A22S2-2	Less than 1
6	RX1	-C	2A22S2-2	Less than 1'
7	RX10000	-C	2A22E2 (CAB GRD)	Infinity
8	RX1	2A22S2-1	2A22W1P2-B	Zero
9	RX1	-3	2A22W1P2-A	Less than 2
10	RX100	-3	2A22XDS1-3	2.2K 220
11	RX1	2A22S2-1	2A22W1P3-B	Zero
12	RX1	-3	2A22W1P3-A	Less than 2
13	RX100	-3	2A22XDS2-3	2.2K-220
14	RX1	2A22S2-1	2A22XA21-6	Zero
15	RX1	-1	2A22XA21-10	Zero
16	RX1	-3	2A22XA21-5	Zero
17	RX1	-3	2A22XA21-9	Zero
18	RX1	2A22S2-1	2A22S2-3	Less than 2
19	RX1	2A22XA3-12	2A22XA3-31	Less than 1
20	RX1	-14	2A22XA3-33	Less than 1
21	RX1	-16	2A22XA3-35	Less than 1
22	RX1	-18	2A22XA3-37	Less than 1
23	RX1	-19	2A22E2 (CAB GRD)	Zero

a Switch 2A22S2 set to OFF position.
b Switch 2A22S2 set to ON position.

4-6. Isolating Troubles in Receiver DC Power Distribution Circuits

WARNING

115 vac is present in the receiver. Do not perform any of the trouble isolation checks given in this paragraph while the radio set is energized.

To isolate a trouble in the de power distribution circuit of the receiver, proceed as follows:

a. Remove power supply 2A3 from the receiver (para 4-14).

b. Remove modules 2A4, 2A8, 2A11, 2A12, 2A13, 2A14, 2A15, 2A16, 2A17, 2A19, and 2A20 from the receiver (TM 11-5820-595-12).

c. Remove connectors 2A22W1P2 and 2A22W1P3 (fig. 4-8) from their mating connectors on the rear of tunnel diode amplifiers 2A1 and 2A2.

d. On the TS-352B/U, turn the FUNCTION switch to OHMS, and connect the two test leads supplied with TS-352B/U to the OHMS terminals.

e. Refer to the dc power distribution check point chart provided in step *h.* Set the range switch TS-352B/U for the position indicated in check step 1, and connect the TS-352B/U test leads between receiver check points 1 and 2 of the same check step.

f. Observe that TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If not, use the receiver interconnecting diagram (fig. 8-59) to trace and isolate the trouble.

g. Repeat steps e and f information above for each successive check step listed in the chart.

h. DC Power Distribution Check Point Chart.

Check step	Range switch position on TS-352B /U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
1	RX1	2A22XA3-1	2A24XA8-1	Less than 1
2	RX1	-1	2A24W1XA13-1	Zero
3	RX1	-1	2A24W1XA14-1	Zero
4	RX10000	-1	2A22E2 (CAB GRD)	Infinity
5	RX10000	-1	2A22XA3-20	Infinity
6	RX1	-20	2A24XA8-2	Less than 1
7	RX1	-20	2A24W1XA13-2	Zero
8	RX1	-20	2A24W1XA14-2	Zero
9	RX1	-3	2A24XA4-3	Less than 1
10	RX1	-3	2A24XA11-3	Less than 1
11	RX1	-3	2A24W1XA12-3	Less than 1
12	RX1	-3	2A24W1XA15-3	Less than 1
13	RX1	-3	2A23W1XA16-3	Zero
14	RX1	-3	2A24XA17-3	Less than 1
15	RX1	-3	2A24W1XA19-3	Zero
16	RX10000	-3	2A22E2 (CAB GRD)	Infinity
17	RX10000	-4	2A22W1P22	Zero
19	RX1	-4	2A22W1P3-E	Zero
20	RX10000	-4	2A22E2 (CAB GRD)	Infinity
21	RX10000	-4	2A22XA3-23	Infinity
22	RX1	-22	2A24XA4-4	Less than 1
23	RX1	-22	2A24XA11-4	Less than 1
24	RX1	-22	2A24W1XA12-4	Less than 1
25	RX1	-22	2A24W1XA15-4	Less than 1
26	RX1	-22	2A24W1XA16-4	Zero
27	RX1	-22	2A24XA17-4	Less than 1
28	RX1	-22	2A24W1XA19-4	Zero
29	RX1	-23	2A22W1P2-F	Zero
30	RX1	-23	2A22W1P3-F	Zero
31	RX1	-5	2A24WIXA13-7	Zero
32	RX1	-5	2A24W1XA14-7	Zero
33	RX1	-5	2A24W1XA16-6	Zero
34	RX1	-5	2A24W1XA20B-16	Zero
35	RX10000	-5	2A22E2 (CAB GRD)	Infinity
36	RX10000	-5	2A22XA3-24	Infinity
37	RX1	-24	2A24W1XA13-8	Zero
38	RX1	-24	2A24W1XA14-8	Zero
39	RX1	-24	2A24W1XA16-7	Zero
40	RX1	-24	2A24W1XA20B-17	Zero
41	RX1	-7	2A24WIXA13-3	Zero
42	RX1	-7	2A24W1XA14-3	Zero

Check step	Range switch position on TS-352B /U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
43	RX1	2A22XA3-7	2A24W1XA20B-1	Zero
44	RX10000	-7	2A22E2 (CAB GRD)	Infinity
45	RX10000	-7	2A22XA3-26	Infinity
46	RX1	-8	2A22A5XDS3-G	Zero
47	RX1	-8	2A22A7XDS7-G	Zero
48	RX1	-8	2A22A6XDS11-G	Zero
49	RX1	-8	2A22XDS15-1	Zero
50	RX1	-8	2A22XDS16-1	Zero
51	RX1	-8	2A22XDS17-1	Zero
52	RX1	-26	2A24W1XA13-4	Zero
53	RX1	-26	2A24W1XA14-4	Zero
54	RX1	-26	2A24W1XA20B-2	Zero
55	RX1	-27	2A22E2 (CAB GRD)	Zero

4-7. Isolating Troubles in Power Supply Chassis 2A3A5

To isolate a trouble in power supply chassis 2A3A5, proceed as follows:

a. Remove plug-in modules 2A3A1 through 2A3A4 from power supply chassis 2A3A5 by performing steps *(1)* through *(7)* of paragraph 4-14*a.*

b. Remove the four screws and associated washers securing the rear shield (fig. 4-6) to power supply chassis 2A3A5.

c. On the TS-352B/U, turn the FUNCTION switch to OHMS, and connect the two test leads supplied with TS-252B/U to the OHMS terminals.

d. Refer to power supply chassis 2A3A5 check point chart provided in step *g.* Set the range switch on TS-352B/U for the position indicated in check step 1, and connect the TS-352B/U test leads between check points 1 and 2 of the same check step.

e. Observe that TS-352B/U meter indication is within the tolerance specified in the chart for that check step. If not, use the power supply 2A3 interconnecting diagram (fig. 8-60) to trace and isolate the trouble.

f. Repeat steps d and e information above for each successive check step listed in the chart.

g. Power Supply Chassis 2A3A5 Check Point Chart.

Check step	Range switch position on TS-352B /U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
1	RX10000	2A3A5P1-1	2ASA5J1	1.1 Meg ±55K
2	RX1	-1	2A3A5XA1-7	Zero
3	RX100	-1	2A3A5XA1-8	Less than 600
4	RX1	-1	2A3A5XA1-13	Zero
5	RX1	-12	2A3A5XA1-14	Less than 1
6	RX1	-20	2A3A5XA1-8	Zero
7	RX1	-31	2A3A5XA1-15	Zero
8	RX10000	-3	2A3A5J2	604K ±6K
9	RX1	-3	2A3A5P1-4	Zero
10	RX1	-3	2A3A5XA2-5	Zero
11	RX100	-3	2A3A5XA2-8	Less than 330
12	RX1	-3	2A3A5XA2-13	Zero
13	RX1	-14	2A3A5XA2-14	Less than 1
14	RX1	-22	2A3A5XA2-8	Zero
15	RX1	-23	2A3A5XA2-9	Zero
16	RX1	-33	2A3A5A2-15	Zero
17	RX1	-5	2A3A5XA3-8	Zero
18	RX100	-5	2A3A5XA3-13	Less than 250
19	RX10000	-5	2A3A5J3	475K ±47K
20	RX1	-16	2A3A5XA3-14	Less than 1
21	RX1	-24	2A3A5XA3-3	Zero
22	RX1	-24	2A3A5XA3-13	Zero
23	RX1	-35	2A3A5XA3-15	Zero
24	RX10000	-7	2A3A5J4	1.1 Meg ±55 K
25	RX1	-7	2A3A5XA4-7	Zero

Check step	Range switch position on TS-352B /U	Transmitter check points		TS-352B/U indication in ohms
		Point 1	Point 2	
26	RX100	2A3A5P1-7	2A3A5XA4-8	Less than 600
27	RX1	-7	2A3A5XA4-13	Zero
28	RX1	-7	2A3A5P1-8	Zero
29	RX1	-18	2A3A5XA4-14	Less than 1
30	RX1	-26	2A3A5XA4-8	Zero
31	RX1	-27	2A3A5P1-26	Zero
32	RX1	-37	2A3A5XA4-15	Zero

4-8. Receiver Frequency Accuracy Test

a. General. The receiver frequency accuracy test is used to check the frequency generating components of the receiver and determine when corrective action must be taken. The test must be performed at the periodic maintenance interval specified in paragraph 2-4 and when indicated in the receiver troubleshooting chart (para 4-3d). The performance standards listed in the chart (*e* below) indicate the minimum requirements for equipment maintained in the field and the corrective action to be taken if the performance standards are not met. This test will interrupt receive radio communications.

b. Test Equipment Required.

(1) Counter Electronic, Digital Readout AN/USM-207.

(2) Adapter, TNC male to BNC female 11PC4 (part of Mk-1207/GRC).

(3) Adapter, BNC to subminiature 11CP3 (part of MK-1207/GRC).

c. Test and Conditions. This procedure assumes that the radio set is turned on and connected for normal operation at the start of the test. Prior to performing the test, the maintenance man should notify the Multiplexer TD-204/U and distant radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

d. Initial Test Equipment Turn-on. Turn on the AN/USM-207 and allow a 15 minute warmup period.

e. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment order test	Test procedure	Performance standard
1	AN/USM-207 SENSITIVITY: PLUG-IN FUNCTION: FREQ	N/A	*a.* Record the receiver operating frequency synthesizer 2A21 controls.	a. None.
	Time base switch to GATE TIME (SEC^{-1}) -10		*b.* Set the controls on frequency synthesizer 2A21 on 4490.0 MHz.	*b.* None.
	Converter attenuator switches to 10V MAX		*c.* Disconnect coaxial cable 2A22W5 from the OUTPUT J8 connector on frequency synthesizer 2A21.	*c.* None.
	DIRECT-HETERO-DYNE: HETERO-DYNE		*d.* Connect the equipment as shown in view A, figure 4-1.	*d.* None.
	Mixing frequency selector to 250-MHz		*e.* Observe the LEVEL METER on AN/USM-207. If meter indication is in the green zone, proceed to step g below. Otherwise, perform step *f* below.	*e.* None.
	DISPLAY control to desired display time.		*f.* Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.	*f.* None.
			g. Observe digital display on AN/USM-207. Record difference between this frequency and 40	*g.* Frequency synthesizer 2A21 frequency error (recorded as Error

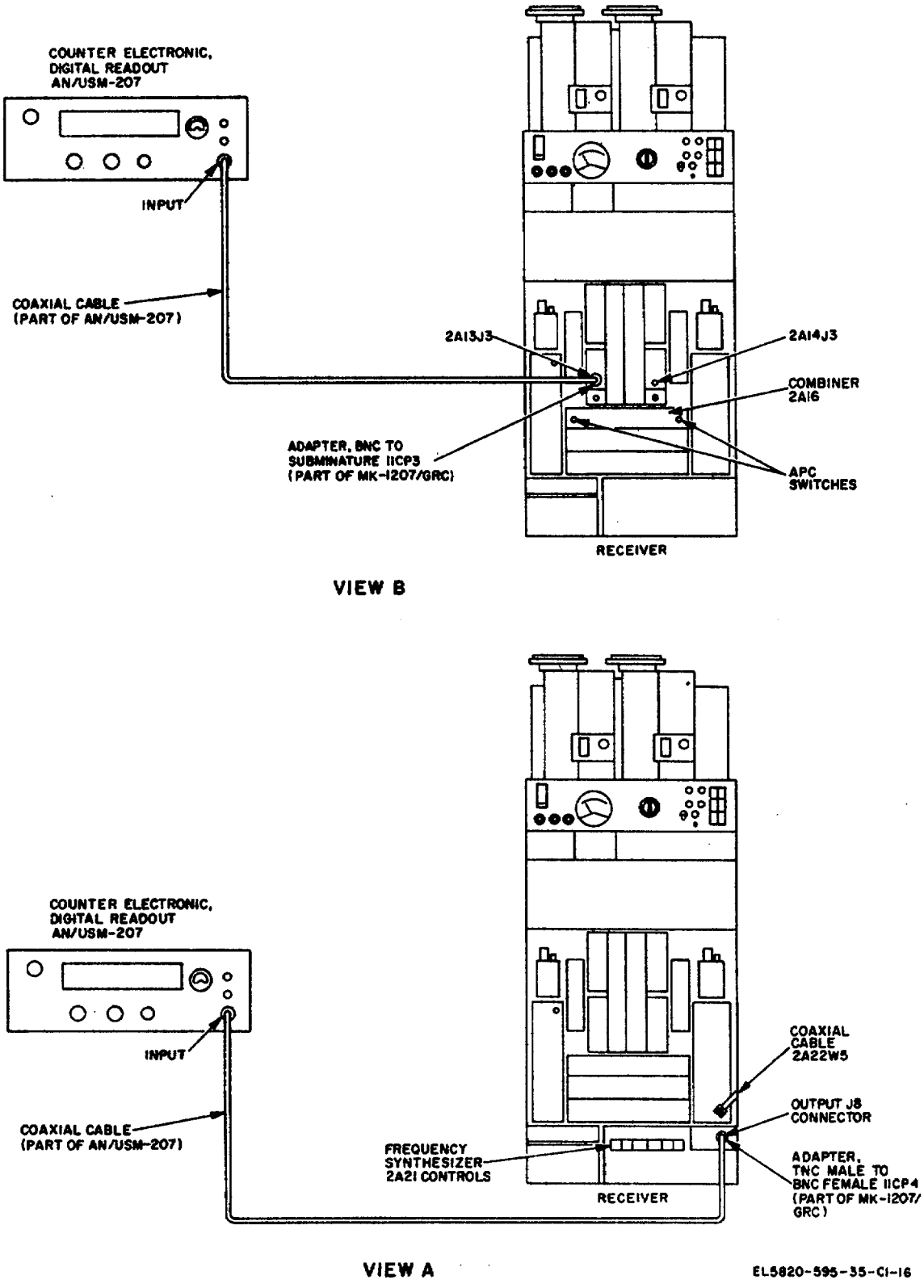


Figure 4-1. Receiver frequency accuracy test set up.

Step No.	Control settings: Test equipment	Control settings: Equipment order test	Test procedure	Performance standard
			MHz, ignoring plus or minus sign. Multiply difference by 16 and record as Error Frequency 1.	Frequency 1) shall not be greater than 48 KHz. If it is greater, refer to the receiver troubleshooting chart (item 45, para 4-3d) for corrective measures.
			h. Disconnect the adapter from OUTPUT J8 connector on frequency synthesizer 2A21	*h.* None.
			i. Connect coaxial cable 2A22W5 to the OUTPUT J8 connector on frequency synthesizer 2A21.	*i.* None.
			j. Disconnect coaxial cables 2A24W10 and 2A24W13 from 2A13J3 and 2A14J3.	*j.* None.
			k. Set both of the APC switches on combiner 2A16 to OFF.	*k.* None.
			l. Connect the equipment as shown in view B, figure 4-1.	*l.* None.
			m. Observe the LEVEL METER on AN/USM-207. If meter indication is in the green zone, proceed to step o below. Otherwise, perform step n below.	*m.* None.
			n. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.	*n.* None.
			o. Observe digital display on AN/USM-207. Record difference between this frequency and 20 MHz, ignoring plus or minus sign. Record this difference as Error Frequency A.	*o.* None.
			p. Disconnect the BNC to subminiature adapters 11CP3 from 2A13J3 and connect it to 2A14J3.	*p.* None.
			q. Observe digital display on AN/USM-207. Record difference between this frequency and 20 MHz ignoring plus or minus sign. Record this difference as Error Frequency B.	q. None.
			r. Add Error Frequency 1 (step g) and either Error Frequency A (step o) or Error Frequency B (step q), whichever is greater. This is the receiver's frequency error. Record.	*r.* Receiver frequency error shall not be greater than 50 kHz. If it is, refer to the receiver troubleshooting chart (item 46, para 4-3d) for corrective action.
			s. Turn the AN/USM-207 off and disconnect the test equipment.	*s.* None.
			t Connect coaxial cables 2A24W10 and 2A24W13 to 2A13J3 and 2A14J3.	*t.* None.
			u. Set both APC switches on combiner 2A16 to ON.	*u.* None.

Step No.	Control settings: Test equipment	Control settings: Equipment order test	Test procedure	Performance standard
			v. Set the controls on frequency synthesizer 2A21 to frequency recorded in step *a.*	*v.* None.

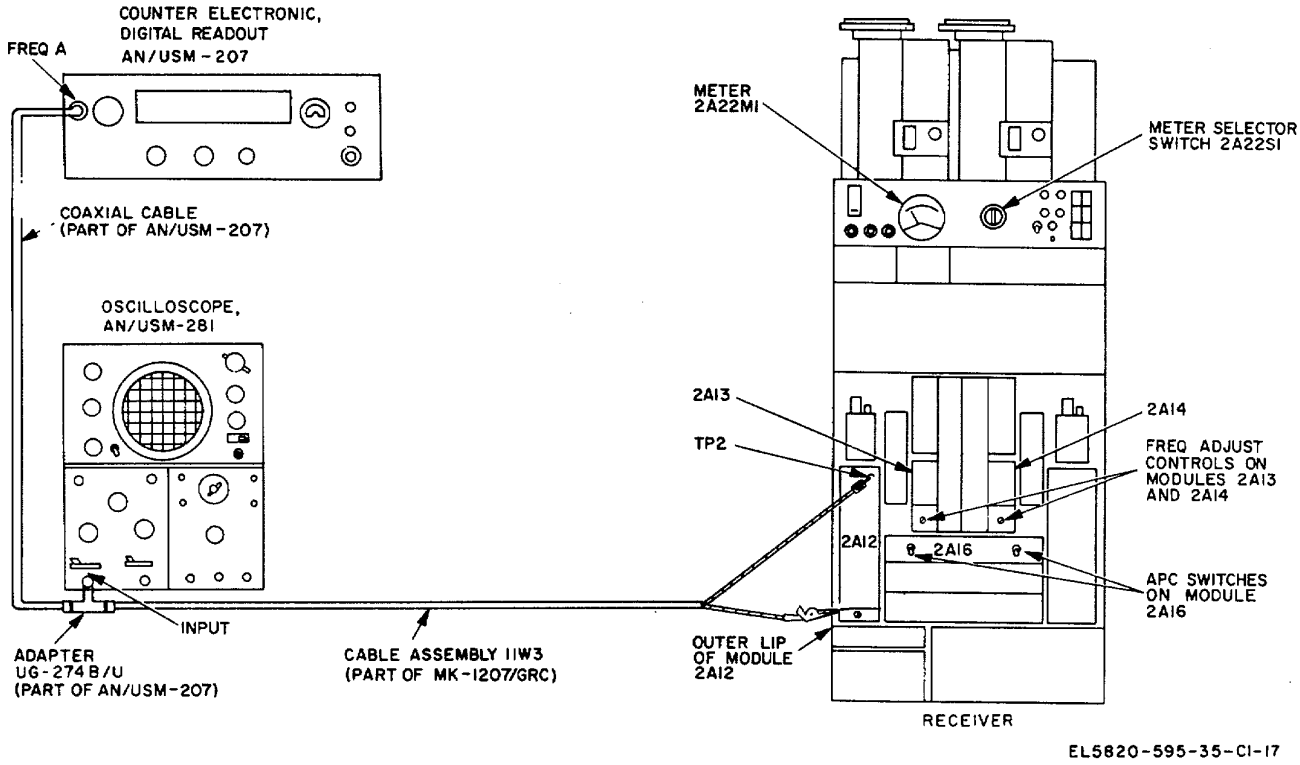


Figure 4-2. Receiver lock and capture test set up.

4-9. Receiver Lock and Capture Test

a. General. The receiver lock and capture test is used to check the receiver APC circuit and determine when corrective action must be taken. The test must be performed at the periodic maintenance interval specified in paragraph 2-4 and when indicated in the receiver troubleshooting chart (para 4-3*d*). The performance standards listed in the chart (*e* below) indicate the minimum requirements for equipment maintained in the field and the corrective action to be taken if the performance standards are not met. This test will interrupt radio communications.

b. Test Equipment Required.

(1) Counter Electronic, Digital Readout AN/USM-207.

(2) Oscilloscope, AN/USM-281.

(3) Cable Assembly 11W3 (part of MK-1207/U GRC).

c. Test and Conditions. This procedure assumes that the radio set is turned on and connected for normal operation at the start of the test. Prior to performing the test, the maintenance man should notify the Multiplexer TD-204/U and distant radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted. Additional test connections and conditions are given in the procedural steps below.

(1) Record the transmitter and receiver operating frequencies.

(2) On the transmitter, set the controls on frequency synthesizer 1A14 and 4.4-5.0 GHz bandpass filter 1FL3 to 4800 MHz.

(3) On the receiver, set the controls on frequency synthesizer 2A21, preselectors 2FL4 and 2FL5, post selectors 2FL6 and 2FL7, and local oscillator filters 2FL8 and 2FL9 to 4700 MHz.

(4) Set the ON/OFF switch on transmitter 100 MHz radio frequency oscillator 1A2 to ON.

(5) Set the meter switch on the transmitter radio test set meter panel to OSC LEVEL.

6) Adjust the LEVEL ADJ control on transmitter 100 MHz radio frequency oscillator 1A2 for a radio test set meter indication of 12 or 24 CHAN depending on the number of pcm channels being used.

(7) Turn the RCVR CHAN A and RCVR CHAN B switches on the transmitter radio test set to T + 20.

d. Initial Test Equipment Turn-on. Turn on the AN USM-207 and AN/USM-281 and allow a 15 minute warmup period.

e. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN /USM-207 SENSITIVITY: 1V FUNCTION: FREQ Time base switch to GATE TIME (SEC^{-1}) -1 DISPLAY control to desired display time AN USM 281 DISPLAY: A VOLTS/CM: .02 GND/AC/DC: AC TIME/CM: 2 MS SWEEP MODE: AUTO EXT 10/EXT/INT/ LINE: INT	N/A----------	*a.* Connect the equipment as shown in figure 4-2.	*a.* None.
			b. Set both APC switches on combiner 2A16 to OFF.	*b.* None.
			c. Rotate the FREQ ADJUST control on module 2A13 clockwise until frequency readout on AN/USM-207 is 500 Hz. If a 500 Hz frequency readout cannot be obtained by adjustment of 2A13 FREQ ADJUST control, rotate the FREQ ADJUST control on module 2A14 counterclockwise until frequency readout on AN/USM-207 is 500 Hz.	*c.* None.
			d. Observe that a sine wave is displayed on AN/USM-281.	*d.* None.
			e. Set both APC switches on combiner 2A16 to ON, and then observe line, display on AN /USM-281.	e. AN/USM-281 display should be a straight indicating that receiver is in lock. If display on AN/USM-281 is not a straight line, refer to the receiver troubleshooting chart (item 47, para 4-3*d*) for corrective action.
			f. Set both APC switches on combiner 2A16 to OFF.	*f.* None.
			g. Turn meter selector switch 2A22S1 to VCO FREQ DIFF.	*g.* None.
			h. Rotate the FREQ ADJUST control on module 2A13 as required to obtain a minimum indication on receiver meter 2A22M1.	*h.* None.
			i. Repeat steps c through h above substituting "2A14" for "2A13."	*i.* Same as e above.
			j. Turn off and disconnect the test equipment.	*j.* None.
			k. Set both APC switches on combiner 2A16 to ON.	*k.* None.
			l. On the transmitter, set ON/OFF switch on 100 MHz radio frequency oscillator 1A2 to OFF.	*l.* None.
			m. Reset the frequency controls on the transmitter and receiver to the frequency settings recorded in step (1) of subParagraph c above.	*m.* None.

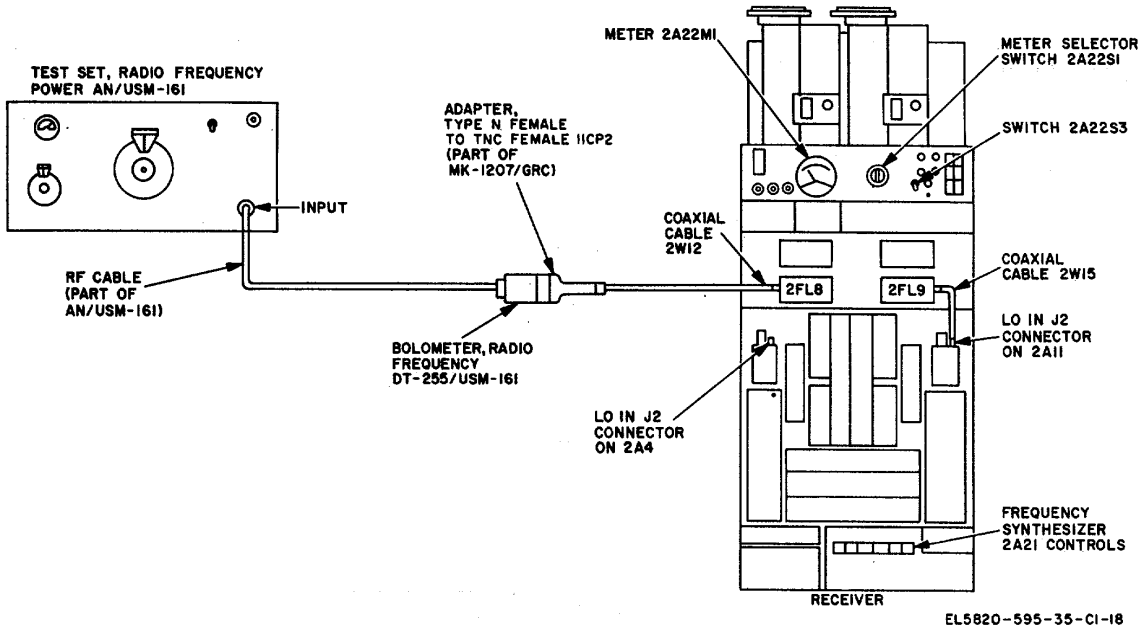


Figure 4-3. Receiver local oscillator chain output power and metering test set up.

4-10. Receiver Local Oscillator Chain Output Power and Metering Test

a. General. The receiver local oscillator chain output power and metering test is used to determine the rf output level of the receiver's local oscillator chain metering circuits. The test must be performed at the periodic maintenance intervals specified in Paragraph 2-4 and when indicated in the receiver troubleshooting chart (para 4-3d). The performance standards listed in the chart (e below) indicate the minimum requirements for equipment maintained in the field and the corrective action to -be taken if the performance standards are not met. This test will interrupt receive radio communications.

b. Test Equipment Required.

(1) Test Set, Radio Frequency Power AN/ USM-161.

(2) Adapter, type N female to TNC female 11CP2 (part of MK-1207/GRC).

c. Test Connections and Conditions. This procedure assumes that the radio set is turned on and connected for normal operation at the start of the test. Prior to performing the test, the maintenance man should. notify the Multipexer TD-204/ and distant radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

d. Initial Test Equipment Turn-on and Calibration. Turn on the AN/USM-161 and allow a 30 minute warmup period. After the warmup period, calibrate the AN/USM-161 using the procedures given in TM 11-6625-498-12.

e. Procedure.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	AN/USM-41 BIAS-READ: READ POWER RANGE: 10 MW-10 DBM POWER indicator dial to 1.0 on outermost scale COMP ATTENUATOR dial to 0.	N/A -----.-----	*a.* Record the receiver operating. frequency setting on frequency synthesizer 2A21 controls.	*a.* None.
			b. Set the controls on frequency synthesizer 2A21 and local oscillator filter 2FL8 to 4400.0 MHz. -	*b.* None.
			c. Disconnect coaxial cable 2W12 from the LO IN J2 connector on amplifier-mixer 2A4.	*c.* None.

Step No.	Test equipment	Control settings Equipment under test	Test procedure	Performance standard
			d. Connect the equipment as shown in figure 4-3.	*d.* None.
			e. Adjust the POWER indicator dial on AN/USM-161 until a null is obtained on the AN/USM-161 NULL INDICATOR meter. Multiply the indication on outermost scale of AN/USM-161 POWER indicator dial by 10. Record.	*e.* Receiver channel A local oscillator output power should be 0.5 milliwatts minimum. If it is not, refer to the receiver troubleshooting chart (item 48, para 4-3d) for corrective action.
			f. Repeat steps b and e above for the following receiver frequencies: 4500.0 MHz, 4600.0 MHz, 4700.0 MHz, 4800.0 MHz, 4900.0 MHz, and 5000.0 MHz.	*f.* Same as e above.
2	AN/USM-161 BIAS-READ: READ POWER RANGE: 1.0 MW 0 DBM POWER indicator dial to .25 on outermost scale COMP ATTENUATOR dial to 0	N/A----------	*a.* Set the controls on frequency synthesizer 2A21 to 4700.0 MHz.	*a.* None.
			b. While observing the NULL INDICATOR meter on AN/USM-161, slowly turn the PUSH TO TURN knob on local oscillator filter 2FL8 toward 4700 MHz until a null indication is obtained on the AN/USM-161 NULL INDICATOR meter.	*b.* None.
			c. Disconnect coaxial cable 2W12 from the adapter on the test equipment and reconnect it to the LO IN J2 connector on amplifier-mixer 2A4.	*c.* None.
			d. Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to A. output power metering circuit (para 4-34).	*d.* Indication on meter 2A22M1 should be 30. If it is not, calibrate the receiver local oscillator
3	Same as 1 above --------	N/A --------	*a.* Set the controls on frequency synthesizer 2A21 and local oscillator filter 2FL9 to 4400.0 MHz.	*a.* None.
			b. Disconnect coaxial cable 2W15 from the LO IN J2 connector on amplifier-mixer 2All.	*b.* None.
			c. Connect coaxial cable 2W15 to the adapter on the test equipment.	*c.* None.
			d. Adjust the POWER indicator dial on AN/USM-161 until a null is obtained on the AN/USM-161 NULL INDICATOR meter. Multiply the indication on the outermost scale of AN/USM-161 POWER indicator dial by 10. Record.	*d.* Receiver channel B local oscillator output power should be 0.5 milliwatts minimum. If it is not, refer to the receiver troubleshooting chart (item 49, para 4--3d) for corrective action.
			e. Repeat steps a and d above for the following receiver frequencies: 4500.0 MHz, 4600.0 MHz, 4700.0 MHz, 4800.0 MHz, 4900.0 MHz, and 5000.0 MHz.	e. Same as d above.

Step No.	Test equipment	Control settings Equipment under test	Test procedure	Performance standard
4	Same as 2 above	N--------	a. Set the controls on frequency synthesizer 2A21 to 4700.0 MHz.	a. None.
			b. While observing the NULL INDICATOR meter on AN/USM-161, slowly turn the PUSH TO TURN knob on local oscillator filter 2FL9 toward 4700 MHz until a null indication is obtained on the AN/USM-161 NULL INDICATOR meter.	b. None.
			c. Disconnect coaxial cable 2W15 from the adapter on the test equipment and reconnect it to the LO IN J2 connector on amplifier-mixer 2All.	c. None.
			d. Turn meter selector switch 2A22S1 to LOCAL OSC POWER and set switch 2A22S3 to B.	d. Same as 2d above.
			e. Turn the AN/USM-161 off and disconnect the test equipment.	e. None.
5	N/A----------	N/A----------	a. Set the controls on local oscillator filter 2FL8 and 2FL9 to 4700 MHz.	a. None.
			b. Alternately set meter selector switch 2A22S1 to the following positions and record 2A22M1 indication for each position: AMPL-MULT, 2ND MULT, MULT OSC A, MULT OSC B, FREQ MIXER CURRENT (3RD MULT A1, FREQ MIXER CURRENT (3RD MULT) A2, FREQ MIXER CURRENT (3RD MULT) B1, and FREQ MIXER CURRENT (3RD MULT) B2.	b. Indication on meter 2A22M1 should be 100 for each meter position checked. If it is not, calibrate the receiver local oscillator chain metering circuits (para 4-35) that are not indieating 100 on meter 2A22M1.
			c. Set the controls on frequency synthesizer 2A21, local oscillator filter 2FL8, and local oscillator filter 2PL9 to the receiver operating frequency recorded in step 1*a* above.	c. None.

Section II. RECEIVER REPAIRS

4-11. Scope of Receiver Repairs

a. The sequence of events listed below should be followed when replacing any part in the receiver to minimize potential personnel- hazards and optimize restoring the radio- set to an operational state.

(1) Deenergize radio set.

(2) Part replacement.

(3) Energize radio set.

(4) Performance check.

(5) Confirm radio set operational status.

b. Equipment malfunctions are generally corrected by replacing the known defective item with its equivalent new part. Part replacement,

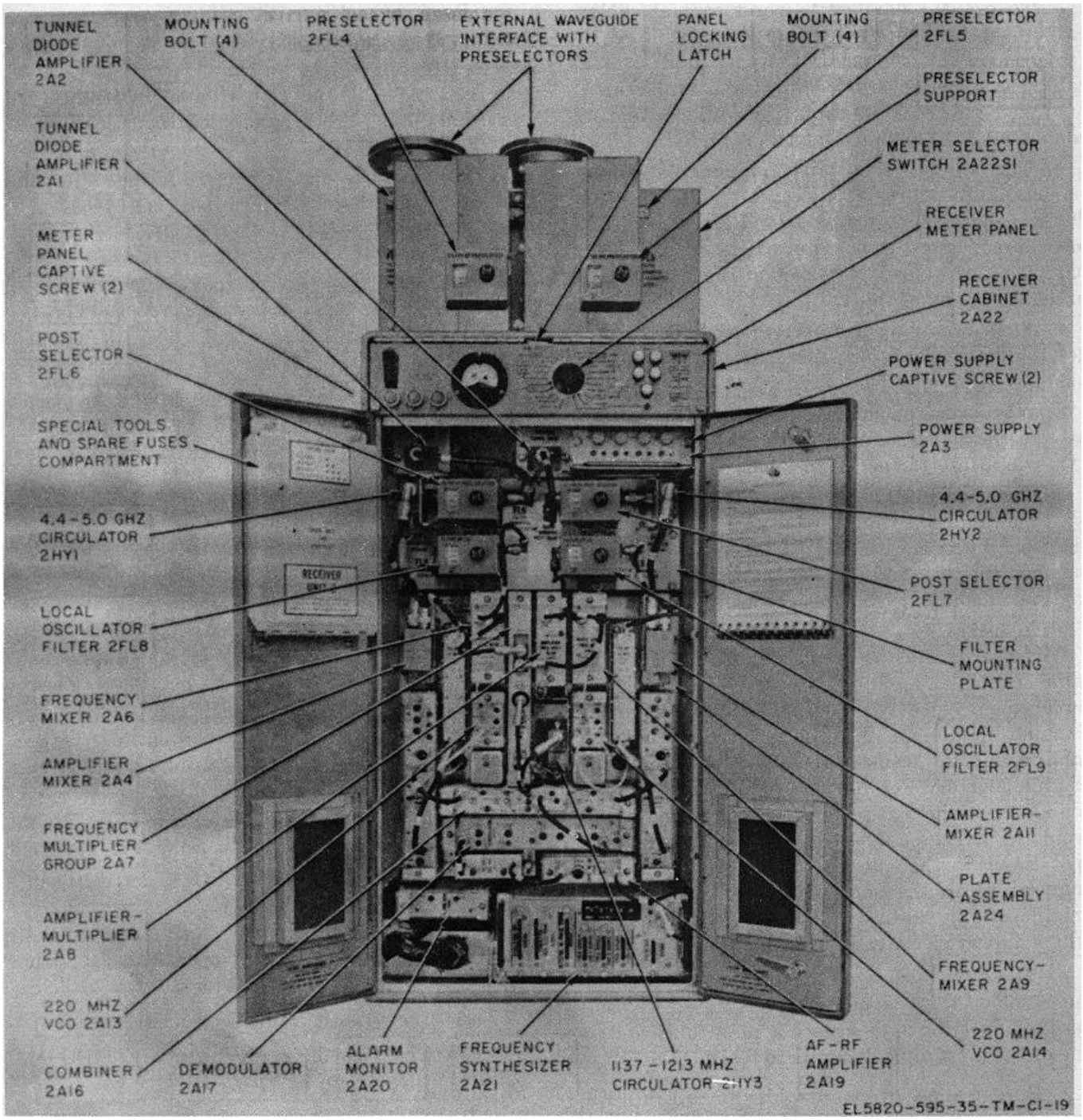


Figure 4-4. Receiver, front view with cabinet doors' open, parts location.

however, does not assure the operational integrity of the radio set and must include performing an operational check. The operational check will confirm correction of the, equipment malfunction prior to reestablishing the radio sets operational status.

c. Procedures for deenergizing the radio set are provided in Paragraph 3-12. Detailed procedure for specific part removal are provided in Paragraph 4-13 through 4-30. When replacing any part, specific precautions and practices should be observed and are itemized in Paragraph 4-12. Procedures for energizing the radio set are provided in Paragraph 3-13.

4-12. Parts Replacement Techniques

The following precautions apply when removing, replacing, or repairing parts in the receiver. 7

a. To prevent damage to rigid coaxial cables, care must be exercised during the removal or replacement of components with rigid coaxial cables. Instructions for removal and replacement of the rigid coaxial cable with their mating connectors are provided in Paragraph 3-14.

b. Tag all hardware and components during removal procedures for correct identification during replacement procedures. Before a part is unsoldered, note the position of the leads. If the part has several leads, tag each of the leads before unsoldering any of them.

c. When removing a defective part, be careful not to damage leads or other parts by pulling or pushing them out of the way.

d. Whenever replacing a part, install the new part in the same position as the original. Use an exact duplicate whenever possible.

e. Use a pencil-type soldering iron with a 25watt maximum heating capacity. If the iron must be used with ac, use an isolating transformer between the iron and ac line. Do not use a soldering gun; damaging voltages can be induced in the equipment parts.

f. If wiring must be replaced, use leads of the same length and gauge if possible. Do not use replacement wire with a higher gauge number (smaller diameter). With the exception of harness cabling, run the leads in the same manner as the original wiring. For harness cabling cut the old conductor as short as possible without removing it from the harness. Dress the new conductor and spot tie it to the outside of the harness. Make connections to the same terminals used in the original wiring, even where there are alternatives which appear electrically equivalent.

g. Make well-soldered connections, using no more solder than is necessary. A carelessly soldered connection may create a new fault and is one of the most difficult faults to find.

h. Do not allow drops of solder to fall into the unit. Do not allow a soldering iron to come into contact with insulation or parts that might be injured by excessive heat.

i. Do not disturb the setting of any uncalibrated control without predetermining its proper setting prior to reenergizing the radio set.

4-13. Replacement of Parts on Receiver Meter Panel

Prior to removing and replacing parts on the receiver meter panel, deenergize the radio set (para 3-12).

a. Removal of Meter 2A22M1.

(1) Loosen the two meter panel captive screws to release meter panel from the receiver cabinet and lock the meter panel in its upward position using the panel locking latch (TM 11-5820-595-12).

(2) Remove the two self-locking nuts: and washers from the meter terminals (fig. 4-5).

(3) Remove and tag the leads from the meter terminals.

(4) While holding the meter in place remove the three self-locking nuts, washers and screws securing meter to the meter panel. Remove meter from the meter panel.

(5) Short the removed meter terminals with several turns of bus wire, to protect the meter movement, until the shorting bar of the new meter can be used.

b. Replacement of Meter 2A22M1.

(1) Place the new meter in position on the meter panel and use the hardware removed in a (4) to secure the new meter 2A22M1 to the meter panel.

(2) Remove the two self-locking juts, washers, and shorting bar from the new meter terminals. (3) Replace the tagged wires on their respective meter terminals and fasten lugs to terminals with hardware removed in step *a*(2).

(4) Replace the bus wire used to short the old meter terminals with the shorting bar removed from the new meter fasten in place with its terminal hardware.

(5) Release the meter panel from upright position and secure it into operational position with the two meter panel captive screws.

(6) Energize the radio set (para 3-13).

(7) Energize the radio set (para 3-13) and calibrate the new meter (para 4-32).

c. Removal of Indicator Assembly 2A22XDS3, XDS7, and XDS11 (fig. 4-5). Follow the procedures as covered in Paragraph 3-15*c*(1) through (7).

d. Replacement of Indicator Light Assembly 2A22XDS3, XDS7 and XDS11 (fig. 4-5).

(1) Follow the procedures as covered in Paragraph 3-15*a* (1) through (11).

(2) Check that the replacement indicator light assembly is lighted. Provided in the chart below are the normal color indications for each indicator.

Name of Indicator	Color Lighted
CARR (IF) A	Green
CARR (IF) B	Green
VCO LOCK	Green
SPARE	Green
SYNTH LOCK	Green
TRAF	Green

e. Replacement of Potentiometers 2A22R1 through 2A22R11 (fig. 4-5). If any of the potentiometers 2A22R1 through R11 located on the receiver meter panel are to be replaced: first deenergize the radio set (para 3-12), replace the defective potentiometer, energize the radio set (para 3-13), and perform the required calibration indicated in the chart below.

Potentiometer	Calibration Procedure
2A22R1 through 2A22R8	Calibration of receiver local oscillator chain metering circuits (para 4-35).
2A22R9 and 2A22R10	Calibration of receiver local oscillator output power metering circuits (para 4-34.
2A22R11	Calibration of receiver traffic metering circuit (para 4-33).

f. Removal of Meter Selector Switch 2A22S1 (figs. 4-5 and 8-59).

(1) Loosen, but do not remove, two allen-head setscrews securing the selector knob to meter selector switch 2A22S1 shaft and remove the knob from selector switch shaft.

(2) Loosen the two meter panel captive screws and swing the meter panel upward and lock it in an upright position using the panel locking latch.

NOTE

When unsoldering leads to the selector switch, remove leads from the top switch deck first. Bend the removed leads out of the way to provide access to lower switch deck and prevent damage to wire insulation when unsoldering leads to the lower switch deck.

(3) Unsolder, remove and tag each lead routed from a cable harness or piece part on the meter panel to the terminals on meter selector switch 2A22A1 (fig. 8-59). Do not remove the jumper leads between terminals.

(4) Release the meter panel from the upright position and rotate it downward until it rests against the receiver cabinet.

(5) Remove hex nut and starwasher securing meter selector switch 2A22S1 to meter panel and remove selector switch from the panel.

g. Replacement of Meter Selector Switch 2A22S1 (figs. 4-4, 4-5 and 8-59).

(1) Place replacement meter selector switch along side the removed meter selector switch. Prepare jumper leads for the lower and upper meter selector switch decks using the removed switch as a guide and solder the prepared jumper leads in their identical positions on the replacement meter selector switch.

(2) Mount replacement meter selector switch on meter panel aligning guide pin with guide hole on meter panel.

NOTE

Support replacement meter selector switch while releasing and lowering meter panel from its upright position.

(3) Secure meter selector switch to meter panel using starwasher and hex nut removed in step*f*(5).

(4) Lock meter panel in an upward position with meter panel locking. latch.

NOTE

When soldering leads to the meter selector switch, start reconnecting leads to the lower deck of meter selector switch first.

(5) Reconnect and solder the leads removed in step f(3) to their respective terminals on the meter selector switch.

(6) Release meter panel locking latch and rotate meter panel. downward until resting against receiver cabinet.

(7) Replace and secure the knob removed in step f(1).

(8) Rotate the meter selector switch and check that replace leads do not interfere with the switch movement.

(9) Secure the meter panel to the receiver cabinet with the two meter panel captive screws.

(10) Energize the radio set (para 3-13) and perform the receiver metering checks (TM 11-5820-595-12).

4-14. Replacement of Power Supply Chassis 2A3A5 (figs. 4-4 and 4-6)

a. Removal.

(1) Deenergize the radio set (para 3-12).

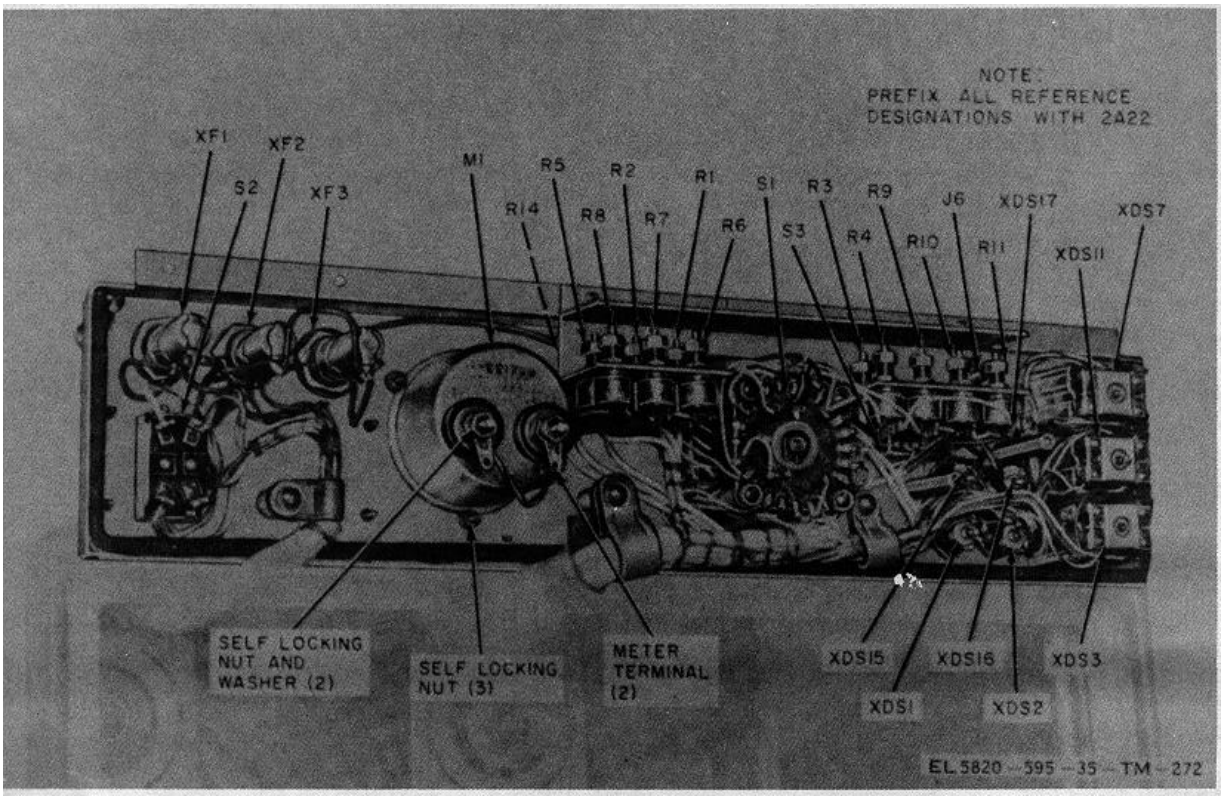


Figure 4-5. Receiver meter panel, rear view, parts location.

(2) Loosen the two meter panel captive screws and lock the meter panel in its upright position using the panel locking latch.

(3) To release power supply 2A3 from the receiver cabinet, loosen the two power supply 2A3 captive screws by alternately unscrewing each captive screw one or two turns at a time to prevent power supply 2A3 from binding against the receiver cabinet walls.

(4) Slide power supply 2A3 out of the receiver cabinet.

(5) Alternately loosen the captive screws on 15 28v regulator 2A3A1 and remove 2A3A1 from the chassis.

(6) Repeat step (5) for 15/28v regulators 2A3A2 and 2A3A4, and 12v regulator 2A3A3.

b. Replacement.

(1) Insert 15/28v regulator 2A3A1 into' replacement power supply chassis 2A3A5 aligning printed wiring board on 2A3A1 with guide rails located on upper and lower portions of power supply chassis. Then slowly push the plug-in component into the power supply chassis until the connectors are mated.

(2) Alternately tighten the two captive screws on 15/28v regulator 2A3A1 to secure the plug-in component to replacement power supply chassis.

(3) Repeat steps (1) and (2) for 15/28v regulators 2A3A2 and 2A3A4, and for 12v regulator 2A3A3. The plug-in components are mounted in power supply chassis 2A3A5 in sequential order 2A3A1, 2A3A2, 2A3A3 and 2A3A4.

(4) Reinstall power supply 2A3 into receiver cabinet so that guide pins and connectors are mated.

(5) Alternately tighten the two captive screws on a power supply 2A3 a few turns each until the power supply is securely fastened': to" receiver cabinet.

(6) Release the meter panel from its upright position and secure it to the receiver cabinet with the two meter panel captive screws.

(7) Energize the radio set (para 3-13).

4-15. Replacement of Parts in Power Supply Chassis 2A3A5 (figs. 4-6 and 4-7)

To replace any part in power supply chassis 2A3A5: remove power supply 2A3 from receiver cabinet (para 4-14a) and refer to the following applicable replacement procedure for the part to be replaced. After the part has been replaced, replace power supply 2A3 in receiver cabinet (para 4-14b). Parts located on terminal board 2A3A5TB1 (fig. 4-7) are removed using standard soldering techniques (para 4-12).

a. Removal of Power Supply Chassis Mounted Module Connectors 2A3A5XA1 through 2A3A5XA4 (fig. 4-6).

(1) remove the four screws and associated washers securing rear shield to power supply chassis 2A3A5.

(2) Tag and unsolder wires connected to module connector terminals of the connector to be replaced.

(3) Remove the two screws and nuts securing module connector to power supply chassis and remove the connector.

b. Replacement of Power Supply Chassis Mounted Module Connectors A3A5XA1 through 2A3A5XA4 (fig. 4-6).

(1) Mount replacement module connector using the two screws and nuts removed in step*a*(3). Do not tighten the two screws and nuts.

(2) Insert voltage regulator module used with replaced connector into power supply chassis and seat its connector into replacement module connector. Secure the module with its two captive screws.

(3) Tighten the two screws and nuts securing module connector to power supply chassis.

(4) Solder wires removed in step a(2) to module connector terminals.

(5) Mount and secure the rear shield to power supply chassis using the four screws and associated washers removed in step *a* (1).

c.. Removal of Lamp Sockets 2A3A5XDS1 through 2A 3A5XDS4 (fig. 4-6).

(1) Turn power supply chassis upside down and remove the 10 screws securing bottom access plate to power supply chassis.

(2) Tag and unsolder wires connected to lamp socket to be replaced.

(3) Force press fitted lamp socket through its mounting hole in power supply chassis by pressing terminal end toward mounting hole and ,remove lamp socket from power supply chassis.

d. Replacement of 4ammp Sockets 2A3A5XDS1. through 2A3A5XDS4 (fig. 4-6).

(1) Replace lamp socket by forcing terminal end of press fitted lamp socket through front of mounting hole in power supply chassis by pressing lamp end until mounted snugly against power supply chassis frame.

(2) Solder wires removed in step *c*(2) to lamp socket terminals.

(3) Mount and secure the bottom access plate to power supply chassis using the 10 screws removed in step *c*(1).

e. Removal and Replacement of Mounted Chassis Connectors 2A3A5P1 (fig. 4-6).

(1) Turn power supply chassis upside down and remove the 10 screws securing bottom access plate to power supply chassis.

(2) If a connector contact requires replacement refer to the procedures provided in Paragraph 428 for removal and replacement of connector contacts and proceed to step (7).

(3) If the connector requires a replacement remove the two screws and nuts securing connector to power supply chassis.

(4) Remove connector from mounting hole and insert replacement connector in mounting hole. Tighten replacement connector in position using the two screws and nuts removed in step (3).

(5) Remove a wired connector contact from the removed connector and install in the identical replaced connector contact location. Refer to Paragraph 4-28 for connector pin removal and replacement.

(6) Repeat step (5) for each wired connector contact until transfer of all connector contacts are completed.

(7) Mount bottom access plate to power supply chassis using the 10 screws removed in step (1).

4-16. Replacement of Blower Motor 2A22B1 (fig. 4-8) TM 11-5820-595-35

WARNING

115 vac is routed to blower motor 2A22B1. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector 2A22J5 (fig. 4-9) before performing this procedure.

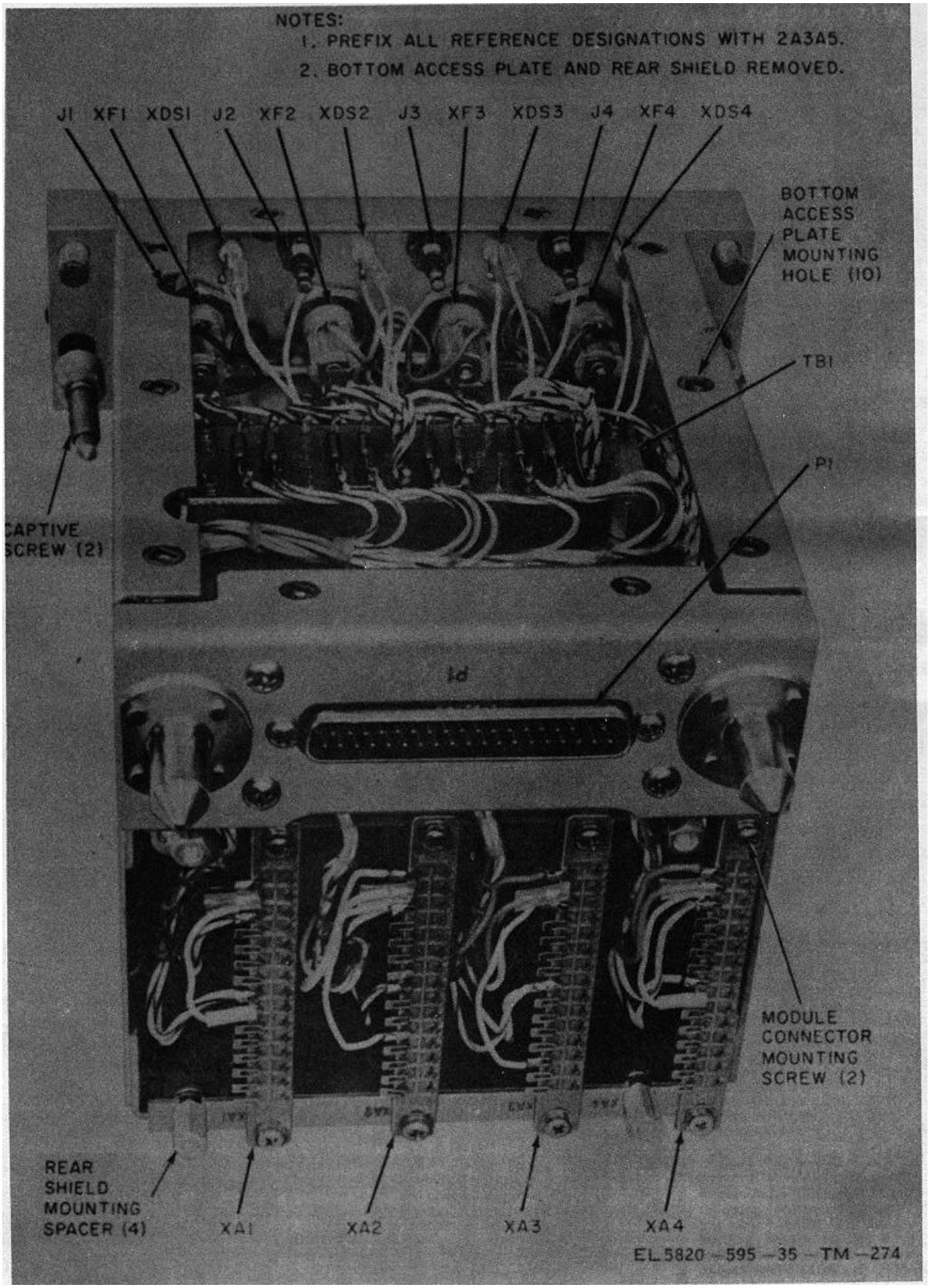


Figure 4-6. Receiver power supply chassis 2A8A5, top rearview, parts location.

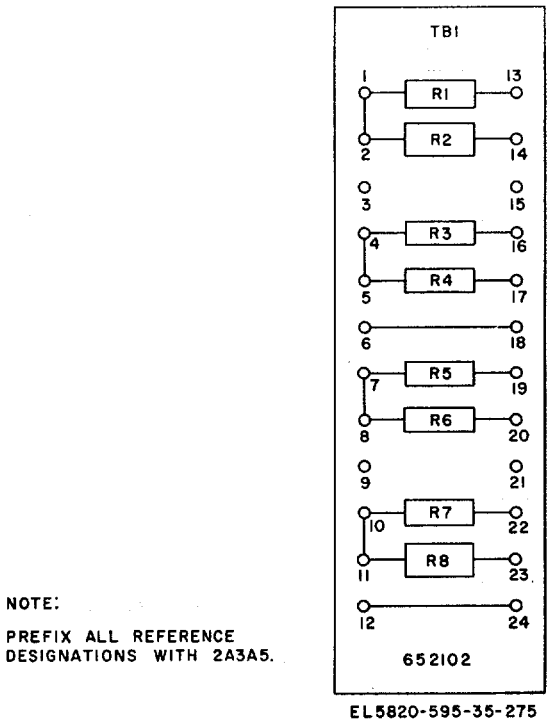


Figure 4-7. Receiver power supply chassis terminal board 2A3A5TB1, top view, parts location.

a. Removal.

(1) Remove power supply 2A3 from receiver cabinet by performing steps (1) through (4) of Paragraph 4-14*a*.

(2) Remove the four thumb screws (refer to fig. 3-11) securing air filter to top of receiver cabinet and remove air filter.

(3) While supporting blower motor 2A22B1 from inside of receiver cabinet, loosen the four synclamp screws (fig. 4-9) securing blower motor 2A22B1 to receiver cabinet. Each screw has a synclamp nut which clamps a blower motor housing to the top of receiver cabinet (fig. 3-11).

(4) Tilt blower motor housing upward and slide past the synclamps, then lower blower motor 2A22B1 into receiver cabinet.

(5) Tag wires connected to blower motor 2A22B1 terminals (refer to fig. 3-11). Remove three screws which secure the wire lugs to blower motor 2A22B1 terminals. The lugs are soldered to the tagged wires.

(6) Remove blower motor 2A22B1 from receiver cabinet.

b. Replacement.

(1) Check that AIR FLOW arrow (printed on side of replacement blower motor 2A22B1) is pointing upward, and insert replacement blower motor 2A22B1 into upper right section of receiver cabinet. Connect wire lugs to blower motor 2A22B1 terminals using three screws removed in step *a*(5).

(2) Position blower motor 2A22B1 against top wall of receiver cabinet between the four synclamps. Align the synclamps with blower motor 2A22 B1 as shown in figure 3-11.

(3) Secure blower motor 2A22B1 to receiver cabinet by tightening the four screws connected to the synclamps.

(4) Mount air filter to top of receiver cabinet and tighten in place using the four screws removed in step a(2).

(5) Replace power supply 2A3 into receiver cabinet-by performing steps (4) through (6) of Paragraph 4-14b.

(6) Energize the radio set (para 3-13) and check blower motor 2A22B1 operation by placing a hand over the air filter on top of the receiver cabinet to feel if air is being blown out of the receiver cabinet through the air filter.

4-17. Replacement of Capacitor 2A22C1 (fig. 4-8)

WARNING

115 vac is routed to capacitor 2A22C1. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector 2A22J5 (fig. 4-9) before performing this procedure.

a. Removal.

(1) Remove power supply 2A3 from receiver cabinet by performing steps (1) through (4) of Paragraph 4-14*a*.

(2) Loosen and remove the self-locking nut, washer and cable clamp (fig. 4-8) securing the leads connected to capacitor 2A22C1.

(3) Remove the two nuts securing capacitor 2A22C1 mounting bracket to rear wall of receiver cabinet.

(4) Remove mounting bracket and carefully place capacitor 2A22C1 in power supply 2A3 enclosure.

(5) Tag and unsolder the two wires connected to capacitor 2A22C1 terminals. Remove the capacitor.

b. Replacement

(1) Place replacement capacitor 2A22C1 into receiver cabinet power supply enclosure and solder the two wires removed in step *a*(5) to capacitor 2A22C1.

(2) Insert capacitor mounting bracket over capacitor 2A22C1, and place the capacitor mount

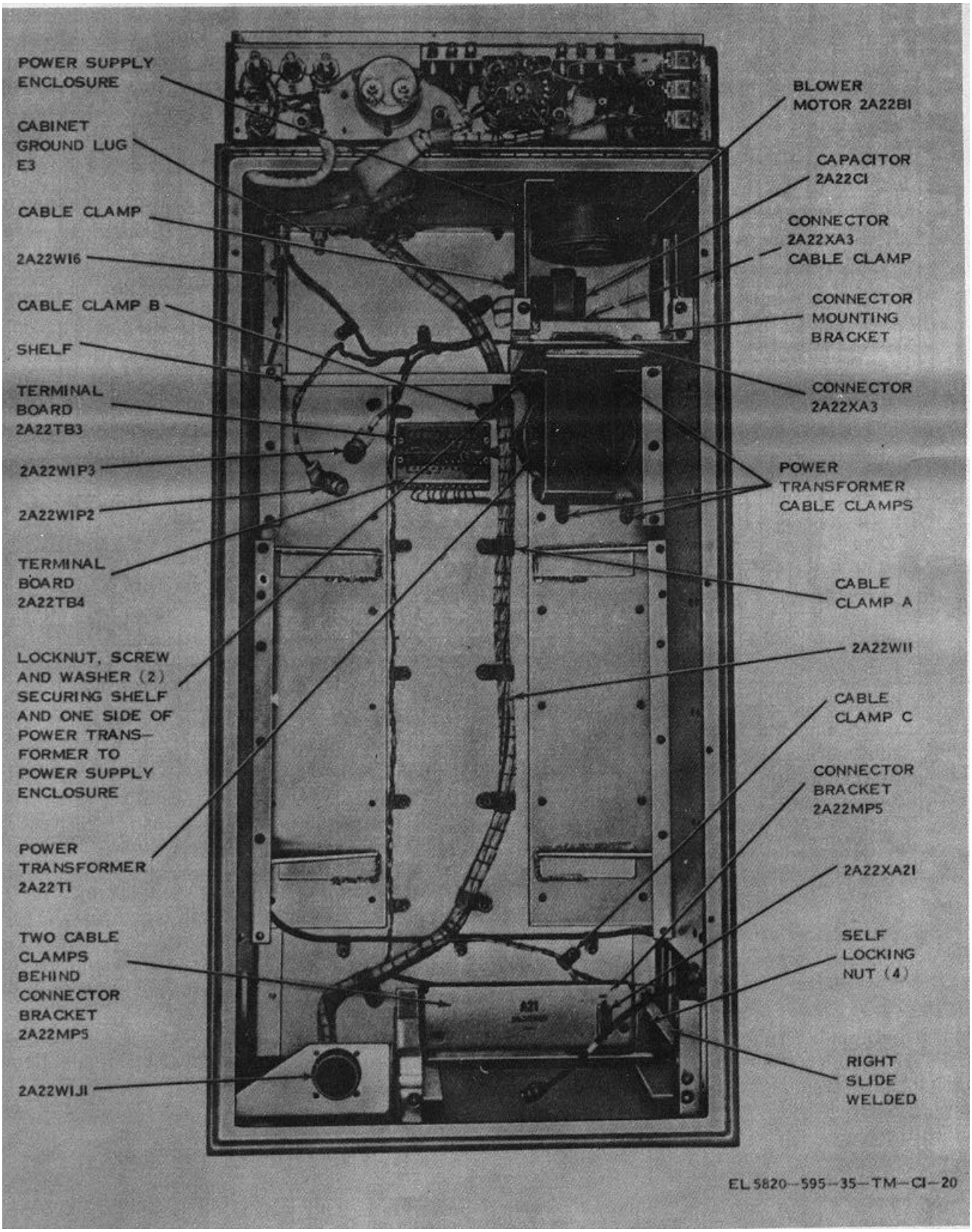


Figure 4-8. Receiver cabinet 2A122, front view, partially disassembled, parts location.

bracket on the threaded studs on rear wall of receiver cabinet (fig. 4-8).

(3) Replace and tighten the two nuts securing capacitor mounting bracket to rear wall of receiver cabinet. Replace and secure cable clamp removed in step a(2).

(4) Replace power supply 2A3 into receiver cabinet by performing steps (4) through (6) of paragraph 4-14b.

(5) Energize the radio set (para 3-13) and check operation of blower motor 2A22B1 by placing a hand over the air filter on top of the receiver cabinet to feel if air is being blown out of receiver cabinet through the air filter.

4-18. Replacement of Low Pass Filter 2A22FL1, Input Filters 2A22FL2 and 2A22FL3

(figs. 4-4, 4-9, 4-10 and 4-11).

WARNING

115 vac is applied to the input filters 2A22FL2 and 2A22FL3. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector 2A22J5 (fig. 4-9) before performing this procedure.

a. Removal.

(1) Remove power supply 2A3 from the receiver cabinet by performing steps (1) through 4) of paragraph 4-14a.

NOTE

Remove external waveguide to preselector, 2FL4 and 2FL5, if required, to provide access to parts mounted on top of receiver cabinet and behind preselector support.

(2) Disconnect coaxial cable 2W1 from TDA2A1 output connector 2AIJ2 (fig. 4-10).

CAUTION

Perform steps (3) and (4) by alternately loosening the TDA2A1 mounting bracket four captive screws approximately two turns and then the knurled knob (TDA2A1J1) approximately two turns. Continue to alternate performing steps (3) and (4) until TDA2A1 is released.

(3) Loosen the four captive screws (fig. 4-10) on TDA2A1 mounting bracket releasing TDA2A1 from its mounting bracket.

(4) Release TDA2A1 from preselector 2FL4 by rotating the knurled ring on TDA2A1 input connector J1 clockwise.

(5) Reach behind TDA2A1 and its mounting bracket. Release the power input cable from TDA2A1 POWER connector J3 (TM 11-5820-595-12).

(6) Carefully slide TDA2A1 away from its mounting bracket toward the rear of receiver cabinet. Swing to the right to clear the mounting bracket.

(7) Remove TDA2A1 from the receiver cabinet and set aside for reassembly.

(8) Repeat steps (2) through (7) for TDA2A2. Refer to figure 4-10 for the applicable piece part designation.

(9) Remove the six screws securing the protective cover to the right and left gusset (fig. 4-9). Three screws are located along each gusset sloping edge.

(10) Remove protective cover from receiver cabinet and set aside for reassembly.

(11) Unsolder, tag and remove the wire leads to input filters 2A22FL2 and 2A22FL3, and low pass filter 2A22FL1 (fig. 4-9).

(12) Loosen and remove the six filter mounting plate screws and washers (fig. 4-11) securing the low pass filter mounting plate to the filter bracket.

(13) Remove four screws (fig. 4-9), accessible on top of receiver cabinet and behind preselector support, securing TDA2A1 mounting bracket (fig. 4-10) to top of receiver cabinet. Tag and save all mounting hardware for reassembly.

(14) Loosen and remove the angle mounting hardware (fig. 4-10) securing TDA2A1 mounting bracket to the angle.

(15) Remove and tag TDA2A1 mounting bracket and the angle mounting hardware from the receiver cabinet and save for reassembly.

(16) Repeat steps (13) through (15) for TDA2A2.

(17) Loosen and remove the two elastic stop nuts securing 115 vac cover (fig. 4-11) mounted against the inside top of the receiver cabinet. Remove 115 vac cover from receiver cabinet and save the cover and elastic stop nuts for reassembly. The underside terminals of low pass filter 2A22FL1 and input filters 2A22FL2 and 2A22FL3 are now accessible from inside receiver cabinet.

(18) Unsolder, remove and tag the wire lead from input filter 2A22FL3 and 2A22FL terminals that are accessible from inside receiver cabinet.

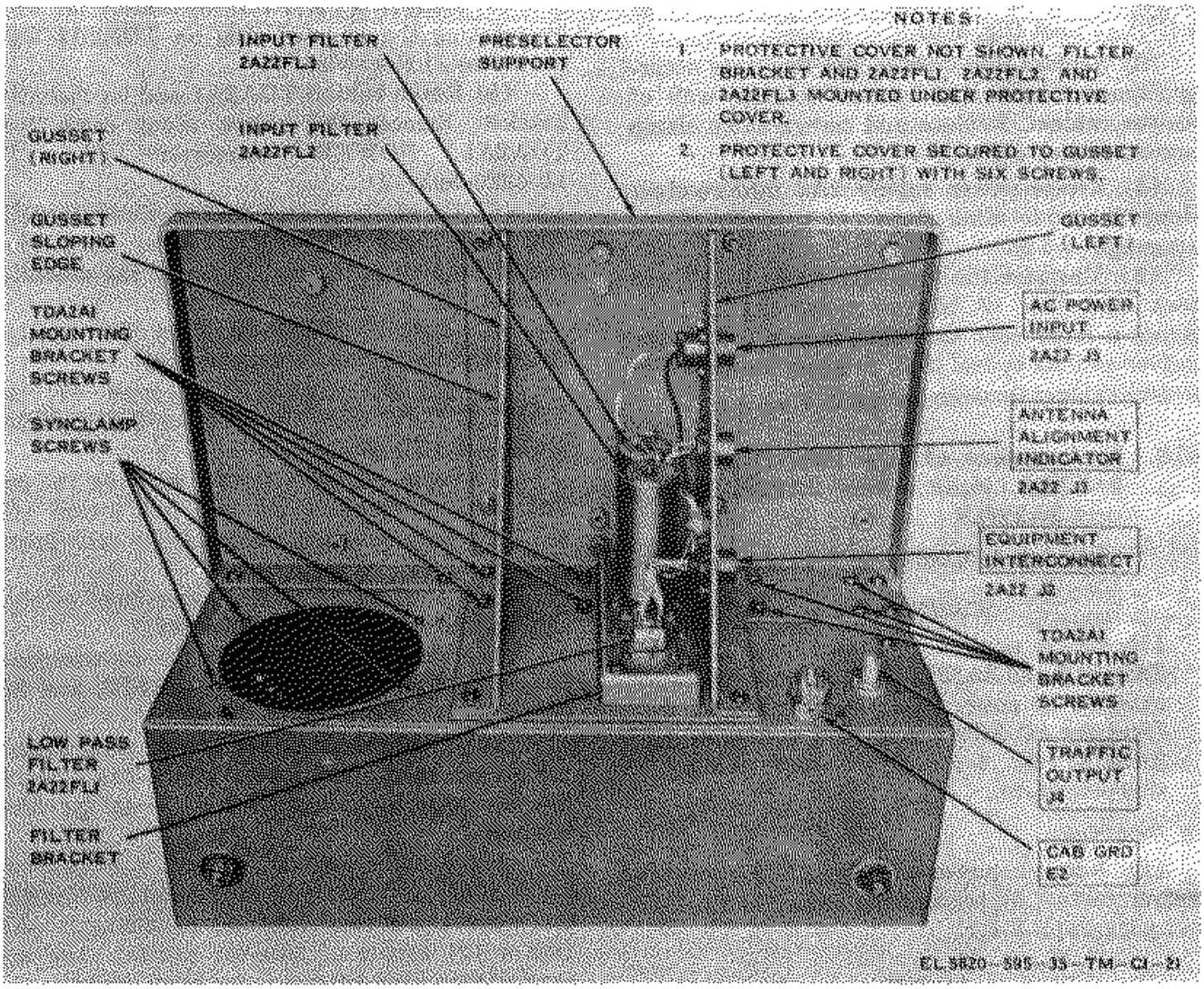


Figure 4-9. Receiver cabinet 2A22, top rear view, partially disassembled, parts location.

(19) Loosen and remove the six mounting screws (fig. 4-11) securing the filter bracket to the top of the receiver cabinet. Save the hardware for reassembly.

(20) Remove the filter bracket with input filters 2A22FL2 and 2A22FL3 mounted on the filter bracket. To separate either filter from the filter bracket, remove the input filter hex nut and lockwasher.

(21) Tag, unsolder and remove the leads from each of the low pass filter 2A22FL1 underside terminals. The terminals are accessible from inside the receiver cabinet.

(22) Remove the filter mounting plate with low pass filter 2A22FL1 from the top of the receiver cabinet.

(23) Loosen and remove the six input filter 2FL1 mounting screws (fig. 4-11) to separate the filter from the mounting plate.

b. Replacement.

(1) Mount and secure replacement low pass filter 2A22FL1 to low pass filter mounting plate using the six screws removed in step a(23) (fig 4-11).

(2) Replace assembled low pass filter 2A22FL1 and its mounting plate on top of receiver cabinet (fig. 4-11).

(3) Resolder the leads removed in step a(21) to 2A22FL1 underside terminals accessible from inside the receiver cabinet.

(4) Proceed to step (6) if input filters 2A22FL2 and 2A22FL3 were not replaced..

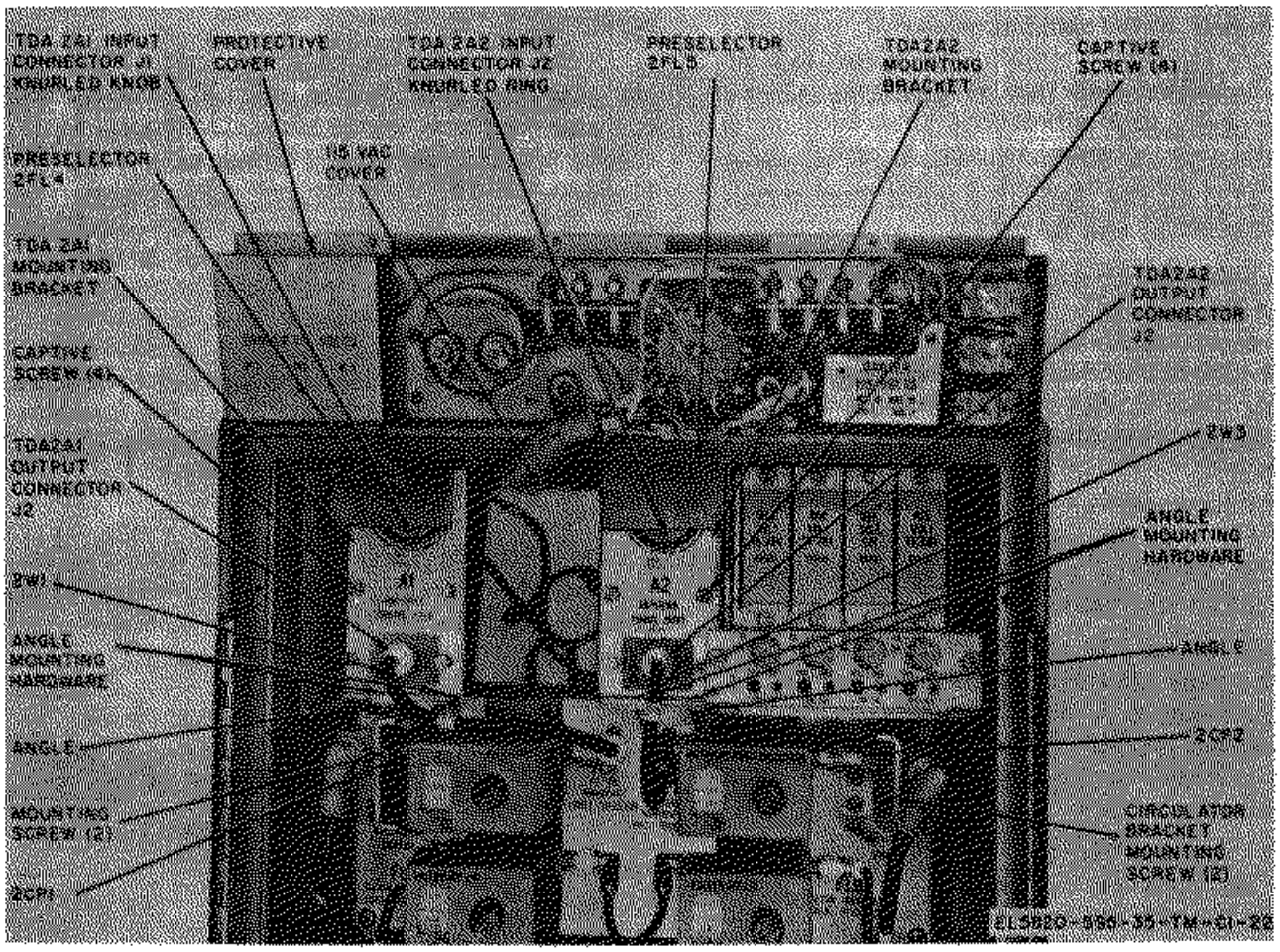


Figure 4-10. Receiver, front view showing upper portion of receiver cabinet 2A22, parts location.

(5) Remove the hex nuts and lockwashers from the replacement input filters 2A22FL3 and 2A22FL2 and secure input filters to filter bracket using the hex nuts and lockwashers (fig. 4-11).

(6) Replace assembled filter bracket with input filters on top of receiver cabinet.

(7) Secure the filter bracket to top of receiver cabinet using the six mounting screws removed in step a(19).

(8) Reconnect and solder the leads removed in step (18) to the respective input filter terminals of 2A22FL3 and 2A22FL2.

(9) Raise (from outside the receiver cabinet) low pass filter 2A22FL1 (fig. 4-11) to rest the low pass filter mounting plate against filter bracket. Align the mounting holes and insert the six filter mounting plate screws removed in step a(12) to secure the low pass filter mounting plate to filter bracket.

(10) Reconnect and solder the leads removed in step a(11) to the respective terminals on low pass filter. 2A22FL1 and input filters 2A22FL2 and 2A22FL3 (fig. 4-9).

(11) Mount 115 vac cover (inside receiver cabinet) on the 115 vac cover mounting studs (fig. 4-11) and secure in place with the elastic' stop a nuts removed in step a(17). Check that the leads (inside the receiver cabinet) to the filter terminals are not crimped or damaged.

(12) Replace TDA2A1 (fig. P10) mounting bracket on the angle and loosely secure in place using the hardware removed in step a(14).

(13) Insert and secure TDA2A1 mounting bracket (fig. 4-9 and 4-10) to the top of the receiver cabinet using the four screws removed in step a(13). These screws are mounted from the top of the cabinet.

(14) Tighten the hardware used in step (12).

(15) Carefully insert TDA2A1 into its mounting bracket (note removal, step a(6)) and reconnect the power input cable to TDA2A1 POWER connector J3 that was removed in step a(5).

(16) Secure TDA2A1 to its mounting bracket and preselector 2FL4 (fig. : 41:) by alternately tightening the four captive screws and knurled' ring (in a counterclockwise rotation) approximately two turns each. Repeat this method until TDA2A1 is secured to its mounting bracket and preselector 2FL4.

(17) Repeat steps (12) through (16) for TDA2A2.

(18) Reconnect coaxial cables 2W1 and 2W3 (fig. 4-10) to TDA output connectors 2A1J2 and 2A2J2 respectively.

(19) Replace power supply 2A3 in receiver cabinet by performing steps (4) through (7) of paragraph 4-: 14b.

(20) Energize the radio set (para 3-13). If low pass filter 2A22FL1 is replaced, perform the operator daily and weekly preventive maintenance checks and services provided in TM 11-5820-595-12.

4-19. Replacement of Preselector 2FL4 or 2FL5
(figs. 44 and 4-10)

The following procedures cover preselector 2FL4 in detail. Using substituted reference designations, the same procedures are applicable to preselector 2FL5.

a. Removal.

(1) Remove power supply 2A3 from receiver cabinet by performing steps a(1l) through a(4) of paragraph 4-14 when replacing 2FL5 only.

NOTE

Remove the necessary external waveguide sections routed to preselector to permit removal of preselector 2FL4.

(2) Disconnect coaxial cable 2W1 (fig. 4-10) from TDA2A1 output connector J2.

CAUTION

Perform steps (3) and (4) by alternately loosening the referenced hardware approximately two turns each. Continue to alternate between steps (3) and (4) until TDA2A1 is released.

(3) Loosen the four captive screws (fig. 4-10) on TDA2A1 mounting bracket.

(4) Rotate the knurled knob (fig. 4-10) on TDA2A1 input connector J1 clockwise.

(5) Slide TDA2A1 toward rear of receiver cabinet away from preselector 2FL4.

(6) Remove the four mounting bolts (fig. 4-4) securing preselector 2FL4 to preselector support.

(7) Remove the four screws, from inside the receiver cabinet, securing the preselector 2FL4 flange to the top of the receiver cabinet.

(8) Lift and remove preselector 2FL4 away from top of receiver cabinet, being careful not to

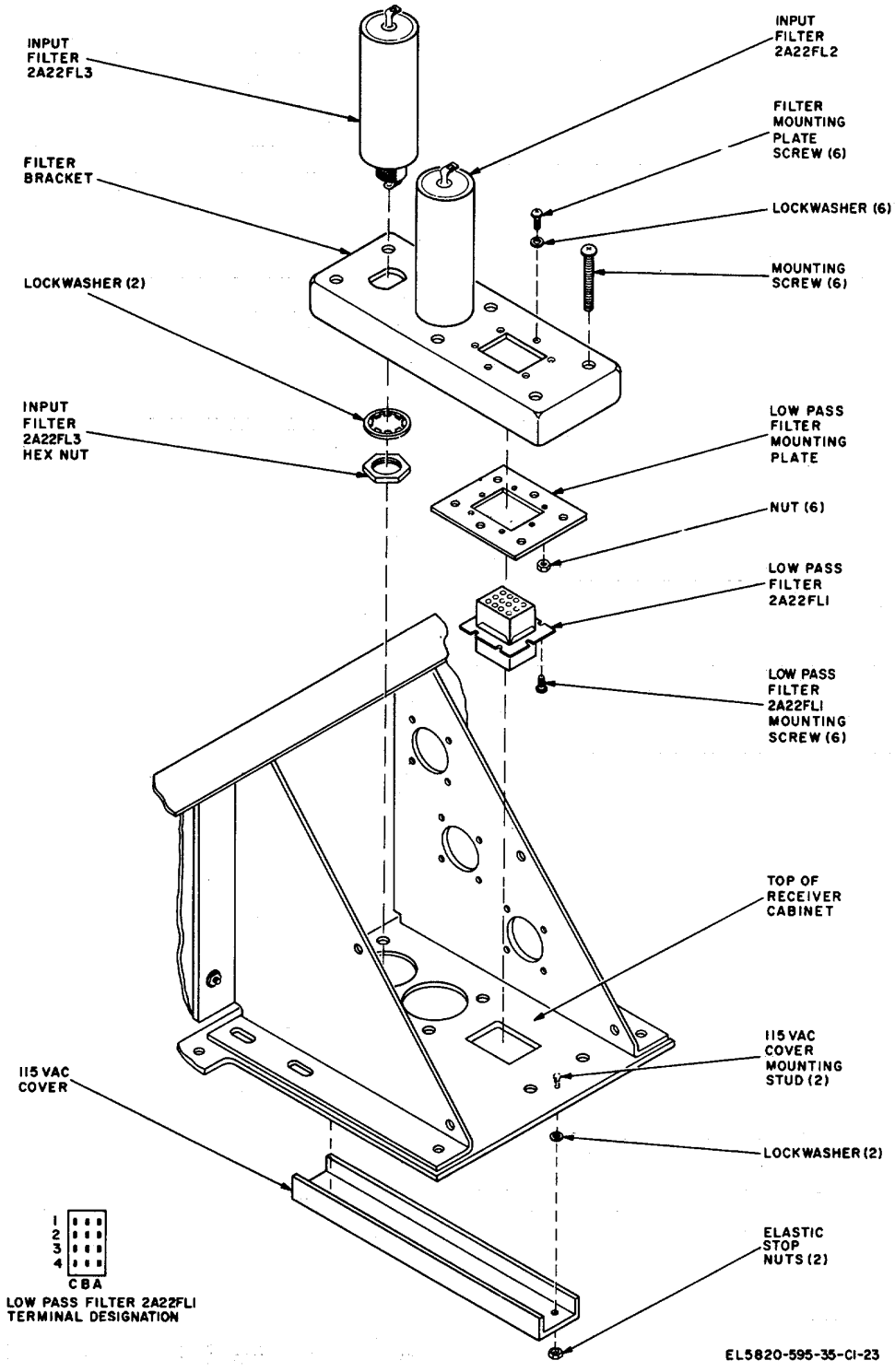


Figure 4-11. Removing low pass filter 2A22FL1, input filter 122FL2, or input filter 2A22FLS from receiver cabinet 2A22.

damage output connector 2FL4J1, which connects to TDA output connector 2A1J2.

b. Replacement.

(1) Mount replacement preselector 2FL4 on receiver cabinet being careful not to damage preselector connectors and controls.

(2) Secure preselector 2FL4 to receiver cabinet using the four screws removed in step a(7).

(3) Secure preselector 2FL4 to preselector support using the four mounting bolts removed in step a(6).

(4) Loosen and remove the eight screws securing the transit protective cover of the replacement preselector interface flange.

(5) Mount protective cover on the preselector removed in a (8).

(6) Slide TDA2A1 toward front of receiver cabinet aligning TDA2A1 input connector J1 with preselector output connector 2FL4J2 and loosely secure TDA2A1 to its mounting bracket with the four captive screws loosened in step a(3).

(7) Alternately rotate the knurled knob counterclockwise for approximately two turns and then the four captive screws approximately two turns each until TDA2A1 is secured to its mounting bracket and preselector 2FL4.

(8) Reconnect coaxial cable 2W1 to TDA output connector 2A1J2.

NOTE

Reconnect the external waveguide that was removed as noted after step a (1).

(9) Set the preselector FREQ MHZ dial indication to the same frequency setting of the frequency synthesizer.

(10) Replace power supply 2A3 in receiver cabinet by performing step (4) through (6) of paragraph 4-14b if preselector 2FL5 were replaced.

(11) Energize the radio set (para 3-13). Check that CARR (IF) A indicator on receiver meter panel is lighted green for replacement of preselector 2FL4. Check that CARR (IF) B indicator on receiver meter panel is lighted green for replacement of preselector 2FL5.

4-20. Replacement of 4.4-5.0 GHz Circulator 2HY1 or 2HY2

(figs. 4-4 and 4-10)

The following procedures cover 4.4-5.0 GHz circulator 2HY1 in detail. Using substituted -reference 4-36 designations, the same procedures are applicable to 2HY2.

a.. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cable 2W2 (fig. 4-12) from 4.4-5.0 GHz circulator 2HY1 connector J2.

(3) Loosen, remove and save the two mounting screws securing 2HY1 to coaxial circulator mounting bracket using an offset screwdriver.

(4) Loosen, remove and save the two circulator bracket mounting screws (fig. 4-10) securing the circulator bracket to the filter mounting plate (fig. 4-4).

(5) Remove the circulator bracket and save for reassembly.

(6) Loosen 2CP1 (fig. 4-10) from post selector 2FL6 and remove 2CP11 and 2HY1 from the receiver cabinet.

(7) Loosen 2CP1 from 2HY1 and save 2CP1 for reassembly.

b. Replacement.

(1) Connect 2CP1 to 4.4-5.0 GHz circulator 2HY1 connector J1.

(2) Connect 2CP1 to postselector 2FL6 in the receiver cabinet.

(3) Mount the circulator bracket in the receiver cabinet. Insert, align and loosely tighten the four mounting screws removed in step a(3) and (4). Tighten the four screws.

(4) Reconnect coaxial cable 2W2 (fig. 4-12) to 4.4-5.0 GHz circulator 2HY1 connector J2.

(5) Energize the radio set (para 3-13). Check that CARR (IF) A indicator on receiver meter panel is lighted green if 2HY1 were replaced. If 2HY2 were replaced, check that CARR (IF) B is lighted green.

4-21. Replacement of Post Selector 2FL6 or 2FL7

(figs. 4-4, 4-10 and 4-12)

The following procedures cover post selector 2FL6 in detail. Using substituted reference designations, the same procedures are applicable to 2FL7.

a. Removal.

(1) the radio set (para 3-12).

(2) Remove 2HY1 and 2CP1 by performing steps (2) through (6) provided in para 4-20a.

(3) Disconnect coaxial cable 2W1 (fig. 4-12) from post selector 2FL6 connector J2.

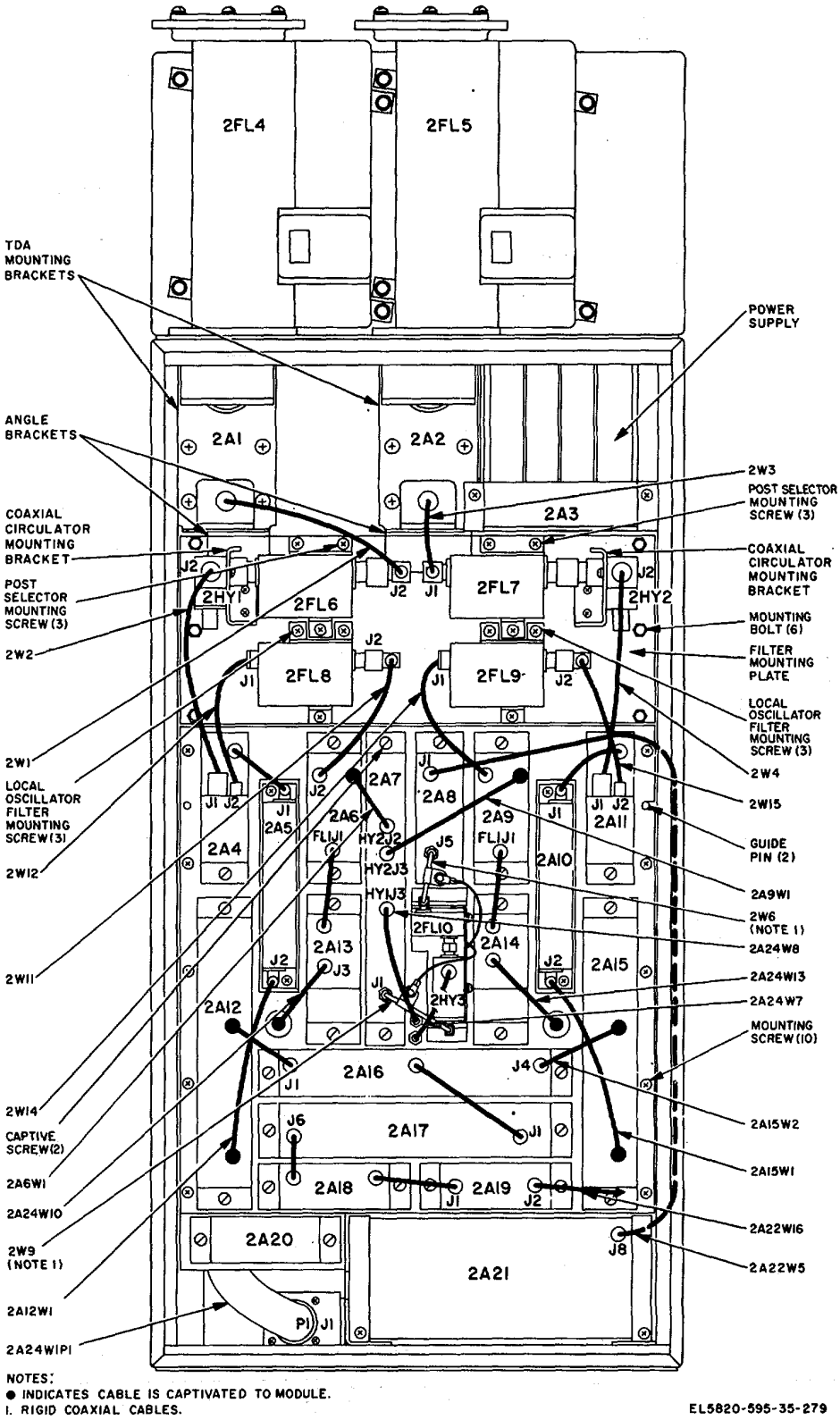


Figure 4-12. Receiver, front view, locating modules, assemblies, and coaxial cables.

(4) Loosen and remove the three post selector mounting screws (fig. 4-12) securing post selector 2FL6 to the filter mounting plate.

(5) Carefully remove post selector 2FL6 from receiver cabinet.

b. Replacement.

(1) Carefully mount replacement post selector 2FL6 (fig. 4-12) on filter mounting plate aligning the three mounting holes and secure 2FL6 using the three screws removed in step a(4).

(2) Replace 2HY1 and 2CP1 by performing steps (2) through (5) provided in paragraph 4-20b.

(3) Connect coaxial cable 2W1 (fig. 4-12) to post selector 2FL6 connector J2.

(4) Set the FREQ MHz dial indication to the same frequency setting of the frequency synthesizer.

(5) Energize the radio set (para 3-13). Check that CARR (IF) A indicator on receiver meter panel is lighted green if post selector 2FL6 were replaced. Check that CARR (IF) B indicator on receiver meter panel is lighted green if post selector 2FL7 were replaced.

4-22. Replacement of Local Oscillator Filter 2FL8 or 2FL9

(figs. 4-4, 4-10 and 4-12)

The following procedures cover local oscillator filter 2FL8 in detail. Using substituted reference designations, the same procedures are applicable to the 2FL9.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cables 2W12 and 2W11 (fig. 4-12) from local oscillator filter 2FL8 connectors J1 and J2 respectively.

(3) Loosen and remove the three mounting screws (fig. 4-12) securing local oscillator filter 2FL8 to the filter mounting plate.

(4) Carefully remove local oscillator filter 2FL8 from the receiver cabinet.

b. Replacement.

(1) Carefully mount replacement local oscillator filter 2FL8 on filter mounting plate aligning the three mounting holes and secure 2FL8 using the three screws removed in step a(3).

(2) Connect coaxial cables 2W12 and 2W11 4-38 (fig. 4-12) to local oscillator filter 2FL8 connectors J1 and J2 respectively.

(3) Set the FREQ MHZ dial indication on 2FL8 to the same frequency setting as the frequency synthesizer.

(4) Energize the radio set (para 3-13). If 2FL8 were replaced, check that the CARR (IF) A indicator on the receiver meter panel is lighted green. If 2FL9 were replaced, check that the CARR (IF) B indicator on the receiver meter panel is lighted green.

4-23. Removal of Filter Mounting Plate 2A22MP62

(figs. 4 4, 4-8, 4-10 and 4-12)

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Remove 4.4-5.0 GHz circulators 2HY1 and 2HY2 by performing steps (2) through (6) of paragraph 4-20a.

(3) Disconnect the following coaxial cables (fig. 4-12): 2W1 from 2FL6J1, 2W3 from 2FL7J1, 2W12 and 2W11 from 2FL8J1 and J2 respectively, and 2W14 and 2W15 from 2FL9J1 and J2 respectively.

(4) Loosen, remove and save the mounting hardware' (fig. 4-10)' securing each angle to TDA2A1 and TDA2A2 mounting brackets.

(5) Loosen, remove and save the six mounting bolts (fig. 4-12) securing the filter mounting plate to the receiver cabinet.

(6) Carefully remove the filter mounting plate from the receiver cabinet.

b. Replacement.

(1) Place filter mounting plate in receiver cabinet aligning the six mounting holes. Insert two of the six mounting bolts removed in step a (5) and finger tighten.

(2) Insert the remaining four bolts removed in step a(5) and tighten all six bolts securing filter mounting plate to the receiver cabinet.

(3) Secure each angle (fig. 4-10) to TDA2A1 and TDA2A2 mounting bracket using the hardware removed in step a (4).

(4) Reconnect the coaxial cables disconnected in step a(3) to their respective module connectors.

(5) Replace 4.4-5.0 GHz circulators 2HY1 and 2HY2 by performing procedural steps (2) through (4) of paragraph 4-20b.

(6) Energize the radio set (para 3-13).

c. Replacement of Parts on or behind Filter Mounting Plate 2A22MP62 (fig. 4-8).

Filter mounting plate 2A22MP62 must be removed to gain access to the following parts mounted on receiver cabinet 2A22: cable harness 2A22W1, terminal boards 2A22TB3 and 2A22TB4, and power transformer 2A22T1. Replacement procedures for power transformer 2A22T1 are provided in paragraph 427. Refer to figure 8-59 for cable harness and terminal board wiring information.

4-24. Replacement of 2275-2425 MHz Circulator 2A7HY1 or 4550-4850 MHz Power Divider 2A7HY2

(figs. 4-4 and 8-106)

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Remove frequency multiplier group 2A7 from receiver cabinet (TM 11-5820-595-12).

(3) Loosen, but do not remove, the three mounting screws securing 4550-4850 MHz power divider 2A7HY2 (fig. 8-106) to the frame.

(4) Loosen, but do not remove, the two screws securing 3rd frequency multiplier 2A7A2 to the frame.

(5) Loosen the connector between 2A7A2 and 2A7HY1, while simultaneously sliding 2A7HY2 and 2A7A2 toward the left away from 2275-2425 MHz circulator 2A7HY1 until 2A7A2 and 2A7HY1 are disconnected.

(6) Slide 2A7A2 and 2A7HY2 to the left as far as the frame mounting slot allows.

(7) Loosen the connector between 2A7HY2 and 2A7A2 while simultaneously sliding 2A7A2 toward rear of frame until the parts are disconnected.

(8) Lift 2A7A2 from frame and set aside.

(9) Remove the three screws loosely securing 2A7HY2 to the frame and remove 2A7HY2 from the frame.

NOTE

Proceed to step b(5) if 4450-4850 MHz power divider 2A7HY2 is the part being replaced or set 2A7HY2 aside if 2275-2475 MHz circulator 2A7HY1 is being replaced.

(10) Loosen, but do not remove, the two screws (fig. 8-106) securing 2nd frequency multiplier 2A7A1 to the frame.

(11) Loosen the connector between 2A7A1 and 2A7HY1 while simultaneously sliding 2A7A1 to the right until the parts are disconnected.

(12) Lift 2A7A1 from the frame and set aside.

(13) Remove the three screws securing 2A7HY1 to the frame and remove 2A7HY1 from the frame.

b. Replacement.

(1) Place replacement 2275-2425 MHz circulator 2A7HY1 (fig. 8-106) on the frame. Align 2A7HY1 with the three mounting holes on the frame. Secure 2A7HY1 to the frame using the hardware removed in step a(13).

(2) Place, 2nd frequency multiplier 2A7A1 on the 'frame aligning 2A7A1 mounting screws with the mounting slots.

(3) Tighten the connector between 2A7A1 and 2A7HY1 while simultaneously sliding 2A7A1 to the left toward 2A7HY1.

(4) Secure 2A7A1 to the frame by tightening the two mounting screws.

(5) Place 4450-4850 MHz circulator 2A7HY2 on the frame and loosely secure in place using the three screws removed in step a(9).

(6) Place 3rd frequency multiplier 2A7A2 on the frame aligning 2A7A2 mounting screws with the mounting slots.

(7) With 2A7A2 and 2A7HY2 at extreme left position in 1 sots, tighten the connector between the two parts while sliding 2A7A2 toward 2A7HY2.

(8) Tighten the connector between 2A7HY1 and 2A'7A2 while carefully sliding mated 2A7A2/ 2A7HY2 toward 2A7HY1.

(9) Secure 2A7HY2 and 2A7A2 to the frame by tightening their mounting screws.

(10) Replace frequency multiplier group 2A7 (TM 11.-5820-595-12) on plate assembly 2A24.

(11) Energize the radio set (para 3-13).Check at the CARR (IF) A and CARR (IF) B indicators on receiver meter panel are lighted green and perform the receiver local oscillator chain output power and metering test (para 4-10).

4-25. Replacement of Frequency Synthesizer Chassis 2A21A10

(figs. 4-4, 4-12 and 4-13)

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Remove frequency synthesizer 2A21 from receiver cabinet, then remove all modules including 2A21A8 from chassis 2A21A10 (TM 11-5820-595-12).

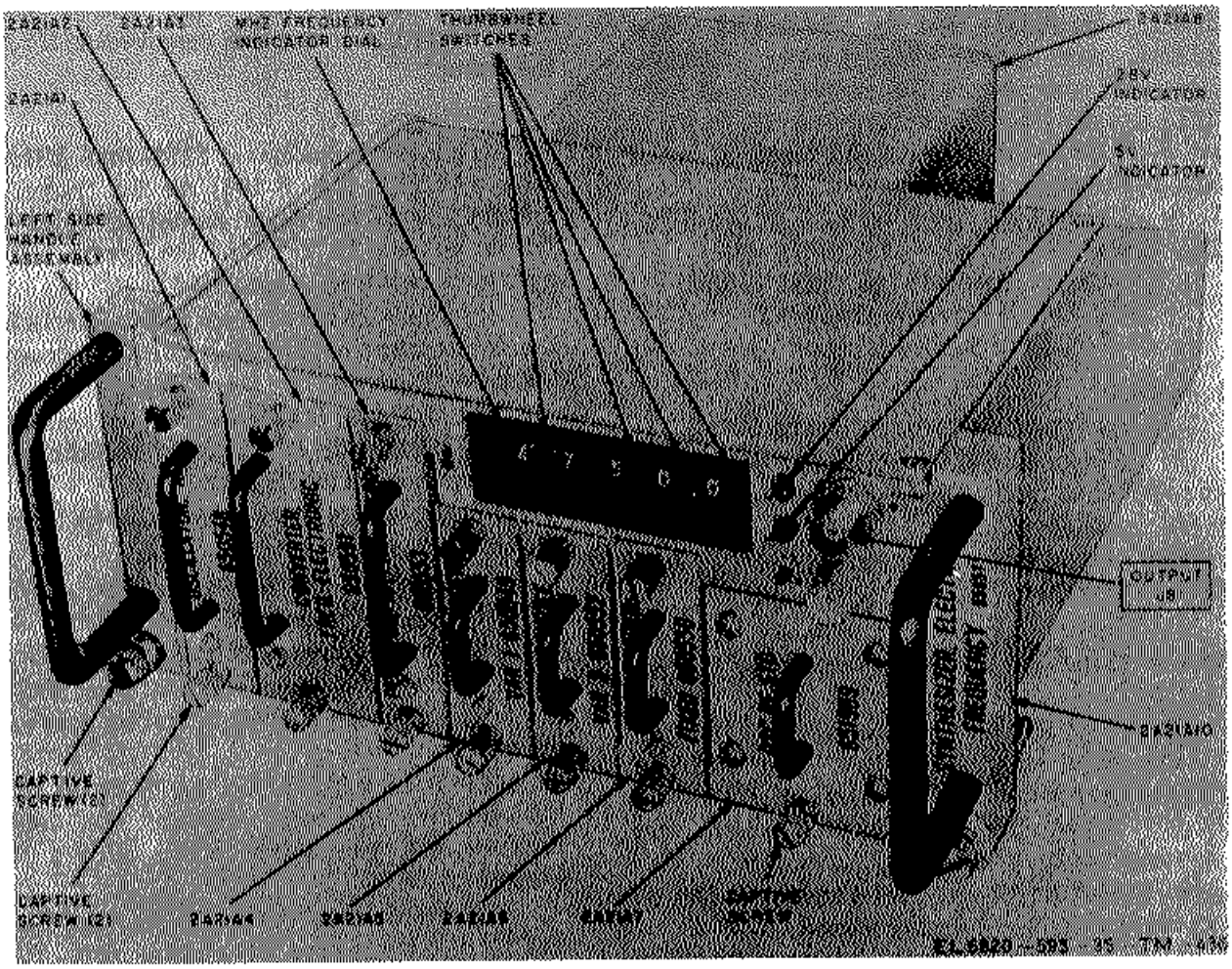


Figure 4-13. Receiver frequency synthesizer 2A21, front view, parts location.

(3) Loosen and remove the two screws securing the left side handle assembly (fig. 4-13) to frequency synthesizer chassis 2A21A10.

b. Replacement.

(1) Install the left side handle assembly (fig. 4-13) on frequency subthesizer chassis 2A21A10 and secure in place using the two screws removed in step a(4).

(2) Replace all modules on chassis 2A21A10 and replace frequency synthesizer 2A21 into receiver cabinet (TM 11-5820-595-12).

(3) Energize the radio set (para 3-13). Check that the SYNTH LOCK indicator on receiver meter panel is lighted green, indicator lamps on plug-in modules 2A21A1 through 4-40 2A21A6 are not lighted, and the output level indication of frequency synthesizer 2A21 checked with meter 2A22M1 on receiver meter panel is in the yellow band. Perform the frequency synthesizer alarm check (TM 11-5820-595-12).

4-26. Removal Plate Assembly 2A24
(figs. 4-4, 4-12 and 4-14)

a.. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect the following coaxial cables (fig. 4-12): 2W2 from 2A4J1, 2W12 from 2A4J2, 2W11 from 2A6J2, 2W14 from 2A9J2, 2W15 from 2A11J2, 2W4 from 2A11J1 and 2A22W5 at both ends. Support all loose coaxial cables out of the

way to prevent possible damage when removing plate assembly 2A24.

(2) Disconnect plug 2A24WIP1 (fig. 4-12) from connector 2A22J1.

(4) Remove the cable clamp and mounting hardware securing cable 2A24W1 to left side of receiver cabinet.

(5) Remove modules 2A12 and 2A15 from the plate assembly (TM 11-5820-595-12).

(6) Remove the ten mounting screws (fig. P12) securing plate assembly 2A24 to receiver cabinet 2A22.

(7) Remove plate assembly 2A24 from receiver cabinet 2A22 being careful not to damage the coaxial cables and the mounted plug-in modules.

b. Replacement.

(1) Replace plate assembly 2A24 by positioning plate assembly (fig. 4-12) on two receiver cabinet 2A22 guide pins.

(2) Secure plate assembly 2A24 to receiver cabinet 2A22 using the ten mounting screws removed in step a (6).

(3) Mount IF amplifiers 2A12 and 2A15 (fig. 4-12) on plate assembly and reconnect the coaxial cables removed in step a(5).

(4) Secure cable 2A24W1 to receiver cabinet using clamp and hardware removed in step a(4).

(5) Connect plug 2A24WIP1 (fig. 4-12) to connector 2A22J1.

(6) Release all coaxial cables from the support used in step a (2) and reconnect to their respective modules (fig. 4-12).

(7) Energize the radio set (para 3-13).

c. Replacement of Parts on or behind Plate Assembly 2A24 (fig. 4-12 and 4-14). Plate assembly 2A24 must be removed from receiver cabinet 2A22 to gain access the following parts mounted on 2A24: cable harness 2A24W1; connectors 2A24XA4, A24WIXA6, 2A24XA8, 2A24NW'1XA9, 2A24XA11, 2A24W1XA12, 2A24W1XA13, 2A24W1XA14, 2A24W1XA15, 2A24W1XA16, 2A24XA17, 2A24W1XA19, 2A24W1XA20A and 2A24W1XA20B; cables 2A24W7, 2A24W8, 2A24W10 and 2A24W13; rf filters 2A24FL11 through 2A24FL32; and terminal boards 2A24TB1 and 2A24TB2.

4-27. Replacement of Power Transformer 2A22T1 (fig. 4-8)

WARNING

115 vac is applied to power transformer 2A22T1. Be sure that the external ac power cable is disconnected from the AC POWER INPUT connector J5 (fig. 4-9) on top of receiver cabinet.

a.. Removal.

(1) Remove power supply 2A3 from receiver cabinet by performing steps (1) through (4) of paragraph 4-14a.

(2) Remove TDA2A1 and TDA2A2 from receiver cabinet by performing steps (2) through (10) and (13) through (16) of paragraph 418a.

(3) Remove preselector 2FL5 from receiver cabinet by performing steps (2) through (8) of paragraph 4-19a.

(4) Remove filter mounting plate from receiver cabinet by performing steps (2) through (6) of paragraph 4-23a.

(5) Remove plate assembly 2A24 by performing steps (2) through (7) of paragraph 4-26a.

(6) Remove the three power transformer cable clamps and their lock nuts (fig. 4-8) securing cable harness routed to power transformer 2A22T1.

(7) Remove the cable clamp and lock nut securing cable harness routed to connector 2A22XA3 (fig. 4-8).

(8) Loosen and remove the mounting hardware securing connector 2A22XA3 (fig. 4-8) to the connector mounting bracket. Remove connector from connector' mounting bracket and slide upward to clear rear of power supply enclosure.

(9) Remove the hardware securing connector mounting bracket to power supply enclosure and remove connector mounting bracket.

(10) Unsolder, remove and tag each lead connected to power transformer 2A22T1 terminals.

(11) Note the mechanical makeup for reassembly purposes, then remove the following hardware securing the self (fig. 4-8) in the receiver cabinet: ' two screws securing shelf to receiver cabinet left wall; two locknuts securing shelf to receiver cabinet rear wall; two screws, washers and locknuts securing shelf and one side of power transformer to power supply enclosure.

(12) Remove the shelf (fig. 4-8) from receiver cabinet.

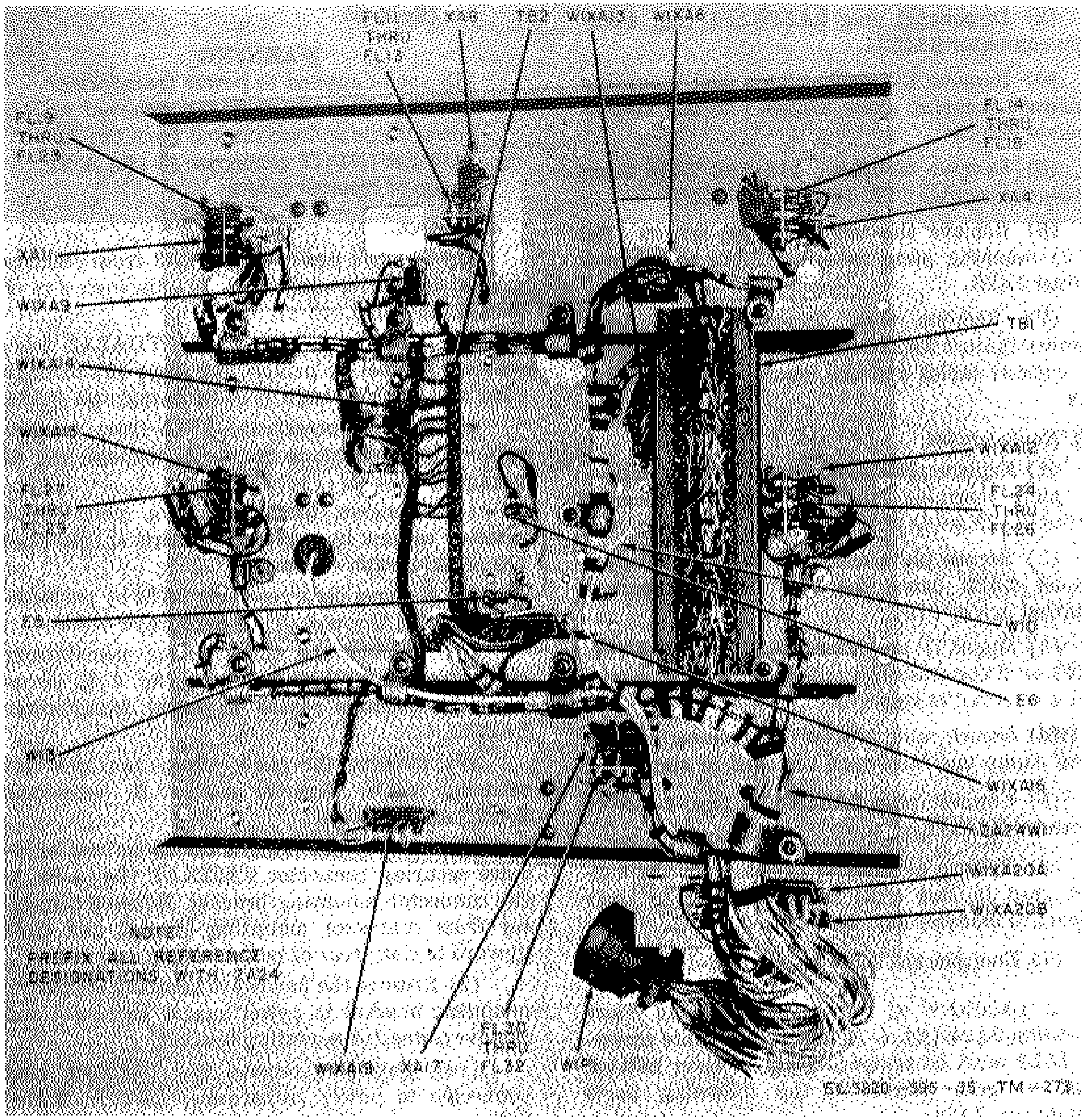


Figure 4-14. Receiver plate assembly 2A24, rear view, parts location.

(13) Replace and finger tighten the two screws, washers and locknuts removed in step (10), that are used to secure the power transformer 2A22T1 to power supply enclosure.

(14) Remove two main harness cable clamps A and B and mounting hardware (fig. 4-8) permitting main cable harness to be shifted to left.

(15) Loosen and remove the two screws, washers, and locknuts securing top of power supply enclosure to top of receiver cabinet.

NOTE

The two screws and washers (step 15) are accessible from outside the receiver cabinet and the locknuts are accessible from inside the receiver cabinet**.**

(16) Loosen and remove the two screws securing right side of power supply enclosure to receiver cabinet right side wall.

(17) Loosen and remove the two locknuts securing rear of power supply enclosure to receiver cabinet rear wall.

NOTE

Check that all cable harness leads routed to power transformer 2A22T1 and power supply enclosure are positioned to prevent damage or crimping the leads when power supply enclosure is removed.

(18) Carefully remove the combined assembly of power supply enclosure with power and transformer 2A22T1 from receiver cabinet by sliding the combined assembly approximately 3-inch to the left away from receiver cabinet right wall. Then slowly slide the combined assembly away from receiver cabinet rear wall and remove from receiver cabinet.

(19) Remove the four locknuts securing power transformer 2A22T1 to power supply enclosure and separate 2A22T1 from power supply enclosure noting power transformer terminal orientation.

b. Replacement.

(1) Mount replacement power transformer 2A22T1 on power supply enclosure orienting power transformer terminals as noted in step a(19).

(2) Replace the four locknuts removed in step a(19). Securely tighten the two locknuts which will be located next to receiver cabinet right wall and finger tighten the other two locknuts.

(3) Insert combined assembly of power transformer 2A22T1 and power supply enclosure (fig. 4-8) into receiver cabinet checking that the cable harness leads are not crimped or snagged by the combined assembly. Align the power supply enclosure two rear mounting holes with two mounting studs on receiver cabinet rear wall.

(4) Carefully slide the combined assembly into position so that the power supply enclosure is flush with receiver cabinet rear and side walls.

(5) Secure the power supply enclosure to the TM 11-5820-595-35 receiver cabinet by replacing the hardware removed in step a(15), (16) and (17).

(6) Secure main cable harness to receiver cabinet rear wall by replacing the cable clamps A and B and secure with the hardware removed in step a(14).

(7) Remove the two lock nuts that were finger-tightened in step b (2). Position that shelf (fig. 4-8) in the receiver cabinet, and secure it with the mounting hardware removed in step a(11).

(8) Tighten all hardware replaced in b7, including the two locknuts that were loosely tightened in step (2) that secure shelf and power transformer 2A22T1 to power supply enclosure.

(9) Remount and secure connector mounting bracket to power supply enclosure using hardware removed in step a(9)..

(10) Remount and secure connector 2A22XA3 to connector mounting bracket using hardware removed in step a(8).

(11) Dress and secure cable harness routed to connector 2A22XA3 using clamp and hardware removed in step a(7).

(12) Connect and solder the power transformer terminal leads removed in step a(10) and perform the receiver primary power distribution circuit checks (para 4-5).

(13) Secure the cable harness leads to power transformer 2A22T1 to the receiver cabinet using the power transformer cable clamps and hardware removed in step a (6).

(14) Replace plate assembly 2A24 in receiver cabinet by performing steps (1) through (6) of paragraph 4-26b.

(15) Replace filter mounting plate in receiver cabinet by performing 'steps (1) through (5) of paragraph 4-23b.

(16) Replace preselector 2FL5 in receiver cabinet by performing steps (1) through (10) of paragraph 4-19 b.

(17) Replace TDA2A1 and TDA2A2 in receiver cabinet by performing steps (12) through (18) of paragraph 4-18b.

(18) Energize the radio set (para 3-13).

4-28. Repair and Replacement of Receiver Connectors

(fig. 8-59)

a. General. Repair of connectors in the receiver requires either; the replacement of the defective connector (solder type nonremovable contacts), or

the replacement of defective connector contacts (crimp type removable contacts). A listing of receiver connectors is provided in b below. This chart specifies connector type, the required repair procedure, the applicable tools and figure reference

Procedures for replacing the different type connector contacts are provided in paragraph 3-32. A continuity check should be performed after a connector or connector pin has been replaced.

b. Receiver Connectors.

Connector	Extraction /insertion tool	Crimping tool	Procedure paragraph	Figure reference
2A3A5P1	MS 18278 Size 20/None	MS 3191 4 with Head Assy. W25	*3-32c*	4-6
2A22XA3	Same	Same	*3-32c*	4-8
2A24W1XA6	Same	Same	*3-32c*	4-14
2A24W1XA9	Same	Same	*3-32c*	4-14
2A24W1XA12	Same	Same	*3-32c*	4-14
2A24W1XA13	Same	Same	*3-32c*	4-14
2A24W1XA14S	Same	Same	*3-32c*	4-14
2A24W1XA15	Same	Same	*3-32c*	4-14
2A24W1XA16	Same	Same	*3-32c*	4-14
2A24WIXA19	Same	Same	*3-32c*	4-14
2A24W1XA20B	Same	Same	*3-32c*	4-14
2A24XA4	Same	Same	*3-32c*	4-14
2A24XA8	MS 18278 Size 20/None	MS 3191-4 with Head Assy. W25	*3-32c*	4-14
252A24XA11	MS 18278 Size 20/None	MS 3191-4 with Head Assy. W25	*3-32c*	4-14
252A24XA17	MS 18278 Size 20/None	MS 3191-4 with Head Assy. W25	*3-32c*	4-14
252A22XA21	CET C6B/None	None	*3-32d*	4-8
2A24W	1XA20A	CETC6B,/None	*3-32d*	4-14
2A22W1J1	MS 24256 R20,/A20	MS 31914 with Head Assy W1	*3-32e*	4-8
2A22W1P2	MS 24256 R20/20	MS 31914 with Head Assy W1	*3-32e*	4-8
2A22W1P3	Same	Same	*3-32e*	4-8
2A24W1P1	MS 24256 R20/A20	MS 31914 with Head Assy W1	*3-32e*	4-12
2A3A5XA1 through 2A3A5XA4	None required	None required	*4-15e*	4-6
2A22J2	None required	None required	*4-15e*	4-9
2A22J3	None required	None required	*3-2f*	4-9
2A22J5	None required	None required	*3-32f*	4-9

4-29. Removal and Replacement of Connector Bracket 2A22MP5 or Connector 2A22XA21

(fig. 4-8)

Connector bracket 2A22MP5 must be removed from receiver cabinet 2A22 to provide access to connector 2A22XA21.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Remove plate assembly 2A24 from receiver cabinet 2A22 (para 426a).

(3) Remove frequency synthesizer 2A21 from receiver cabinet 2A22 (TM 11-5820- 595-12).

(4) Loosen and remove cable clamp c (fig. 4-8) securing harness leads to connector 2A22XA21 mounted on connector bracket.

(5) Loosen the mounting hardware securing connector 2A22XA21 (fig. 4-6) to connector bracket and release connector from connector bracket.

(6) Loosen and remove four self locking nuts securing connector bracket 2A22'MP5 to receiver cabinet rear wall.

CAUTION

When moving connector bracket in any direction, exercise care to prevent stressing or damage to coaxial cable and wire harness leads.

(7) Slide connector bracket away from the four studs on the rear receiver cabinet wall. Then move connector bracket to left while swinging right side clear of right slide welded (fig 4-8).

(8) Carefully remove connector bracket from receiver cabinet.

(9) Loosen and remove two cable clamps (fig. 4-8) securing coaxial cable to receiver cabinet rear wall. The cable clamps are those that are normally behind connector bracket 2A22MPS.

(10) If required, transfer wired connector contacts from connector 2A22XA21 to its identical terminal position on the replacement connector. Refer to paragraph 4-28 for the applicable connector pin replacement procedures.

b. Replacement.

(1) Secure the coaxial cable to the receiver cabinet rear wall using the two cable clamps and hardware removed in step a (9).

(2) Position connector bracket in receiver cabinet close to rear wall. Secure replacement connector 2A22XA21 to the connector bracket using the mounting hardware removed in step a (5).

(3) Slide connector bracket into position and mount on the four studs on receiver cabinet rear wall.

(4) Secure connector bracket to receiver cabinet using the hardware removed in step a (6).

(5) Secure harness leads to receiver cabinet rear wall using cable clamp c and hardware removed in step a (4). Perform a continuity check for each connector contact on connector 2A22AX21 referring to fig. 859 for wire routing.

(6) Replace frequency synthesizer 2A21 in receiver cabinet (TM 11-5820-595-12).

(7) Replace plate assembly 2A24 (para 4-26 b(1) through (6).

(8) Energize the radio set (para 3-13). The SYNTH LOCK indicator on receiver meter panel is lighted green, indicator lamps on plug-in modules 2A21A1 through 2A21A6 are not lighted, and the output level indication of frequency synthesizer 2A21 checked with meter 2A22M1 on receiver meter panel is in the yellow band. Perform the frequency synthesizer alarm check (TM 11-5820-595-12).

4-30. Replacement of 1137-1213 MHz Circulator 2HY3 and 1137-1213 MHz Bandpass Filter 2FL10

(figs. 4-4 and 4-12)

Replacement of 1137-1213 MHz circulator 2HY3 or 1137-1213 MHz bandpass filter 2FL10 requires removal of a mounting bracket attached to plate assembly 2A24. Both modules are mounted on the mounting bracket.

a. Removal.

(1) Deenergize the radio set (para 3-12).

(2) Disconnect coaxial cable 2A4W7 (fig. 4-12) from 1137-1213 MHz circulator 2HY3 connector DC MONITOR J3.

CAUTION

The steps referenced for removal of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(3) Disconnect rigid coaxial cable 2W9 and 2W6 (para 3-14').

(4) Remove the two screws securing the mounting bracket to plate assembly 2A24 and remove mounting bracket with the 2HY3 and 2FL10 attached.

(5) The 2FL10 is secured to the mounting bracket with two screws in the side of the bracket and four screws in the rear of the bracket. Remove the six screws.

(6) Loosen the mating type TNC connector between the 2HY3 and 2FL10, and slide the 2FL10 away from 2HY3. Remove the 2FL10 from the mounting bracket.

NOTE

If 1137-1213 MHz bandpass filter 2FL10 is the part being replaced proceed to step b (2) for the replacement procedure. If 1137-1213 MHz circulator 2HY3 is to be replaced continue with step (7) and set 2FL10 aside for reassembly.

(7) Remove three screws from the side of the mounting bracket to release the 2HY3.

b. Replacement.

(1) Place replacement 1137-1213 MHz circulator 2HY3 on the mounting bracket, align 2HY3 mounting holes with mounting slots on side of mounting bracket and loosely secure to the mounting bracket with the three mounting screws.

(2) Place 1137-1213 MHz bandpass filter 2FL10 on the mounting bracket and align mating

type TNC connector with INPUT J1 connector on 2HY3.

(3) Finger tighten the type TNC connector.

(4) Replace the six screws removed in step a(5) to loosely secure 2FL10 to the mounting bracket and then firmly tighten the mating type TNC connector between the two units.

(5) Tighten the four screws at rear of mounting bracket that secure 2FL10 to the mounting bracket. Then tighten the five screws on the side of the mounting bracket.

(6) Place the mounting bracket with 2FL10 and 2HY3 on plate assembly 2A24 and secure the mounting bracket to plate assembly 2A24 with the two screws removed in step a(4).

CAUTION

Replacement of components with rigid coaxial cables must be performed carefully to prevent damage to the rigid coaxial cables.

(7) Connect rigid coaxial cable 2W9 between 2HY3J2 and-'2A7J1, and 2W6 between 2FL10J1 and 2A8J5 (para 3-14).

(8) Connect coaxial cable 2A24W7 to 1137-1213 MHz circulator 2HY3 connector DC MONITOR J3 (fig. 4-12).

(9) Energize the radio set (para 3-13) and perform the receiver local oscillator chain output power and metering test provided in paragraph 4-10.

Section III. RECEIVER CALIBRATION AND ADJUSTMENT

4-31. General

a. This section contains procedures for calibrating receiver meter 2A22M1, the receiver metering circuits, and adjusting the receiver vco frequency. The calibration procedures (para 4-32 through 4-35) are performed at periodic maintenance intervals (para 2-4) to maintain the calibration accuracy of the receiver metering circuits, or when receiver tests (para 4-8 through 4-10) or troubleshooting indicates that calibration is required. The adjustment procedure (para 4-36) is performed when troubleshooting (para 4-3d) indicates that a receiver vco frequency adjustment is required.

b. All of the procedures contained in this section assume that the radio set is turned on and connected for normal operation at the start of each procedure. Prior to performing any of the procedures, the maintenance man should notify the Multiplexer TD-204/U and distant radio set operators that maintenance must be performed on the radio set and that radio communications will be temporarily interrupted.

c. If trouble is encountered during performance of a procedure, or if the indications specified in the procedure are not obtained, refer to the receiver troubleshooting chart (para 4-3d) for corrective action.

4-32. Calibration of Receiver Meter 2A22M1

a. Turn the TS-656/U on and allow a 5 minute warmup period.

b. Set POWER ON/OFF switch 2A22S2 (fig. 4-15) to OFF.

c. Turn meter selector switch 2A22S1 to OFF (TRANSIT).

d. Adjust the meter zero screw on front of meter 2A22M1 for a zero meter indication.

e. Turn meter selector switch 2A22S1 to TEST LEAD (+).

f. On the TS-656/U, set FUNCTION switch to DIR CUR, set CURRENT switch to 100 MICRO-AMP, and rotate DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the TEST LEAD jack (fig. 4-15) on the receiver meter panel.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the E2 CAB GRD lug (fig. 4-9) on top of the receiver.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing steps j and k below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter 2A22M1 indicates 150.

k. Record meter indication on TS-656/U and then release the TEST switch.

l. Turn the TS-656/U off and disconnect the test leads.

m. Meter indication recorded in step k should be 37.5 + 1.5 microamperes. If. it is not, replace meter 2A22M1 (para 4-13).

n. Set POWER ON/OFF switch 2A22S2 (fig. 4-15) to ON.

4-33. Calibration of Receiver Traffic Metering Circuit

a. Turn the TS-656/U on and allow a 5 minute warmup period.

b. Set POWER ON/OFF switch 2A22S2 to OFF.

c. Remove alarm monitor 2A20 (fig. 4-4) from plate assembly 2A24 (TM 11-5820-595-12).

d. Connect the connector adapter 11A3 (part c MK-1207A/RC) to connector 2A24W1XA20A (fig 4-15),.

e. Turn meter selector switch 2A22S1 to TRAFFIC.

f. On the TS-656/U, set FUNCTION switch to DIR CUR, set CURRENT switch to 100 MICROAMP, and rotate DECREASE/INCREASE control counterclockwise until mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the red test jack TP1 on the connector adapter 11A3.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the black test jack TP2 on the connector adapter 11A3.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing steps j and k below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter on TS-656/U indicates 50 microamperes.

k. Indication on meter 2A22M1 should be 100. If it is not, perform the adjustment given in step I below. Otherwise, proceed to step m below.

l. Remove the protective plate over the potentiometer bracket, unlock potentiometer 2A22R11 (fig. 4-5) and with the TEST switch on TS-656/ U in the test position, adjust 2A22R11 for a 2A22M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the receiver troubleshooting. chart (para 4-3d) for TM 11-5820-595-35 corrective action upon completion of the procedure.

m. Turn the TS-656/U off and disconnect the test leads.

n. Remove connector adapter 11A3 from connector 2A24W1XA20A (fig. 4-15) and reinstall alarm monitor 2A20 on plate assembly 2A24.

o. Set receiver POWER ON/OFF switch 2A22S2 (fig. 4-15) to ON.

4-34. Calibration of Receiver Local Oscillator Output Power Metering Circuits

a. Turn on the AN/USM-161 and AN/ URM-52B on and allow a 30 minute warmup period.

b. Disconnect coaxial cable 2W12 from the J1 connector on local oscillator filter 2FLS.

c. Turn meter selector switch 2A22S1 (fig. P16) to LOCAL OSC POWER.

d. Set switch 2A22S3 (fig. 4-16) on receiver meter panel to A.

e. Calibrate the AN/USM-161 using the procedures given in TM 11-6625-49812 and calibrate the AN/URM-52B at 4700 MHz using the procedures given in TM 11-6625-214-10.

f. Connect the equipment as shown in figure 3-22.

g. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3.0 MW +5 DBM, set the COMP ATTENUATOR dial to 0, and set the POWER indicator dial for a dial scale indication of 1.0 on the center scale.

h. Adjust the OUTPUT ATTEN control on AN/URM-52B until a null indication is obtained on the AN/USM-161 NULL INDICATOR.

i. Adjust the POWER SET control on AN/ URM-52B for an index indication of 0 dbm on the OUTPUT ATTEN dial.

j. Turn the AN/USM-161 off and disconnect CG-92D/U and type N female to female adapter 11CP from the DT 255/USM-161 (fig. 3-22).

k. Set the OUTPUT ATTEN control an AN/ URM-52B for a dial scale indicator of -6 dbm (0.25 milliwatts).

l. Connect the equipment as shown in figure 4-16.

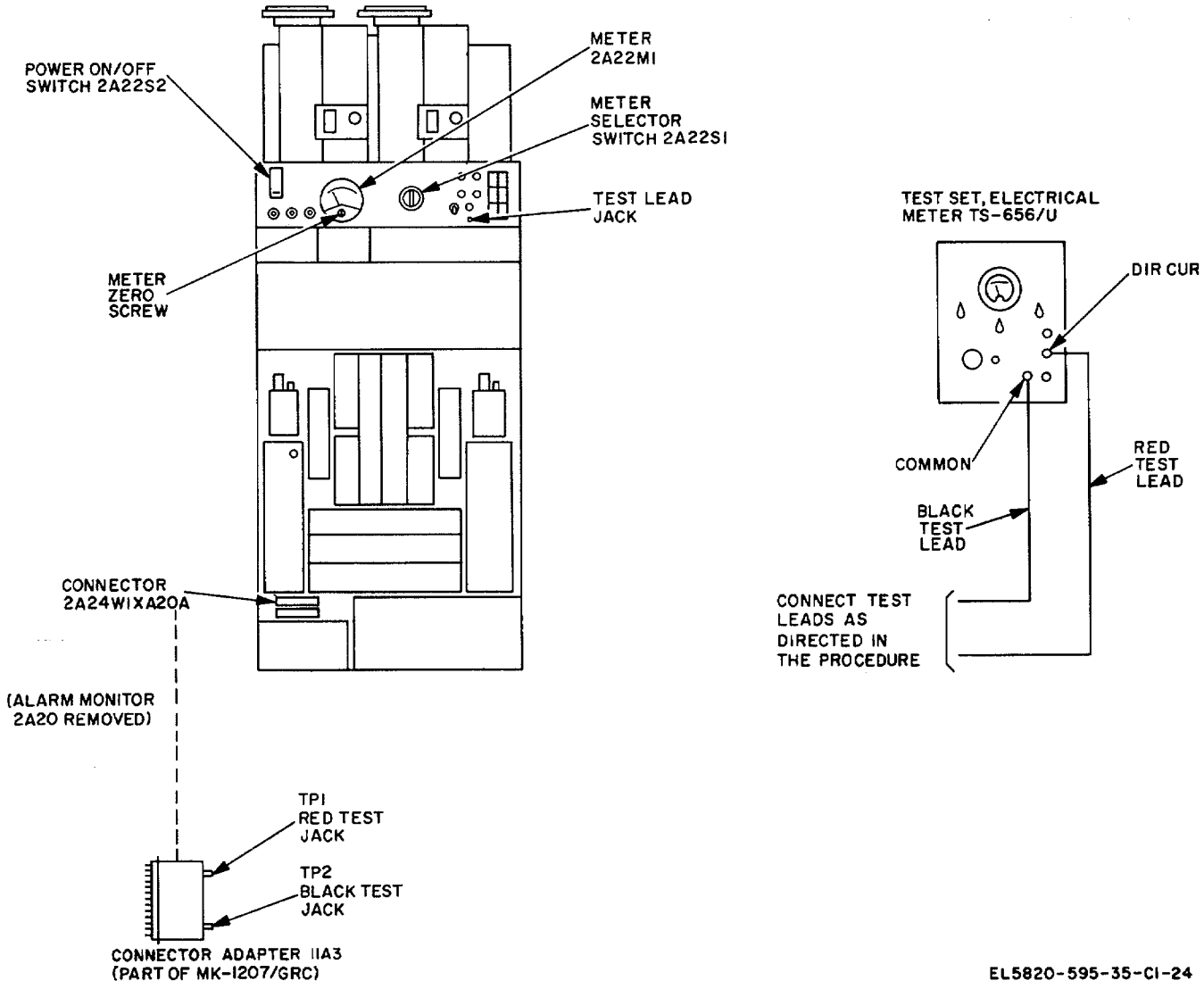


Figure 4-15. Receiver meter 2A22M1 calibration test set up.

m. Indication on receiver meter 2A22M1 should be 30. If it is not, perform the adjustment given in step n below. Otherwise, proceed to step o below.

n. Remove the protective plate over the potentiometer bracket, unlock potentiometer 2A22R9 (fig. 4-5) and adjust it for a 2A22M1 meter indication of 30. If a meter indication of 30 cannot be obtained, refer to the receiver troubleshooting chart (para 4-3d) for corrective action upon completion of this procedure.

o. Set receiver switch 2A22S3 (fig. 4-16) on receiver meter panel to B.

p. Disconnect the type N female to TNC female adapter 11CP2 coaxial cable 2W12 (fig. 4-16) and then reconnect coaxial cable 2W12 to J1 connector on local oscillator filter 2FL8.

q. Disconnect coaxial cable 2W15 (fig. 4-16) from the J2 connector on local oscillator filter 2FL9.

r. Connect the free end of coaxial cable 2W15 to the CG-92D/U, using the type N female to TNC female adapter 11CP2.

s. Indication on meter 2A22M1 should be 30. If it is not, perform an adjustment given in step t below. Otherwise, proceed to step u below.

t. Unlock potentiometer 2A22R10 (fig. 4-5) and

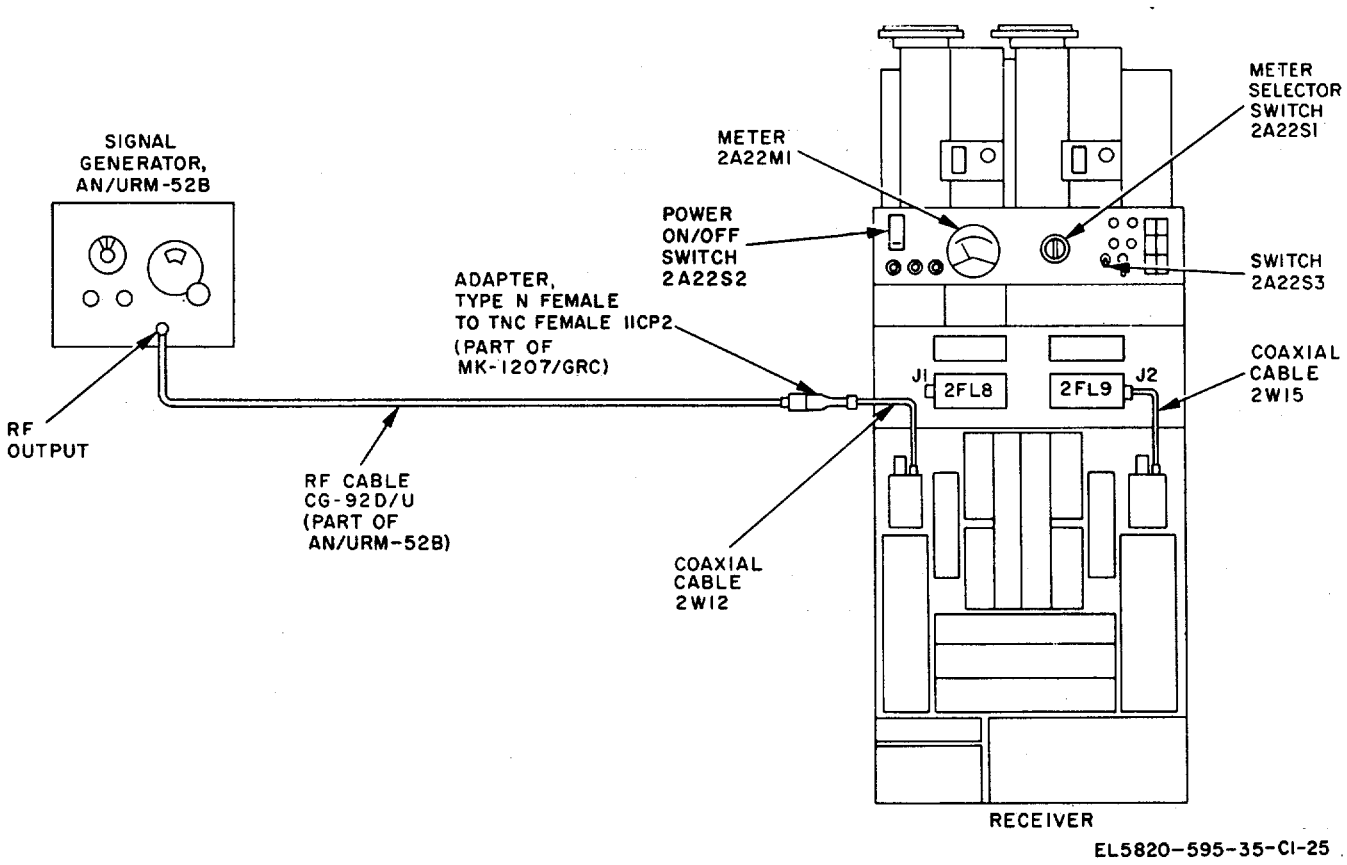


Figure 4-1 6. Receiver local oscillator output power metering circuits calibration test set up.

adjust it for a 2A22M1 meter indication of 30. If a meter indication of 30 cannot be obtained, refer to the receiver troubleshooting chart (para 43d) for corrective action upon completion of this procedure.

u. Turn the AN/URM-52B off and disconnect the test equipment.

v. Connect coaxial cable 2W15 (fig. 4-16) to the J2 connector on local oscillator filter 2FL9.

4-35. Calibration of Receiver Local Oscillator Chain Metering Circuits

NOTE

Do not calibrate any of the receiver local oscillator chain metering circuits when the receiver's local oscillator output power is less than 0.5 milliwatts. Use the receiver local oscillator chain output power and **metering test (para 4-10) to determine** the receiver's local oscillator output power if it is not known**.**

To calibrate any of the receiver, local oscillator chain metering circuits, turn meter selector switch 2A22S1 (fig. 4-4) to the circuit to be calibrated and observe the indication on meter 2A22M1. If meter indication is not 100, remove the protective plate over the potentiometer bracket, unlock the potentiometer listed below and adjust it for a 2A22M1 meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the receiver troubleshooting chart (para 4-3d) for corrective action.

Meter selector switch 2A22S1	*Potentiometer adjusted*
AMPL-MULT	2A22R1
2ND MULT	2A22R2
MULT OSC A	2A22R3
MULT OSC B	2A22R4
FREQ MIXER CURRENT (3RD MULT) Al	2A22R5
FREQ MIXER CURRENT (3RD MULT) A2	2A22R6
FREQ MIXER CURRENT (3RD MULT) B1	2A22R7
FREQ MIXER CURRENT (3RD MULT) B2	2A22R8

4-36. Receiver VCO Frequency Adjustment

a. Turn the AN/USM-207 on and allow a 15 minute warmup period.

b. Set the controls on AN/USM-207 as follows:

(1) SENSITIVITY switch to PLUG-IN.

(2) FUNCTION switch to FREQ.

(3) Time base switch to GATE TIME (SEC -1 -103.

(4) Converter attenuator switches (upper and lower) to 10V MAX.

(5) DIRECT-HETERODYNE switch to HETERODYNE.

(6) Mixing frequency selector switch to 200.

(7) DISPLAY control to the desired display time.

c. On the receiver, set both APC switches on combiner 2A16 (fig. 4-1) to OFF.

d. Disconnect coaxial cables 2A24W10 and 2A24W13 from 2A13J3 and 2A14J3 (view B, figure P1).

e. Connect the equipment as shown in view B, figure 4-1.

f. Observe the LEVEL METER on AN/ USM-207. If meter indication is in the green zone, proceed to step h below. Otherwise, perform step g below.

g. Alternately set the upper and lower converter attenuator switches on AN/USM-207 to the left, one position at a time, until LEVEL METER indication is in the green zone.

h. Remove the green cap from the FREQ ADJUST control on module 2A13, and using the tuning tool, adjust the control for a digital display of 20 MHz on AN/USM-207. Replace the greet. cap.

i. Disconnect the BNC to subminiature adapter 11CP3 from 2A13J3 (view B, figure 4-1) and connect it to 2A14J3.

j. Remove the green cap from the FREQ ADJUST control on module 2A14, and using the tuning tool, adjust the control for a digital display of 20 MHz on AN/USM-207. Replace the green cap.

k. Turn off and disconnect the test equipment.

l. Reconnect coaxial cables 2A24W10 and 2A24W13 to 2A13J3 and 2A14J3 respectively.

m. Set both APC switches on combiner 2A16 to ON.

n. Turn meter selector switch 2A22S1 to VCO FREQ DIFF. 2A22M1 indication should be in the blue band. If it is not, set both APC switches on combiner 2A16 to OFF and adjust the FREQ ADJUST control on 2A13 for a minimum indication on meter 2A22M1. Set both APC switches on combiner 2A16 to ON.

CHAPTER 5
POWER AMPLIFIER DIRECT SUPPORT MAINTENANCE

Section I. POWER AMPLIFIER TROUBLESHOOTING

WARNING
ELECTROMAGNETIC
RADIATION

High frequency electromagnetic radiation is present in the power amplifier. Do not work on the power amplifier waveguides or the external waveguides connected to the power amplifier cabinet while the power amplifier is turned on. High frequency electromagnetic radiation can cause fatal internal burns. It can literally "cook" internal organs and flesh. If you feel the slightest warming effect while near the power amplifier MOVE AWAY QUICKLY

WARNING

Voltages in excess of 7,000 volts are present in the power amplifier. Do not disable or bypass any equipment interlocks unless it is specifically stated in the text. Do not place hands or tools near any high voltage terminal in the power amplifier. 230 vac is also present in the power amplifier. Do not remove or replace parts; or perform continuity or resistance check while primary power is applied to the equipment.

5-1. Scope of Power Amplifier Maintenance

This chapter contains direct support maintenance procedures for troubleshooting, repairing, calibrating, adjusting, and checking the power amplifier. Paragraph 5-2 specifies power amplifier preventive maintenance. Detailed procedures are provided for troubleshooting (para 5-3 and 5-4), repairs (para 5-5 through 5-15) and calibrations and adjustments (para 5-16 through 5-27). Procedures for deenergizing and energizing the radio set are provided in paragraphs 3-12 and 3-13 respectively.

5-2. Power Amplifier Calibration Checks and Tests

Periodic calibration checks and tests must [be performed as periodic preventive maintenance on the power amplifier to verify the calibration accuracy of its metering circuits and check its operating condition. Paragraph 2-4 lists the calibration checks and tests that must be performed on each unit of the radio set, and specifies the maintenance interval in which they should be performed.

5-3. Power Amplifier Troubleshooting Charts

a. General. The power amplifier troubleshooting charts are supplied as an aid in localizing troubles in the power amplifier. The charts list the symptoms that may be observed when sectionalizing a trouble to the power amplifier and includes or references the procedures to be used to locate and correct the trouble.

b. Use of the Charts. The power amplifier troubleshooting chart (d below) supplements the operational checks and corrective measures contained in TM 11-5820-595-12. Apply the operational checks and corrective measures contained in TM 11-5820-595-12 before using the troubleshooting chart in this manual. If the corrective measures for the operational checks in TM 11-5820-595-12 fail to correct the trouble or indicate that higher category maintenance is required,

apply the corrective measures listed in the chart below. To use the chart, read down the symptom column of the troubleshooting chart until the abnormal indication or condition is found. Then perform the corrective measures indicated in the chart for that item. The numbers of the items in e below correspond to the numbers of the items in d below.

c. Conditions for Troubleshooting. In general, power amplifier troubleshooting begins with the radio set turned on and connected for normal operation. During performance of troubleshooting, it is often necessary to check a part by substitution or to perform continuity and resistance checks. Performing corrective measures of this nature require that the power amplifier be deenergized (para 3-12) before the part is substituted, or the continuity and/or resistance check is made. After the corrective measure has been performed, the power amplifier must be energized (para 3-13) to determine whether the corrective measure has corrected the trouble. If the corrective measure fails to correct the trouble, proceed to the next corrective measure and repeat the cycle. Procedures for performing continuity and resistance checks are provided in paragraph 5-4. Procedures for replacing parts in the power amplifier are provided in paragraphs 5-5 through 5-15. figures 5-1 through 5-17 are parts location diagrams which will aid the maintenance man in locating parts within the power amplifier.

d. Power Amplifier Troubleshooting Chart.

Caution:

During all handling and use of klystron 3A9V1, keep all magnetic materials six inches away(wristwatches). Keep all magnets 12 inches away.

Item	*Symptom*	*Probable trouble*	*Corrective measure*
1	Fuse 3A9A23F1 blows when replaced.	a. Defective component or wire in unfiltered -12 volt power supply.	a. Deenergize the power amplifier (para, 3-12) and check resistance between pins 5 and 6 of transformer 3A9T2 (fig. 5-13 and 8-69). Resistance should beapproximately 10 ohms with either polarity of test leads.
		b. Defective wiring	b. If meter indication is less than 3 ohms for both meter indications, check for defective wiring between terminal 6, 3A9T2 and pin 11 of time delay control module 3A5 (fig. 8-69).
		c. Bridge rectifier 3A9CR8 defective.	c. If meter indication is less than 3 ohms for either meter indication, but not both, trouble is defective bridge rectifier 3A9CR8 (fig. 5-13).
		d. Transformer 3A9T2 defective-	d. If meter indication is approximately 10 ohms for both meter indications, trouble is shorted transformer 3A9T2 (fig. 5-13) winding, or defective wiring between fuse 3A9A23F1 and transformer 3A9T2. Perform continuity and resistance checks (para 5-4) to trace and isolate the trouble.,
2	All status and alarm indicators on the power amplifier meter panel are extinguished.	Loss of primary ac power, MAIN POWER SWITCH 3A9A32A1S5 defective, or defective component or wire in unfiltered -12 volt power supply.	Refer to item 2 in the power amplifier flow charts (para 5-3e).
3	MAIN POWER SWITCH and BEAM SWITCH indicators on power amplifier meter panel lighted; all other status and alarm indicators are extinguished.	Defective component or wire in +28 , volt power supply, or transformer 3A9T1 'defective.	Refer to item 3 in the power amplifier flow charts (para 5-3e).
4	TIME DELAY indicator on power amplifier meter panel still lighted	a. Same as. item 6 in this chart	a. Check FILAMENT indicator on amplifier meter panel. If this in-

Item	Symptom	Probable trouble	Corrective measure
	amber 4.0 minutes after MAIN POWER SWITCH has been activated (lighted green).		dicator is lighted red, refer to item 6 in this chart.
		b. Defective wiring	b. Deenergize the power amplifier (para 3-12). Remove 3A3 and 3A5 and check for continuity between pin 3 of connector 3A9XA5 and pin T of connector 3A9XA3 (fig. 8-69).
5	AIR indicator on power amplifier meter panel lighted red.	Thermal switch 3A9V1S2 defective, or blower assembly 3A9B1 defective.	Refer to item 5 in the power amplifier flow charts (para 5-3e).
6	FILAMENT indicator on power amplifier meter panel lighted red.	Klystron filament leads 3A9P3 or 3A9P4 disconnected, klystron tube 3A9V1 defective, or filament voltage power supply defective,	Refer to item 6 in the power amplifier flow charts (para 5-3e).
7	DC OVERLOAD indicator on power amplifier meter panel lighted red.	Klystron tube 3A9V1 defective-	Refer to item 7 in the power amplifier flow charts (para 5-3e).
8	AC INTERLOCK indicator on power amplifier meter panel lighted red.	High voltage interlock door open -	Refer to item 8 in the power amplifier flow charts (para 5-3e).
9	ANTENNA MISMATCH indicator on power amplifier meter panel lighted red.	Antenna mismatch trip point requires adjusting, or antenna defective.	Refer to item 9 in the power amplifier flow charts (para 5-3e).
10	AC OVERLOAD indicator on power amplifier meter panel lighted red.	High voltage power supply 3A9A1 defective, or klystron tube 3A9V1 defective.	Refer to item 10 in the power amplifier flow charts (para 5-3e).
11	LOW RF indicator on power amplifier meter panel lighted red.	Low rf alarm trip point requires adjusting, or klystron tube 3A9V1 defective.	Refer to item 11 in the power amplifier flow charts (para 5-3e).
12	BEAM indicator on power amplifier meter panel lighted red; all other indicators lighted green.	Defective wiring	Deenergize the power amplifier (para 3-12) and check for continuity (fig. 8-69) between pin U of connector 3A9XA2 and pin L of connector 3A9XA6.
13	Main blower and cabinet fans continue to operate after blower time delay has elapsed.	MAIN POWER SWITCH 3A9A32A1S5 defective.	Replace MAIN POWER SWITCH 3A9A32A1S5 (para 5-7).
14	Main blower 3A9B1B1 not operating.	a. Main blower 3A9B1B1 defective.	a. Deenergize the power amplifier (para 3-12) and check resistance between pins A and B of connector 3A9B1J9 (fig. 5-10). Resistance should be 15±5 ohms.
		b. Defective wiring	b. Make the following continuity checks: Check for continuity (fig. 8-69) between pin A of plug 3A9W11P5 (connected to 3A9B1J9) and pin 18 of connector 3A9XA5; check for continuity between pin B of plug 3A9W11P5 and terminal 1 of meter 3A9M1.
		c. Capacitor 3A9B1C1 defective-	c. Check capacitor 3A9B1C1 (para 5-13) by substitution.
15	All cabinet fans (3A9A26B2 through 3A9A26B5) not operating.	One of the cabinet fans is defective, or defective cabinet wiring.	Refer to item 15 in the power amplifier flow charts (para 5-3e).

Item	Symptom	Probable trouble	Corrective measure
16	Any cabinet fan (3A9A26B2 through 3A9A26B5) not operating.	Cabinet fan defective -	Deenergize the power amplifier (para 3-12). Remove fan assembly 3A9A26 (para 5-14). Tag and remove wires connected to inoperative cabinet fan. Make the following resistance checks: T1 to T4 (fig. 8-69) should be 500 - 100 ohms; and T1 to T5 should be 800+100 ohms. If correct resistance is obtained, use continuity checks (para 5-4) to check wiring between inoperative fan and 3A9A26TB1.
17	FILAMENT VOLTAGE meter indication not in green band.	Defective component in filament voltage metering circuit or FILAMENT VOLTAGE meter 3A9M2 defective.	Refer to item 17 in the power amplifier flow charts (para 5-3e).
18	BEAM VOLTAGE meter indication not in green band.	Defective component in beam voltage metering circuit or BEAM VOLTAGE meter 3A9M3 defective.	Refer to item 18 in the power amplifier flow charts (para 5-3e).
19	BEAM CURRENT meter indication not in green band.	Defective component in beam current metering circuit or BEAM CURRENT meter 3A9M4 defective.	Refer to item 19 in the power amplifier flow charts (para 5-3e).
20	No indication on RF MONITOR meter 3A9M5 when RF MONITOR SELECT switch 3A9S8 is set to each position.	a. Defective wiring	a. Deenergize the power amplifier (para 3-12) and check for continuity (fig. 8-69) between RF MONITOR SELECT switch 3A9S8 and RF MONITOR meter 3A9M5 (fig. 5-2).
		b. RF MONITOR meter 3A9M5 defective.	b. Check RF MONITOR meter 3A9M5' by performing the RF MONITOR meter calibration procedure (para 5-20).
		c. RF MONITOR SELECT switch 3A9S8 defective.	c. Check RF MONITOR SELECT switch 3A9S8 by substitution (para 5-7).
21	ANTENNA FORWARD WATTS X 10 meter indication not in green band.	Defective component in metering circuit or metering circuit requires calibration.	Refer to item 21 in the power amplifier flow charts (para 5-3e).
22	ANTENNA REFLECTED WATTS meter indication not in blue band.	Defective component in metering circuit or metering circuit requires calibration.	Check metering circuit by performing the power amplifier antenna mismatch trip point adjustment and reflected power metering circuit calibration procedure (para 5-25).
23	INPUT FORWARD MILLIWATT meter indication not in yellow band.	Defective component in metering circuit or metering circuit requires calibration.	Refer to item 23 in the power amplifier flow charts (para 5-3e).
24	FILAMENT RUNNING TIME indicator 3A9M1 not operating.	a. FILAMENT RUNNING TIME indicator 3A9M1 defective.	a. Check for 115 vac between terminals 1 and 2 of FILAMENT RUNNING TIME indicator 3A9M1 (fig. 5-2). If 115 vac is obtained, replace FILAMENT RUNNING TIME indicator 3A9M1 (para 5-7).
		b. Defective wiring	b. Deenergize the power amplifier (para 3-12) and check wiring at terminals (fig. 8-69) of FILAMENT

Item	Symptom	Probable trouble	Corrective measure
			RUNNING TIME indicator 3A9M1 (fig. 5-2) using continuity checks (para 5-4).
25	Cannot calibrate the power amplifier input power metering circuit (para 5-21).	a. Defective component or wire in metering circuit.	a. Deenergize the power amplifier (para 3-12) and make the following checks: Check resistance between center conductor of coaxial cable 3A9W11W3P1 (fig. 5-13) and pin A5 of RF MONITOR SELECT switch 3A9S8 (fig. 5-2). Note that resistance varies smoothly from zero to 10,000 ohms as INPUT potentiometer 3A9A23R19 (fig. 5-17) is varied from one extreme to the other. Also check for continuity between pin B5 of RF MONITOR SELECT switch 3A9S8 and the (negative) terminal of meter 3A9M5.
		b. RF MONITOR meter 3A9M5 defective.	b. Check RF MONITOR meter 3A9M5 by performing the RF MONITOR meter calibration procedure (para 5-20).
		c. Crystal detector 3A9XCR13 defective.	c. Check crystal detector 3A9XCR13 (fig. 5-13) by substitution (TM 11-5820-595-12).
		d. Directional coupler 3A9DC1 defective.	d. Check directional coupler 3A9DC1 (fig. 5-13) by substitutior.
26	Cannot calibrate the power amplifier forward power metering circuit (para 5-22).	a. Defective component or wiring in metering circuit.	a. Deenergize the power amplifier (para 3-12) and make the following checks: Check resistance between center conductor of coaxial cable 3A9W11-W8P1 (connected to 3A9XCR17) and pin Al of RF MONITOR SELECT switch 3A9S8 (fig. 8-69). Note that resistance varies smoothly from zero to 10,000 ohms as OUTFWD potentiometer 3A9A23R17 (fig. 5-17) is varied from one extreme to the other. Also check for continuity between pin B1 of RF MONITOR SELECT switch 3A9S8 and the - (negative) terminal of meter 3A9M5.
		b. RF MONITOR meter 3A9M5 defective.	b. Check RF MONITOR meter 3A9M5 by performing the RF MONITOR meter calibration procedure (para 5-20).
		c. Crystal detector 3A9XCR17 defective.	c. Check crystal detector 3A9XCR17 by substitution (TM 11-5820-595-12).
		d. Directional coupler 3A9DC2 defective.	d. Pull magnet support of cabinet (para 5-8a(1) through (9) and check directional coupler 3A9DC2 (fig. 5-15) by substitution.
		e. Waveguide assembly 3A9W9 defective.	e. Check waveguide assembly 3A9W9 (fig. 5-12) by substitution.
		f. Output filter 3A9FL8 defective	f. Check output filter 3A9FL8 (fig. 5-12) by substitution.

Item	Symptom	Probable trouble	Corrective measure
27	Cannot adjust power amplifier dc overload trip point (para 5-24).	Defective wiring	Deenergize the power amplifier (para 3-12) and make the following checks: Remove beam gate-dc overload control module 3A6 and check for continuity between pin T (fig. 8-69) of connector 3A9XA6 and TP1 BM I CAL test jack 3A9A23J8 (fig. 5-17); remove control indicator 3A3 and check for continuity between pin P of connector 3A9XA3 and pin S of connector 3A9XA6. Also check resistance between pin J of connector 3A9XA3 and chassis ground 3A9E1 (fig. 8-69). Resistance should be greater than 25 ohms. Check for continuity between pin A of connector 3A9XA3 and pin A of DC OVERLOAD indicator 3A9XDS37 (fig. 8-69).
28	Cannot calibrate the power amplifier beam current metering circuit (para 5-24).	a. Defective component or wire in metering circuit.	a. Deenergize the power amplifier (para 3-12) and make the following checks: Check resistance between jack 3A9A23J8 and chassis ground 3A9E1 (fig. 8-69). Resistance should be 10±0.1 ohms. Remove bracket assembly 3A9A23 from cabinet wall and check for continuity between TP1 BM I CAL test jack 3A9J8 and terminal 6 of bracket assembly 3A9A23 (fig. 8-69). Check resistors 3A9A23R11, 3A9A23R12, and 3A9A23R13 (fig. 5-17) by substitution.
		b. BEAM CURRENT meter 3A9M4 defective.	b. Check BEAM CURRENT meter 3A9M4 by performing the BEAM CURRENT metercalibration procedure (para 5-19).
29	Cannot adjust power amplifier antenna mismatch trip point (para 5-25).	a. Defective module 3A4	a. Deenergize the power amplifier (para 3-12) and check module 3A4 by substitution.
		b. Defective component or wire in metering circuit.	b. Deenergize the power amplifier (para 3-12) and make the following checks: Check for continuity between the center conductor of coaxial cable 3A9W11W6P1 and pin F of connector 3A9XA4 (fig. 8-69). Check for continuity between pin J of connector 3A9XA4 and pin S of connector 3A9XA3. Check for continuity between pin L of connector 3A9XA3 and pin B of ANTENNA MISMATCH indicator 3A9XDS41. Check for continuity between pin D of connector 3A9XA3 and pin A of ANTENNA MISMATCH indicator 3A9XDS41.
		c. Crystal detector 3A9XCR14 defective.	c. Check crystal detector 3A9XCR14 (fig. 5-15) by substitution (TM 11-5820-595-12).
		d. Directional coupler 3A9DC2 defective.	d. Check directional coupler 3A9DC2 (fig. 5-15) by substitution.

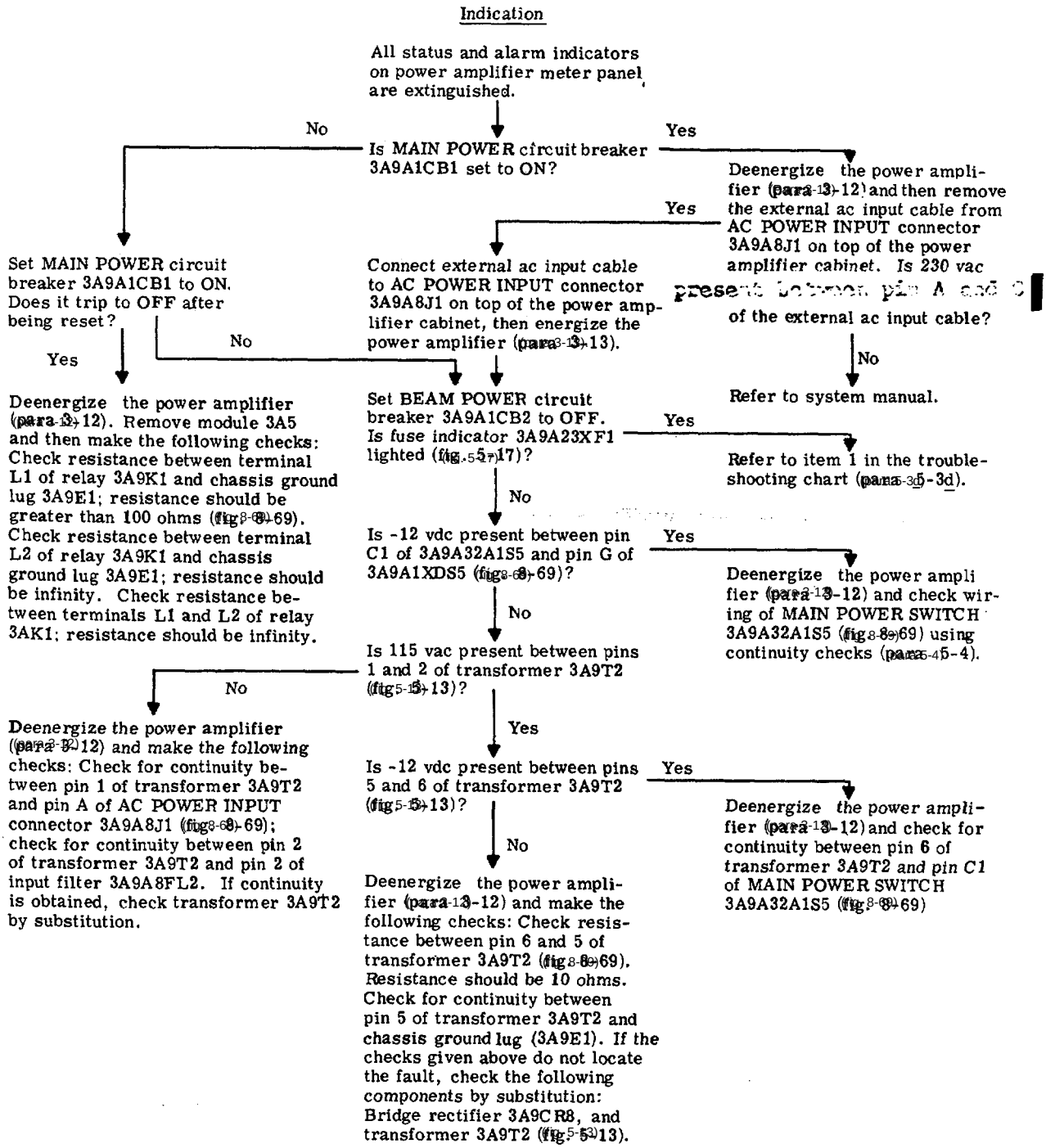
Item	Symptom	Probable trouble	Corrective measure
30	Cannot calibrate the power amplifier reflected power metering circuit (para 5-25).	a. Defective component or wire in metering circuit.	a. Deenergize the power amplifier (para 3-12) and make the following checks: Check resistance between the center conductor of coaxial cable 3A9W11W7P1 and pin A3 of RF MONITOR SELECT switch 3A9S8 (fig. 8-69). Note that resistance varies smoothly from zero to 10,000 ohms as OUT REFL potentiometer 3A9A23R18 (fig. 5-17) is varied from one extreme to the other. Also check for continuity between pin B3 of RF MONITOR SELECT switch 3A9S8 and the ® (negative) terminal of meter 3A9M5.
		b. RF MONITOR meter 3A9M5 defective.	b. Check RF MONITOR meter 3A9M5 by performing the RF MONITOR meter calibration procedure (para 5-20).
		c. Crystal detector 3A9XCR14 defective.	c. Check crystal detector 3A9XCR14 (TM 11-5820-595-12) by substitution.
		d. Directional coupler 3A9DC2 defective.	d. Check directional coupler 3A9DC2 (fig. 5-15) by substitution.
31	Cannot adjust power amplifier filament voltage (para 5-26).	Same as item 6 in this chart	Refer to item 6 in this chart.
32	Cannot calibrate the power amplifier filament voltage metering circuit (para 5-26).	a. FILAMENT VOLTAGE meter 3A9M2 defective.	a. Check FILAMENT VOLTAGE meter 3A9M2 by performing the FILAMENT VOLTAGE meter calibration procedure (para 5-17).
		b. Potentiometer 3A9R5 or resistor 3 A9R7 defective.	b. Check resistors 3A9R5 and 3A9R7 (fig. 5-14) by substitution.
33	Cannot perform the power amplifier filament current sensing check (para 5-27).	Same as item 6 in this chart	Refer to item 6 in this chart.

e. Power Amplifier Flow Charts.

Note:

The item number used in the flow chart corresponds to the same item number in the power amplifier troubleshooting chart (para 5-3d).

ITEM 2



e. Power Amplifier Flow Charts (cont).

ITEM 3

Indication

MAIN POWER SWITCH and BEAM SWITCH indicators on power amplifier meter panel lighted; all other status and alarm indicators are extinguished.

Main blower 3A9B1B1 and cabinet fans 3A9A26B2 through 3A9A26B5 operating?

No → Deenergize the power amplifier (para 3-12) and make the following checks: Check for continuity between pin C3 of BEAM SWITCH 3A9A34A1S4 and pin B of connector 3A9XA5 (fig. 8-69). Also check for continuity between pin 16 of connector 3A9XA5 and pin C of AC POWER INPUT connector 3A9A8J1 (fig. 8-69).

Yes ↓

Is CONTROL POWER circuit breaker 3A9A1CB4 set to OFF?

Yes → Set CONTROL POWER circuit breaker 3A9A1CB4 to ON. Does it trip to OFF after being reset?

No → Deenergize the power amplifier (para 3-12) and make the following checks: Use continuity checks to determine if any of transformer 3A9T1 windings are shorted (fig. 8-69). Remove power supply control module 3A7 from the cabinet; energize the power amplifier (para 3-13). Does CONTROL POWER circuit breaker 3A9A1CB4 trip to OFF?

Yes → Deenergize the power amplifier (para 3-12) and make the following checks: Check for continuity between pin 3 of transformer 3A9T1 and pin 6 of rectifier assembly 3A9A21 (fig. 8-69). Check for continuity between pin 4 of transformer 3A9T1 and pin 6 of rectifier assembly 3A9A21. If the checks given above do not locate the fault, check the following components by substitution: 3A9A21CR2, and 3A9A21CR1 (fig. 8-69).

No ↓

Set BEAM POWER circuit breaker 3A9A1CB2 to OFF. Is 28 vac present between pins 5 and 7 of transformer 3A9T1 (fig. 5-14 and 8-69)?

No → Is 115 vac present between pin 1 and 2 of transformer 3A9T1 (fig. 5-14 and 8-69)?

No → Deenergize the power amplifier (para 3-12) and check for continuity between pin 1 of transformer 3A9T1 and pin F of 3A9W11P1 (fig. 8-69).

Yes → Deenergize the power amplifier (para 3-12) and replace transformer 3A9T1 (fig. 5-14).

Yes ↓

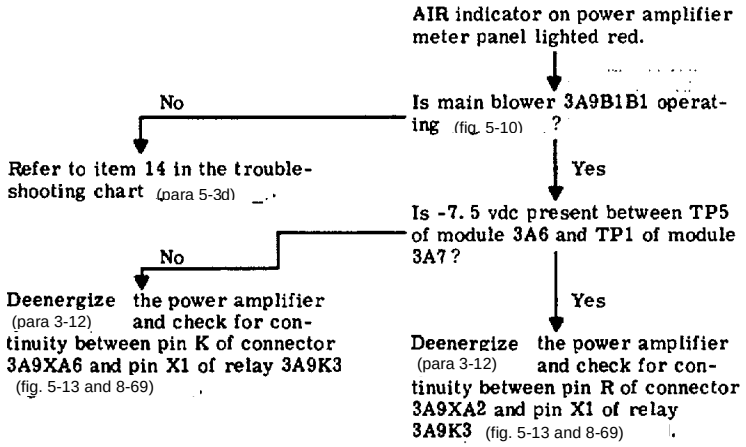
Deenergize the power amplifier (para 3-12) and make the following checks: Check for continuity between pin 5 of transformer 3A9T1 and pin N of connector 3A9XA7 (fig. 5-14 and 8-69). Check for continuity between pin 7 of transformer 3A9T1 and pin R of connector 3A9XA7. Check for continuity between pin D of connector 3A9XA7 and pin G of indicator light socket 3A9XDS17 (fig. 8-69).

No → Deenergize the power amplifier (para 3-12) and reinstall power supply control module 3A7. Check for continuity between the following points: from pin D of connector 3A9XA7 to pin H of connector 3A9XA7; from pin F of connector 3A9XA7 to pin J of connector 3A9XA7; and from pin B of connector 3A9XA7 to pin 8 of connector 3A9XA7 (fig. 8-69).

e. Power Amplifier Flow Charts (cont).

ITEM 5

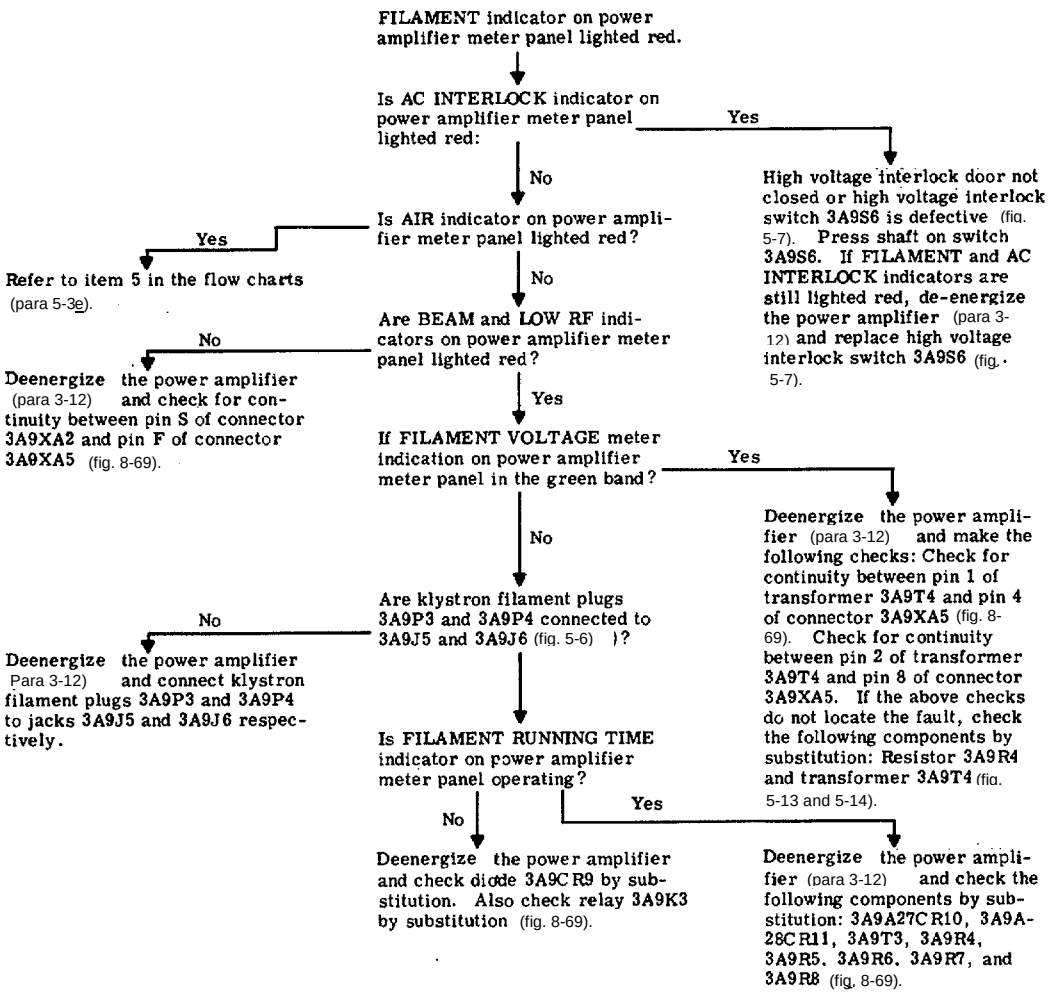
Indication



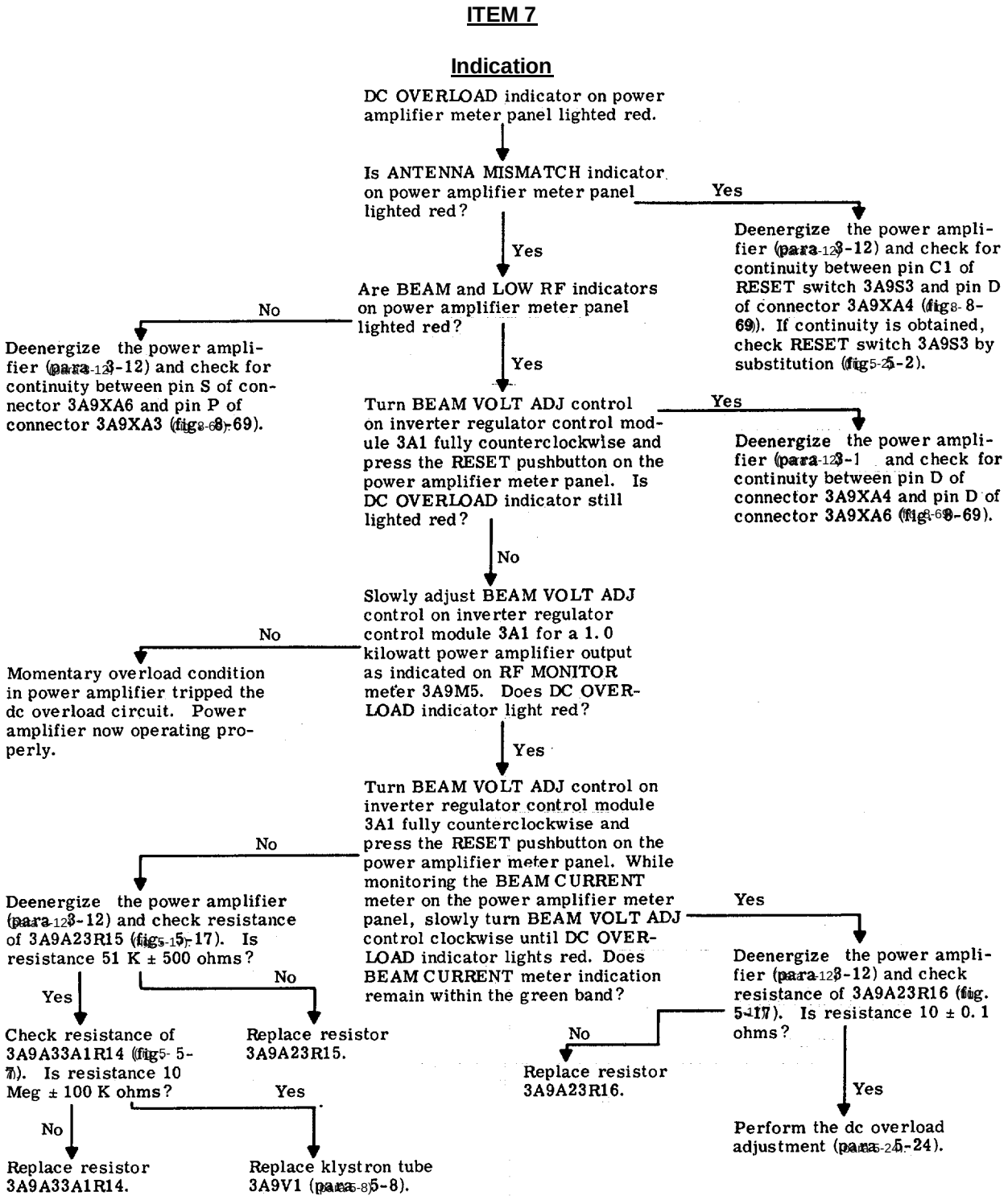
e. Power Amplifier Flow Charts (cont).

ITEM 6

Indication



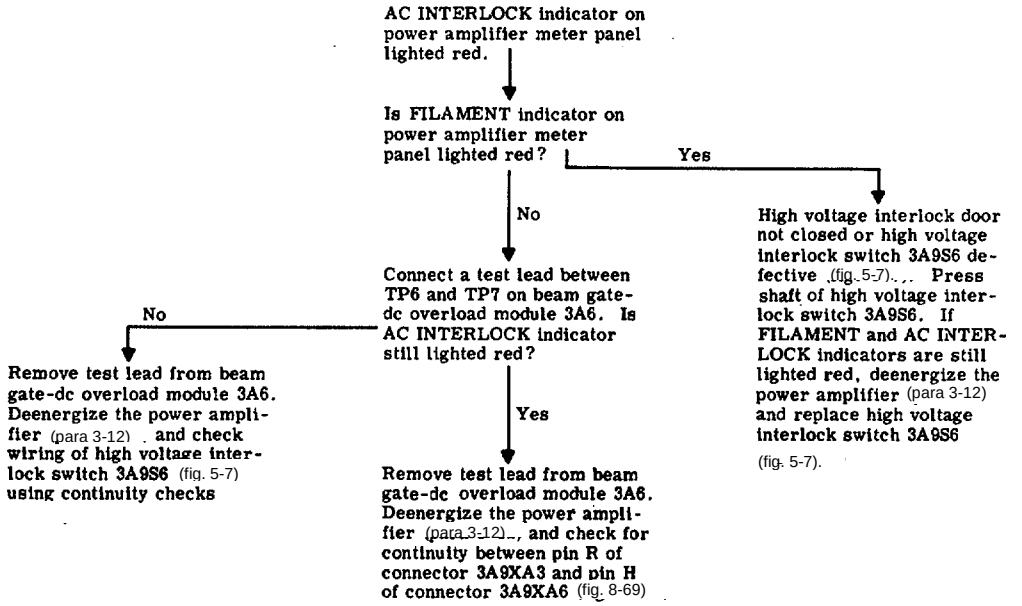
e. Power Amplifier Flow Charts (cont.)



e. Power Amplifier Flow Charts (cont).

ITEM 8

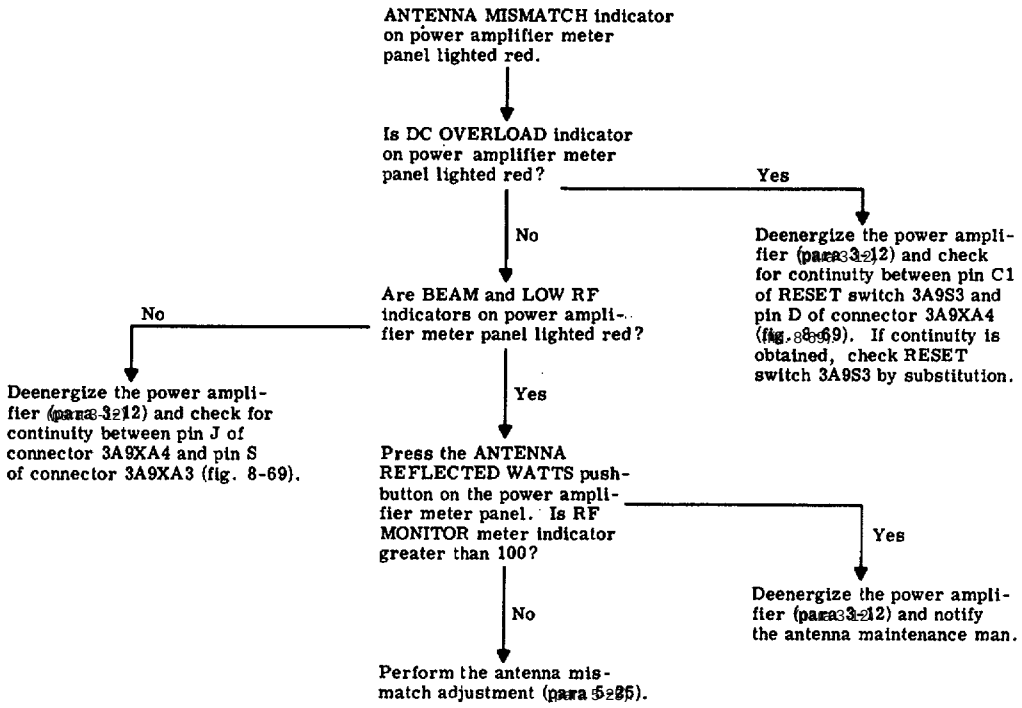
Indication



e. Power Amplifier Flow Charts (cont).

ITEM 9

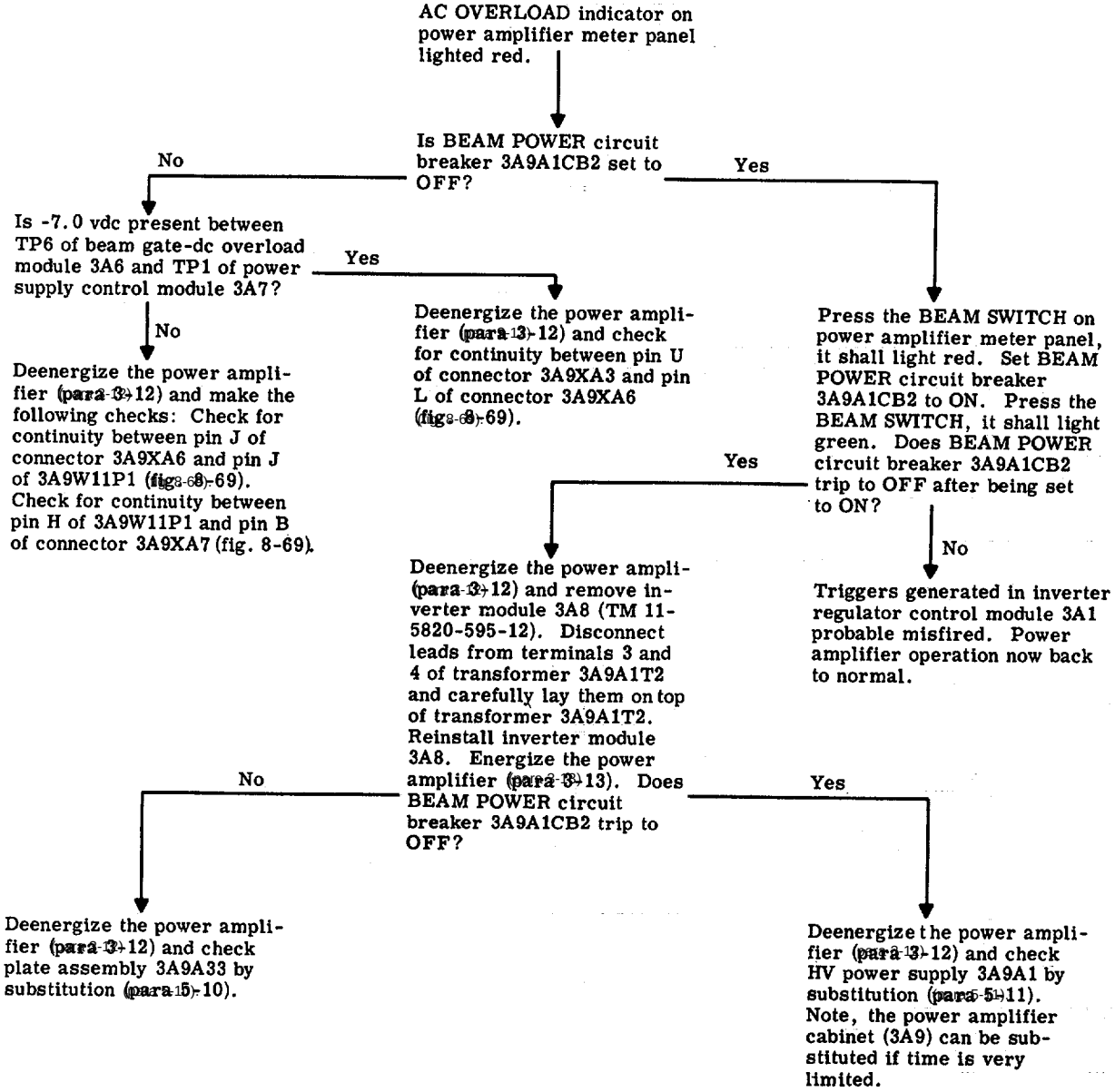
Indication



e. Power Amplifier Flow Charts (cont).

ITEM 10

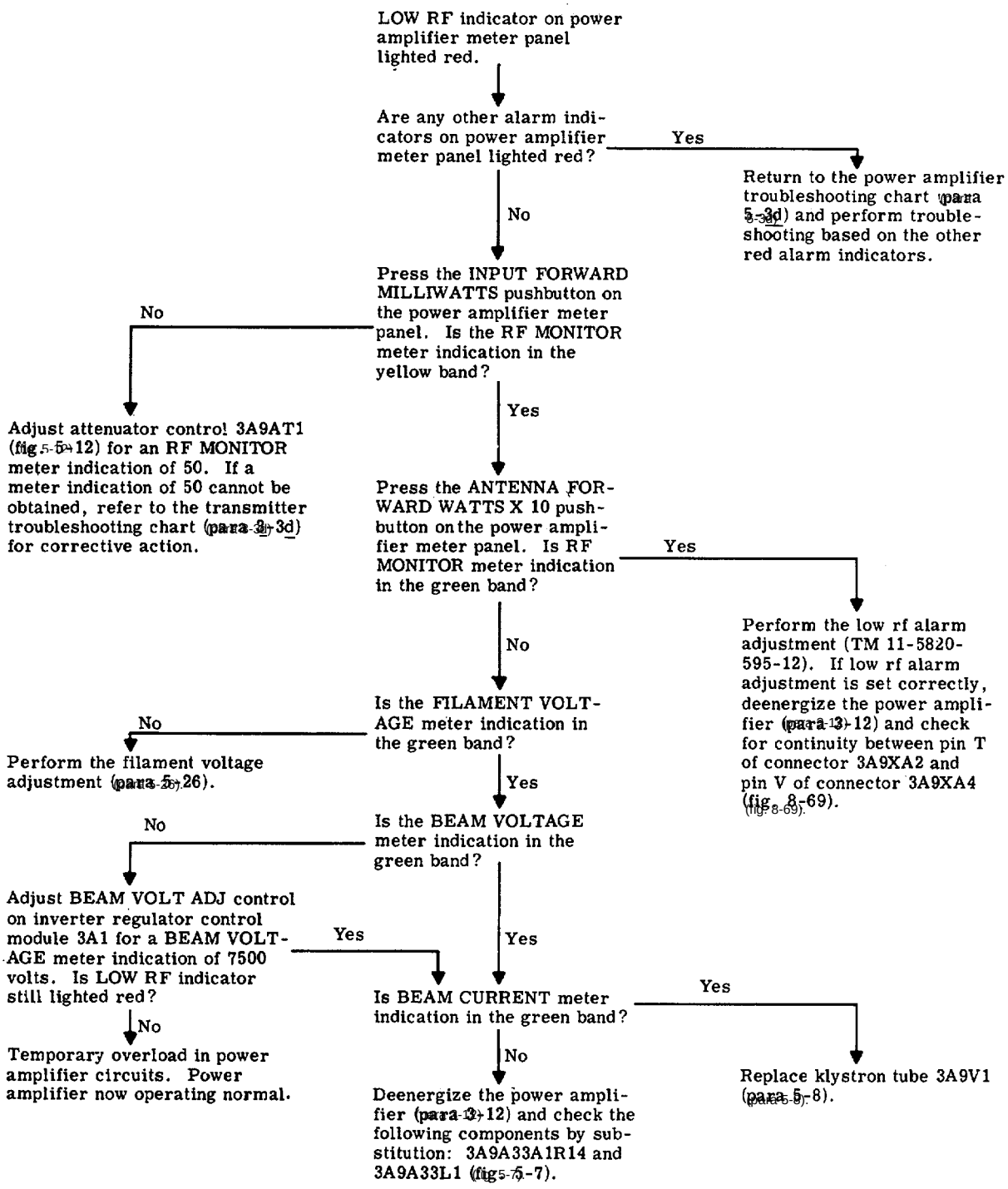
Indication



e. Power Amplifier Flow Charts (cont).

ITEM 11

Indication



e. Power Amplifier Flow Charts (cont).

ITEM 15

Indication

All cabinet fans (3A9A26B2 through 3A9A26B5) not operating.

Is CABINET FANS circuit breaker 3A9A1CB5 set to ON?

Yes → Deenergize the power amplifier (para 3-12) and check for continuity between pin E of 3A9W11P1 and terminal 1 of capacitor 3A9C2 (fig. 8-69).

No → Set CABINET FANS circuit breaker 3A9A1CB5 to ON. Does it trip to OFF after being reset?

No → Momentary overload caused CABINET FANS circuit breaker 3A9A1CB5 to trip. Power amplifier now operating normal.

Yes → Deenergize the power amplifier (para 3-12) and check wiring between terminal board 3A9A26TB1 and each of the cabinet fans (3A9A26B2 through 3A9A26B5) by performing continuity checks (para 5-4). If trouble not located, check for continuity between pin 3 of 3A9A26TB1 and pin 2 of 3A9W11P2 8-69). Also check for continuity between pin 2 of 3A9A26TB1 and pin E of 3A9W11P2. Check capacitor 3A9C2 by substitution. If trouble not located, remove each cabinet fan (3A9A26B2 through 3A9A26B5), one at a time and check its resistance as follows:

T1 to T4 should be 500 ± 100 ohms.
T1 to T5 should be 800 ± 100 ohms.

e. Power Amplifier Flow Charts (cont).

ITEM 17

Indication

FILAMENT VOLTAGE meter indication not in the green band.

Is any alarm indicator on power amplifier meter panel lighted red?

Yes → Return to the power amplifier troubleshooting chart (para 5-3d) and perform troubleshooting based on the red alarm indicator.

No → Is FILAMENT VOLTAGE meter indication approximately zero?

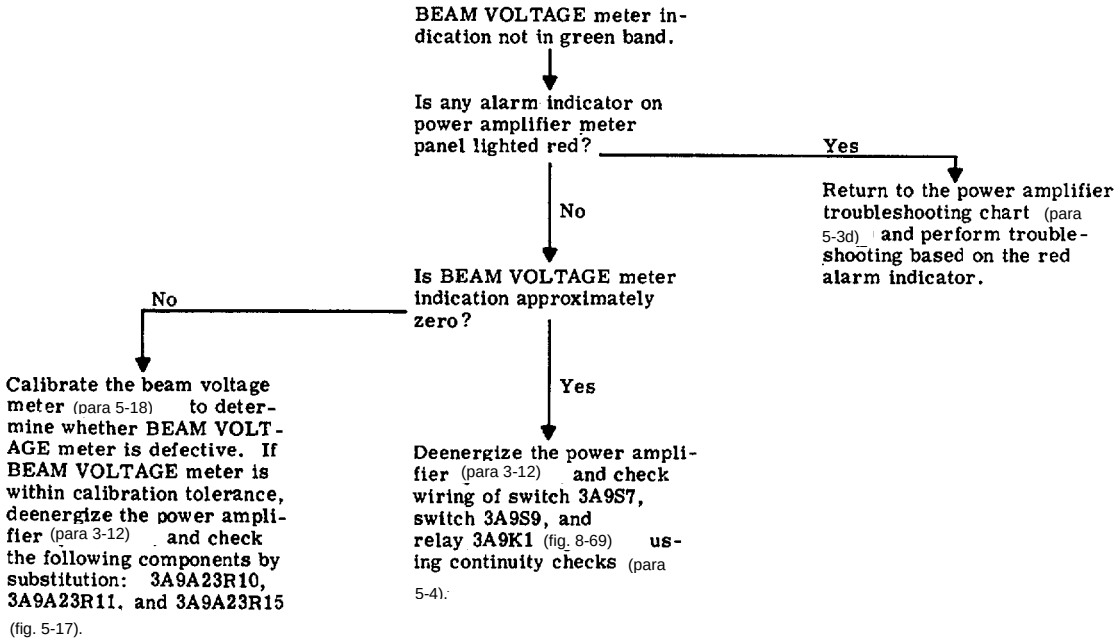
Yes → Calibrate the filament voltage metering circuit (para 5-26) to determine whether the FILAMENT VOLTAGE meter is defective. If FILAMENT VOLTAGE meter is within calibration tolerance, check the following components by substitution: 3A9R5, 3A9R7, 3A9A27CR10, 3A9A28CR11, 3A9R4, 3A9M1, and 3A9T3 (fig. 8-69).

No → Perform the filament voltage adjustment (para 5-26). If filament voltage can not be adjusted for an in-band meter indication, perform the filament voltage metering circuit calibration (para 5-26). If FILAMENT VOLTAGE meter indication is still not in green band, check the following components by substitution: 3A9R5, 3A9R7, 3A9A27CR10, 3A9A28CR11, 3A9R4, 3A9M1, and 3A9T3 (fig. 8-69).

e. Power Amplifier Flow Charts (cont).

ITEM 18

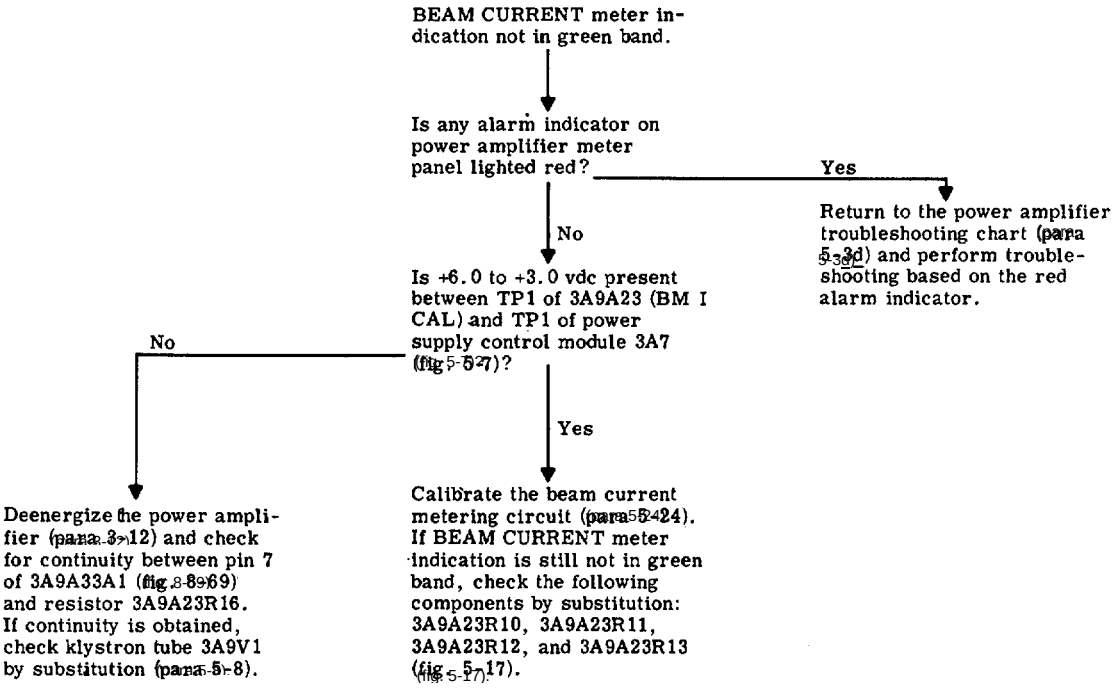
Indication



e. Power Amplifier Flow Charts (cont).

ITEM 19

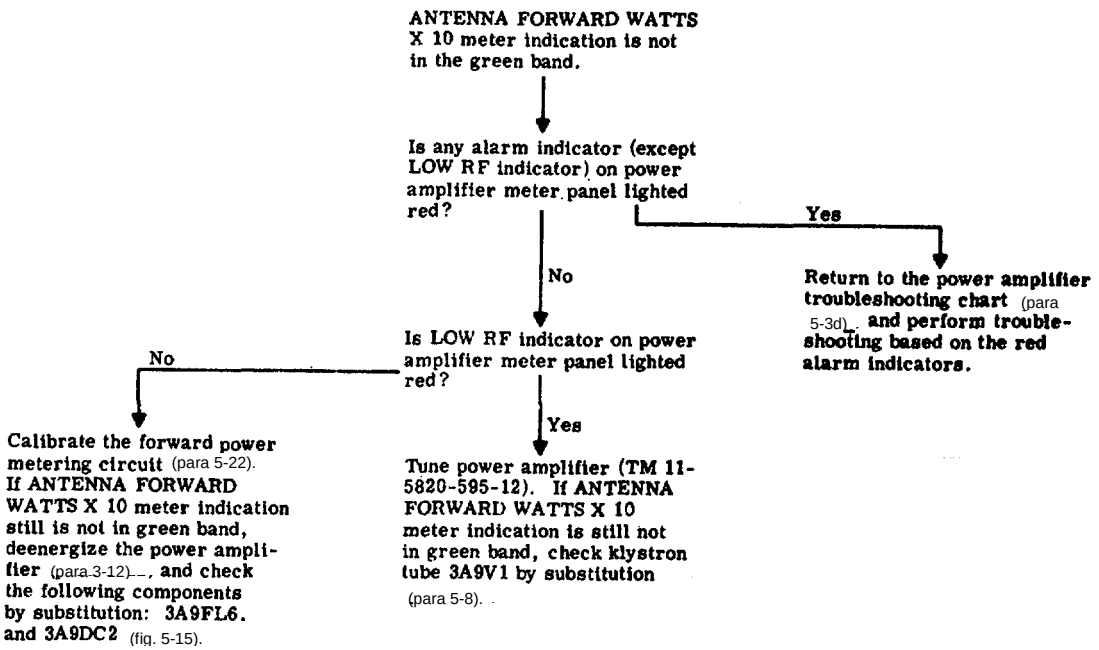
Indication



e. Power Amplifier Flew Charts (cont).

ITEM 21

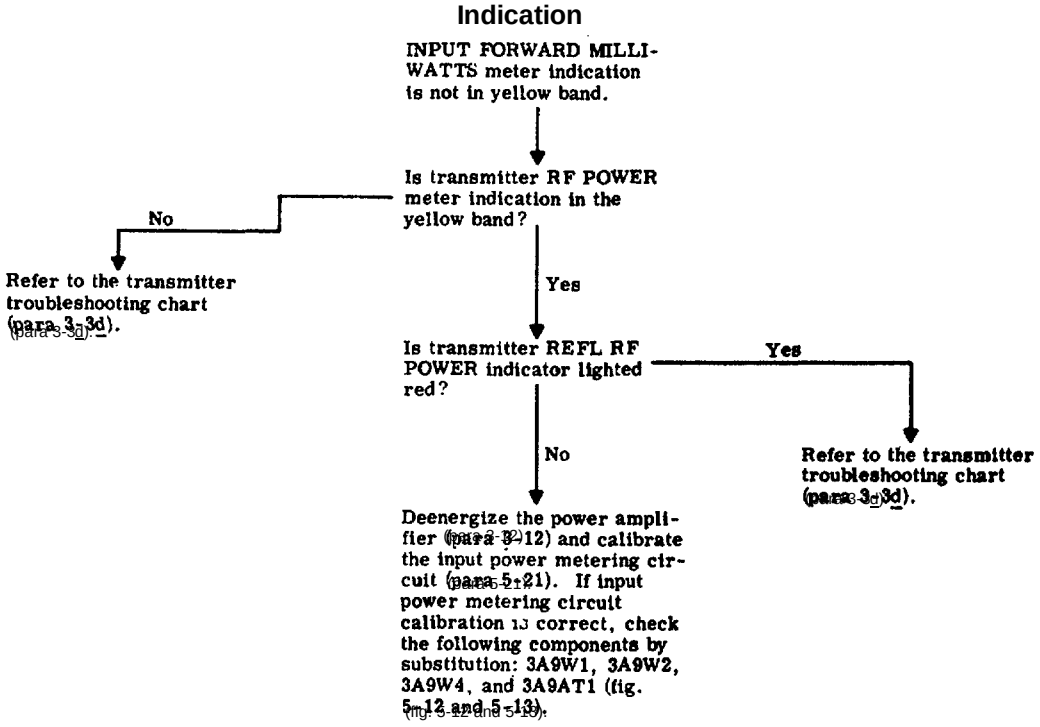
Indication



e. Power Amplifier Flow Charts (cont).

ITEM 23

Indication



5-4. Continuity and Resistance Checks

WARNING
230 vac is present in the power amplifier. Do not perform any continuity or resistance check while the radio set is energized.

To perform any continuity or resistance check given in the power amplifier troubleshooting chart, proceed as follows:

a. Deenergize the power amplifier (para 3-12).

b. Connect the TS-352B/U test leads between the two points given in the troubleshooting chart or flow chart. If wiring must be checked, refer to the figure given in the troubleshooting chart of flow chart and select the first two points to be checked.

c. For continuity checks, observe that the meter indication on TS-352B/U is less than 5 ohms. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

d. For resistance checks, observe that the indication is within the tolerance specified in the troubleshooting chart or flow chart. If it is not, use the interconnecting diagram referenced in the chart to trace and isolate the trouble.

e. After the trouble has been corrected, energize the power amplifier (para 3-13) and check that the corrective action taken has corrected the trouble.

5-4.1. High Voltage Interlock Test (fig. 5-6.1)

a. Deenergize the power amplifier (para 3-12).

b. Open high voltage interlock door.

c. Unplug the white and yellow wires (3A9J5 and 3A9J6).

d. Short the yellow wire to ground with the grounding rod to assure the HV capacitors are discharged.

e. Connect on ohmmeter between the yellow jack and chassis ground. A zero ohm should be observed.

f. If a resistance or open is read S6 contacts must be cleaned (para 5-10). After cleaning and adjustment recheck for continuity.

Section II. POWER AMPLIFIER REPAIRS

5-5. Scope of Power Amplifier Repairs

a. The sequence of events listed below should be followed when replacing any part in the power amplifier to minimize potential personnel hazards and optimize restoring the radio set to an operational state.

(1) Deenergize the radio set.
(2) Part replacement.
(3) Energize radio set.
(4) Performance check.
(5) Confirm radio set operational status.

b. Equipment malfunctions are generally corrected by replacing the known defective item with its equivalent new part. Part replacement, however, does not assure the operational integrity of the radio set and must include performing an operational check. The operational check will confirm correction of the equipment malfunction prior to reestabalishing the radio sets operational status.

c. Procedures for deenergizing the radio set are provided in paragraph 3-12. Detailed procedures for specific part removal are provided in paragraph 5-7 through 5-15. When replacing any part, specific precautions and practices should be observed and are itemized in paragraph 5-6. Procedures for energizing the radio set are provided in paragraph 3-13.

5-6. Power Amplifier Parts Replacement Techniques

The following precautions apply when removing, replacing, or repairing parts in the power amplifier.

a. Tag all hardware and components during removal procedures for correct identification during replacement procedures. Before a part is unsoldered, note the position of the leads. Of the part has several leads, tag each of the leads before unsoldering.

b. When removing a defective part, be careful not to damage leads or other parts by pulling or pushing them out of the way.

c. Whenever replacing a part, install the new part in the same position as the original. Use an exact duplicate whenever possible.

d. If wiring must be replaced, use leads of the same length and gauge if possible. Do not use replacement wire with a higher gauge number (smaller diameter). With the exception of harness cabling, run the leads in the same manner as the original wiring. For harness cabling cut the old conductor as short as possible without removing it from the harness. Dress the new conductor and spot tie it to the outside of the harness. Make connections to the same terminals used in the original wiring, even where there are alternatives which appear electrically equivalent.

e. Make well-soldered connections, using no more solder than is necessary. A carelessly soldered connection may create a new fault and is one of the most difficult faults to find.

f. Do not allow drops of solder to fall into the unit. Do not allow a soldering iron to come into contact with insulation or parts that might be injured by excessive heat.

g. Do not disturb the setting of any uncalibrated control without predetermining its proper setting prior to or reenergizing the radio set.

h. During all handling and use of Klystron 3A9VI keep all magnetic materials (wristwatches) six inches away. Keep all magnets 12 inches away.

5-7. Replacement of Parts on Power Amplifier Meter Panel 3A9
(figs. 5-1 and 5-2)

Prior to removing and replacing parts on the power amplifier meter panel, deenergize the radio set (para 3-12).

a. Removal of Main Power and Beam Light Switch Assemblies 3A9A32 and 3A9A34 (fig. 5%2). Apply same procedures covered in paragraph 3%15%.

b. Replacement of Main Power and Beam Light Switch Assemblies 3A9A32 and 3A9A34 (fig. 5.2).

(1) Apply the same procedures covered in paragraph 3-15d (1) through (12).

(2) Check that the replace light switch assemblies indicate as follows:

Name of indicator	*Indication*
MAIN POWER SWITCH (3A9A32)	White or green; depress MAIN POWER SWITCH and note that indication has changed
BEAM SWITCH (3A9A34)	Read or white; depress BEAM SWITCH and note that indication has changed.

c. Removal of Light Indicator Assemblies 3A9XDS9, 3A9XDS13, 3A9XDS17, 3A9XDS21, 3A9XDS25, 3A9XDS29, 3A9XDS33, 3A9XDS37

and SA9XDS41 (fig. 3-6, 5-1, and 5-2). Apply the same procedures covered in paragraph 3-15c.

d. Replacement of Light Indicator Assemblies 3A9XDS9, 3A9XDS17, 3A9XDS21, 3A9XDS25, A9XDS29, 3A9XDSSS33, 3A9XDS37 and 3A9XDS41 (fig. 3-6, 5-1, and 5-2).

(1) Apply the same procedures covered in paragraph 3-15d(1) through (12).

(2) Check that the replaced light assemblies indicate as follows:

Name of Indicator	Indication
AIR (3A9XDS9)	Green
FILAMENT (3A9XDS13)	Green
BEAM (3A9XDS21)	Red
LOW RF (3A9XDS21)	Red
TIME DELAY (3A9XDS25)	Amber-Turns green after 3 or 4 minutes
AC INTERLOCK (3A9XDS29)	Red
AC OVERLOAD (3A9XDS33)	Green
DC OVERLOAD (3A9XDS37)	Green
ANTENNA MISMATCH (3A9XDS41)	Green

e. Removal of FILAMENT RUNNING TIME Indicator 3A9M1 (fig. 5-1 and 5-2).

(1) Loosen the two meter panel captive screws (fig. 5-1) and lock the meter panel in an upright position with the meter panel locking latch.

(2) Slide the 3A9M1 cover (fig. 5-2) away from the terminal connections.

(3) Tag and unsolder wires connected to indicator 3A9M1 terminals.

(4) Release the meter panel locking latch, position the meter panel downward, and remove the two screws (fig. 5-1) on the front of indicator 3A9M1 and the two nuts (fig. 5-2) located at rear of indicator 3A9M1. Remove indicator 3A9M1.

f. Replacement of FILAMENT RUNNING TIME Indicator 3A9M1(fig. 5-1 and 5-2).

(1) Insert replacement indicator 3A9M1 into position on the front of the meter panel (fig. 5-1) and secure into place with the two screws and nuts removed in e(4) above.

(2) Solder wires, removed in e(3) above, to indicator 3A9M1 terminals.

(3) Reposition plastic cover over rear of indicator 3A9M1.

(4) Finger tighten the two meter panel captive screws securing the meter panel to power amplifier cabinet 3A9.

(5) Energize the radio set as described in paragraph 3-13.

(6) Check the operation of the replaced indicator 3A9M1 by observing that hours and tenths of hours are registering during use.

g, Removal. of RF MONITOR SELECT Selector Switch 3A9S8 (fig. 5-1 and 5-2).

(1) Pull the three pushbutton knobs (fig. 5-1) off the front of selector switch 3A9S8 (fig. 5-2). Note the color positions for replacement purposes.

(2) Loosen the two meter panel captive screws (fig. 5-1) and lock the meter panel in an upright position with the meter panel locking latch.

(3) Tag and unsolder the wires connected to selector switch 3A9S8 (fig. 5-2) terminals.

(4) Release the meter panel downward and remove the two screws, washers, standoffs, and nuts that secure selector switch 3A9S8 to the meter panel. Remove the selector switch 3A9S8.

h. Replacement of RF MONITOR SELECT Selector Switch 3A9S8 (fig. 5-1 and 5-2).

(1) Position replacement selector switch 3A9S8 on back of meter panel and secure the switch with the two screws, washers, and standoffs removed in *g* (4) above.

(2) Lock the meter panel in an upright position and solder all wires, removed in g (3) above, to selector switch terminals.

(3) Release the meter panel downward, and finger tighten the two meter panel captive screws.

(4) Replace the three pushbutton knobs, removed in g (1) above.

(5) Check the operation of the replaced selector switch 3A9S8 by performing the power amplifier tuning procedure (TM 11-5820-595-12).

5-8. Replacement of Parts on Magnet Support 3A9A7

(fig. 5-1, 5-4, and 5-5)

Caution: During all handling and use of klystron A9V1 keep all magnetic materials (eg, wristwatches) six inches away. Keep all magnets 12 inches away.

a. Removal of Magnet Support 3A9A7 from Power Amplifier Cabinet 3A9.

(1) Deenergize the radio set (para 3-12).

(2) Loosen captive screw on high voltage interlock door (fig. 5-1) and lower the door.

(3) Unplug filament cables 3A9P3 and 3A9P4 from 3A9J5 and 3A9J6 located behind high voltage interlock door (fig. 5-4).

(4) Loosen the hose clamp securing tuner cooling hose to klystron tube 3A9V1, and disconnect tuner cooling hose from klystron tube 3A9V1.

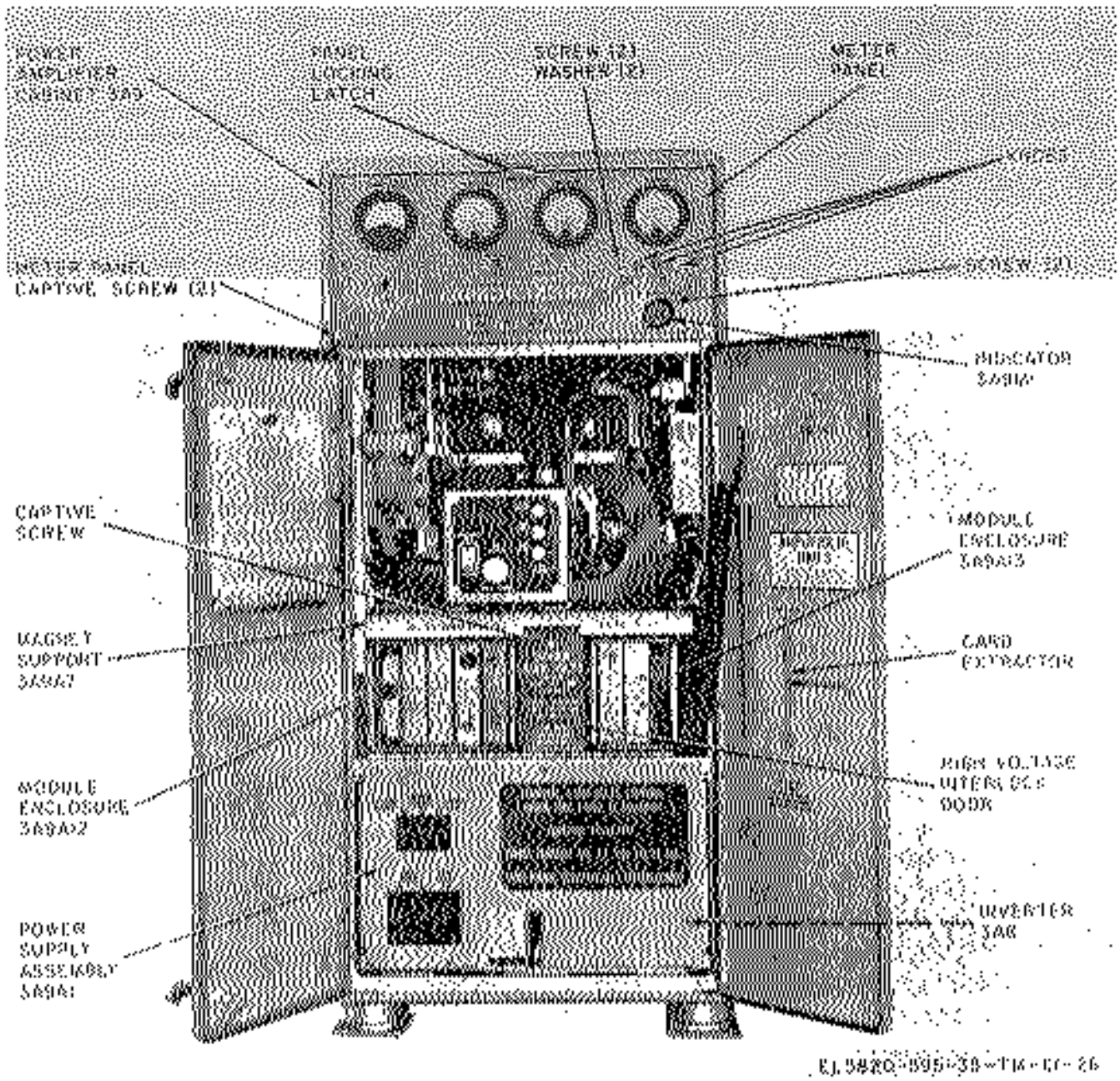


Figure 5-1. Power amplifier front view with cabinet doors open, parts location.

(5) Loosen the duct clamp securing klystron collector duct to the blower assembly 3A9B1 and. disconnect klystron collector duct from blower assembly 3A9B1.

(6) Tag and disconnect the lugs four wires connected to terminal board 3A9VlTBl. Remove the cable clamp securing the four wires to magnet support 3A9A7.

(7) Release the quick disconnect clamp securing flexible Waveguide 3A9W5 to the Waveguide output connector 3A9V1P2 by pulling the quick disconnect clamp up and forward.

(8) Remove four bolts and washers that secure magnet support 3A9A7 to power amplifier cabinet 3A9. Two of the bolts are located on the magnet support guide rails.:

(9) Partially slide magnet support 3A9A7 out of power amplifier cabinet 3A9 and discon

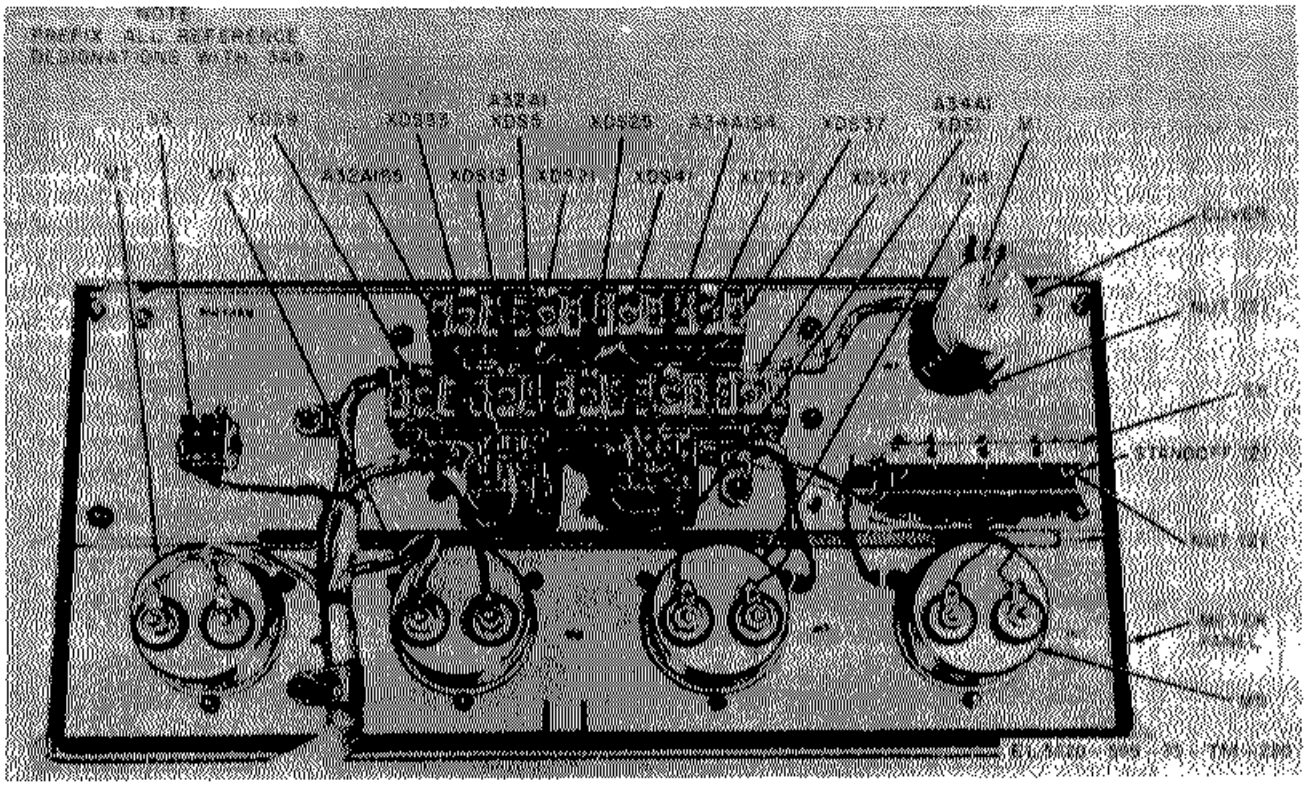


Figure 5-2. Power amplifier meter panel (part SA9), rear view, parts location.

nect coaxial cable 3A9W4 (terminating with type N connector) from RF input connector 3A9VIP1 (fig. 5-5). Slide magnet support 3A9A7 out of power amplifier cabinet 3A9 until the detent spring locks (located on both sides of the magnet support slide rails) are engaged in their lock positions.

(10) Loosen the duct clamp and disconnect the klystron collector duct from klystron 3A9V1.

CAUTION

The magnet support 3A9A7 must be placed on blocks to prevent damage to its protruding filament cables located on the bottom portion of magnet support 3A9A7.

(11) Release detent spring locks (located on both magnet support slide rails (fig. 5-4)) by pushing the detent spring locks inward and remove the magnet support 3A9A7 from power amplifier cabinet 3A9.

b. Removal of Klystron Tube 3A9V1 (fig. 5-5).

(1) Loosen the four frequency tuner mounting screws and slide frequency tuner 3A9A6 toward the right side of magnet support 3A9A7 until the sprocket chain is loose. Remove the sprocket chain from the miniature sprocket gear.

(2) Loosen the two set screws securing each fine tuning shaft (three) to klystron cavity tuning shafts and pull fine tuning shafts off of klystron cavity tuning shaft.

(3) Remove the four klystron tube mounting bolts, nuts, and associated hardware securing klystron tube to magnet support.

(4) Remove klystron 3A9V1 from magnet support 3A9A7 using care that klystron filament cables do not catch on magnet support.

c. Replacement of KLYSTRON Tube 3A9V1.

(1) Feed filament cables 3A9P3 and 3A9P4 on replacement klystron 3A9V1 through filament access, hole on magnet support 3A9A7, and position replacement klystron tube on magnet support 3A9A7.

(2) Replace and tighten the four klystron mounting bolts, nuts, and associated hardware securing klystron tube to magnet support 3A9A7.

(3) Connect the three fine tuning shafts to the klystron cavity tuning shafts. Secure the

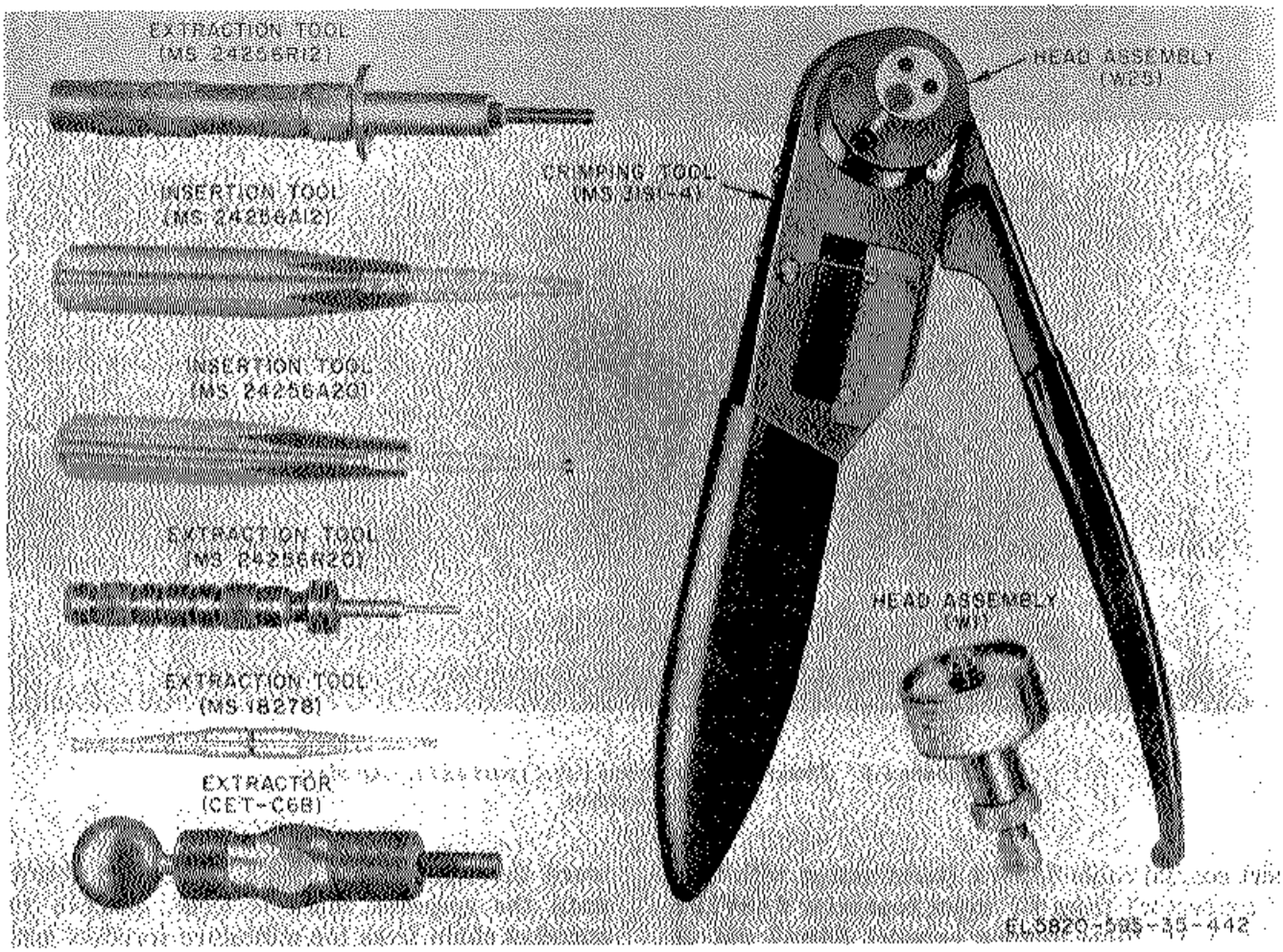


Figure 5-3. Crimping, extraction, and insertion tools.

shafts by tightening the two set screws on each fine tuning shaft.

(4) Connect the sprocket chain to the miniature sprocket gear.

(5) Slide frequency tuner 3A9A6 toward left side of magnet support 3A9A7 until sprocket chain is taut, then tighten the four frequency tuner mounting screws securing frequency tuner to magnet support 3A9A7.

(6) Connect klystron collector duct removed in step a(10) to klystron 3A9V1 and tighten duct clamp.

(7) Replace the magnet support 3A9A7 into the power amplifier cabinet (para 5-8f).

(8) Energize the radio set (para 3-13).

(9) Perform the power amplifier frequency tuner drum dial readout calibration procedure (para 5-23).

d. Removal of Frequency Tuner 3A9A6 (fig. 5-5).

(1) Partially slide magnet support 3A9A7 out of power amplifier cabinet (para 5-a(l) through (9)). Loosen the two set screws securing the 2nd, 3rd, and 4th CAVITY FINE TUNING knobs on frequency tuner 3A9A6, and remove the knobs.

(2) Remove the four frequency tuner mounting screws and washers securing the frequency tuner 3A9A6 to magnet support 3A9A7.

(3) Slide frequency tuner 3A9A6 toward the right side of magnet support 3A9A7 and remove the sprocket chain from the miniature sprocket gear.

(4) Carefully withdraw frequency tuner 3A9A6 from magnet support 3A9A7.

e. Replacement of Frequency Tuner 3A9A6.

(1) Carefully position the replacement frequency tuner 3A9A6 on the magnet support 3A9A7 (fig. 5-5) and guide the three fine tuning shafts through the chassis bushings.

(2) Connect the sprocket chain to the miniature sprocket.

(3) Slide the tuner toward the left side of magnet support until the sprocket chain is taut. Replace and tighten the four frequency tuner mounting screws removed in step d (2) above.

(4) Insert 2nd, 3rd, and 4th CAVITY FINE TUNING control knobs on the fine tuning shafts and tighten the two set screws on each control knob.

(5) Check the operation of the frequency tuner 3A9A6 as follows: (a) Visually check to 'see that all gears are meshed with their associated gears.

(b) Check for binding.

(6) Reassemble magnet support 3A9A7 into the power amplifier cabinet 3A9 as described in paragraph 5-8f and perform the power amplifier frequency tuner drum dial readout calibration (para 5-23).

f. Replace)lent of Magnet Support 3A9A7 into Poive Amplifies Cabinet 3A9 (fig. 5-4).

(1) Check that the quick disconnect clamp is in the fully released position (quick disconnect clamp handle should be facing away from klystron 3A9V1).

(2) Extend magnet support slide rails (fig. 5-4) located within power amplifier cabinet 3A9 until they lock in their most extended position.

(3) Lift magnet support 3A9A7 and carefully insert the magnet support guide rails (fig. 5-5) into the magnet support slide rails until detent springs lock into position.

(4) Release detent spring locks (located on the outer side of the magnetic support guide rails) and carefully slide magnet support 3A9A7 partially into power amplifier cabinet 3A9.

(5) Connect coaxial cable 3A9W4 (type N connector) to RF input connector 3A9V1P1 located on rear portion of klystron tube 3A9V1.

(6) Care should be taken to guide the two filament cables 3A9P3 (yellow) and 3A9P4 (white) into their proper plug positions 3A9J5 and 3A9J6 located in the high voltage interlock compartment while slowly sliding magnet support 3A9A7 into the power amplifier cabinet 3A9 until waveguide output connector 3A9V1P2 and input flange of the flexible waveguide 3A9W5'are flush mounted to each. other. Then secure the waveguide output connector 3A9V1P2 to flexible waveguide 3A9W5 by pulling the quick disconnect clamp handle toward the klystron 3A9V1.

(7) Connect the yellow filament cable 3A9P3 to the yellow porcelain receptacle 3A9J5 and the white filament cable to the white porcelain receptacle 3A9J6.

(8) Reconnect the four tagged wires removed in step a (6) above and secure the cable clamp.

(9) Connect klystron collector duct to blower assembly 3A9B1 and tighten duct clamp.

(10) Connect tuner cooling hose to klystron and secure in place with the hose clamp.

NOTE

One of the four bolts is shorter than the remaining three in step (11) below and must be inserted in the front left mounting hole of the magnet support.

(11) Secure the magnet support 3A9A7 to the power amplifier cabinet 3A9 with the four bolts and washers removed in step a (8).

(12) Close high voltage interlock door and secure with captive screw.

5-9. Replacement of Module Enclosures 3A9A12 and 3A9A13 (fig. 5-1 and 5-6)

a. Removal of Module Enclosure 3A9A12 and 3A9A13.

(1) Deenergize the radio set (para 3-12).

(2) Remove inverter module 3A8 (TM 11-5820-595-12).

(3) Remove magnet support 3A9A7 (para 5-8a).

(4) Remove plug-in modules 3A1 through 3A7 (TM 11-5820-595-12).

(5) Remove four bolts (two rear bolts each certain a washer) securing each module enclosure 3A9A12 and 3A9A13 to front and rear module enclosure mounting brackets.

(6) Remove harness from trough located on the right side of module enclosure 3A9A13. Lift module enclosure 3A9A13 approximately ½l/-inch from the module enclosure mounting brackets. Carefully pull out module enclosure 3A9A13 from power amplifier cabinet 3A9 noting the positions of removed and loose hardware. During the removal of module enclosure 3A9A13 care should also be taken to prevent the flat shim and cable guide (located under the front portion of module

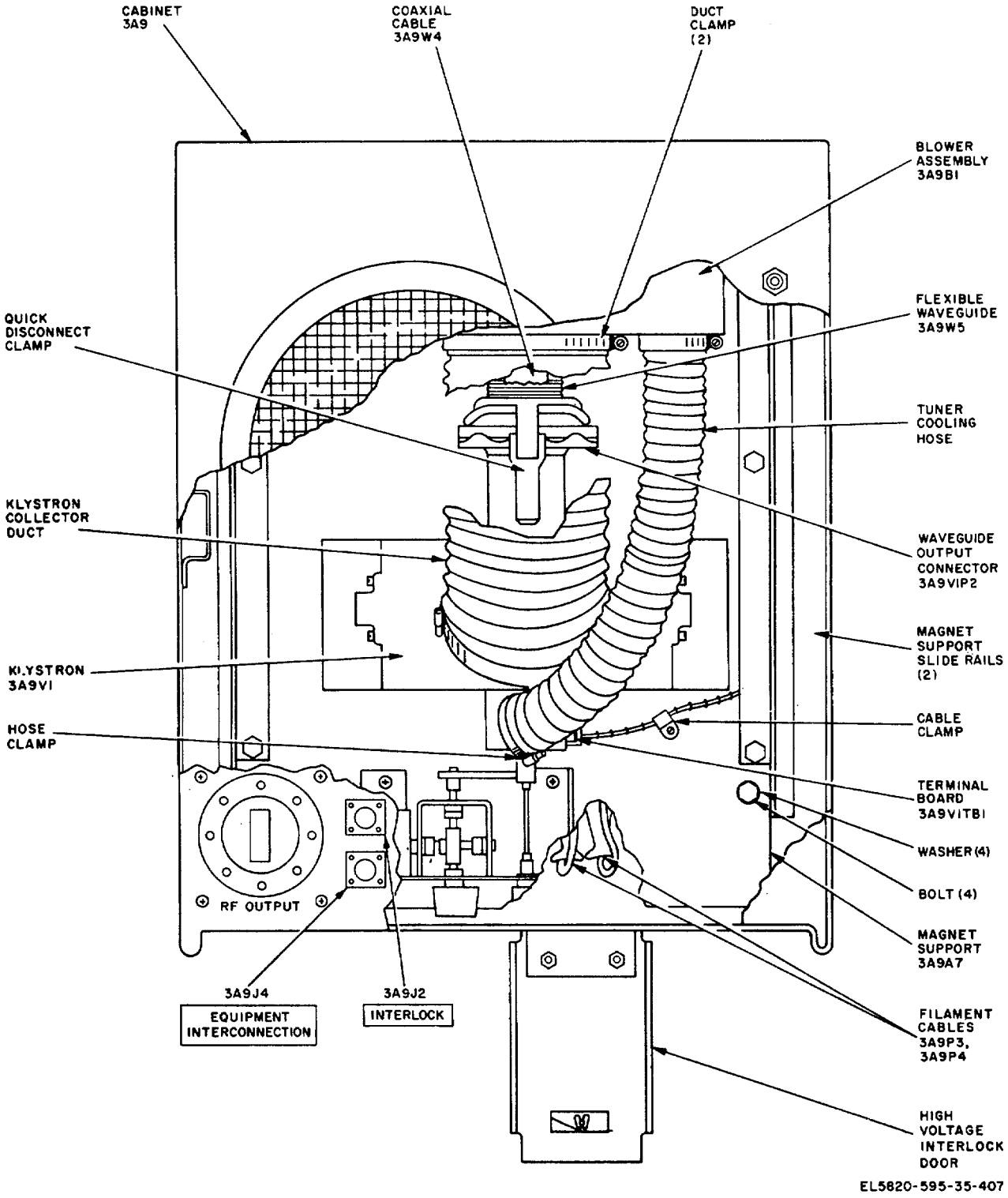


Figure 5-4. Magnet support SA9A7 with mounted components 3A9V1 and 3A9A6, cutaway, top view.

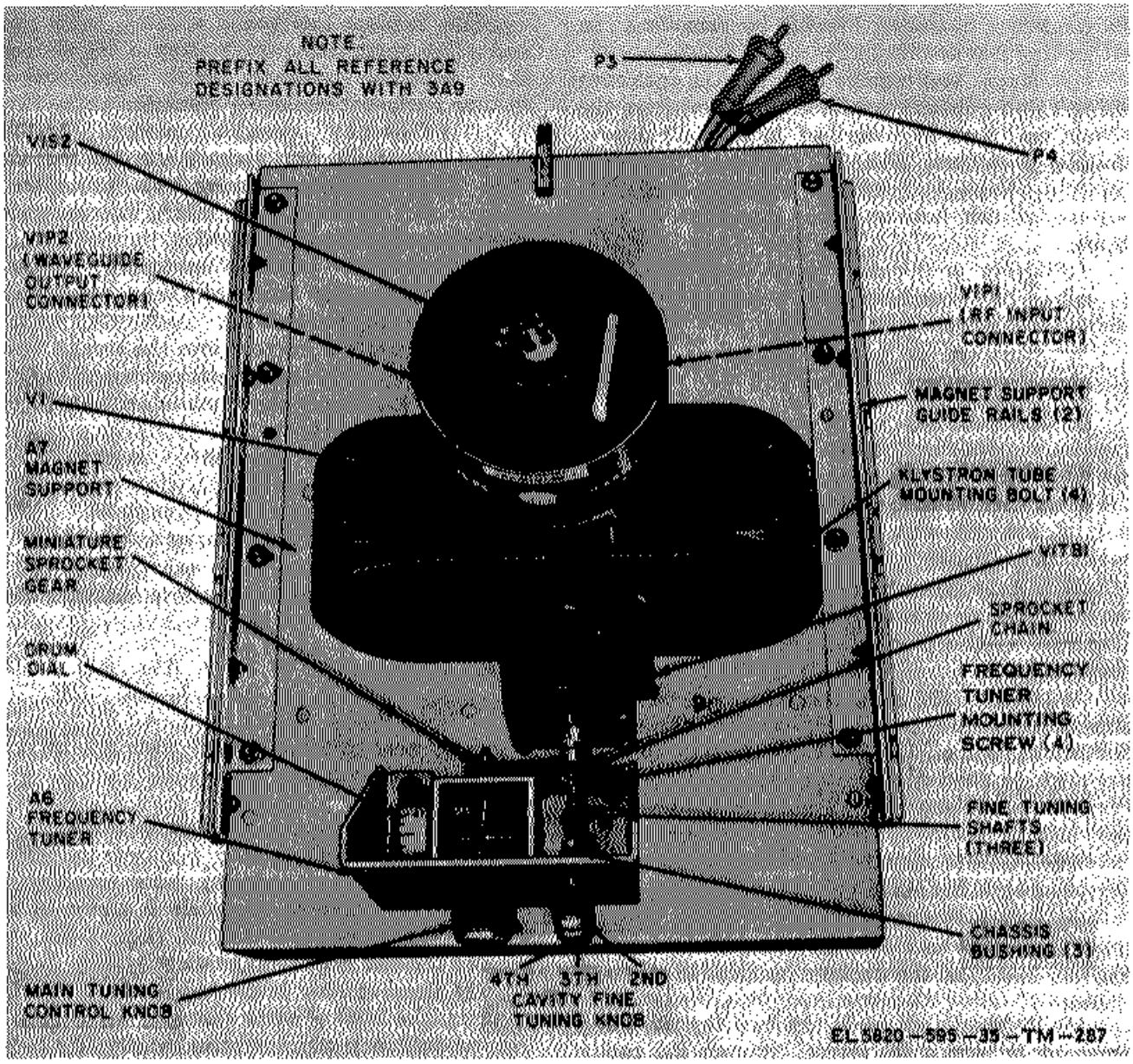


Figure 5-5. Magnet support 3A9A7, top view, parts location.

enclosure 3A9A13 between the enclosure and its mounting bracket) and the two round spacers (located under the rear portion of module enclosure 3A9A13 between the enclosure and its mounting bracket) from dropping into the bottom of power amplifier cabinet 3A9.

(7) Remove two screws (rear) and two lock nuts (front) securing the connector mounting bracket to the front and rear module enclosure mounting brackets.

(8) Tag and unsolder two wires connected to interlock switch 3A9S6.

(9) Remove self locking nut securing wire support clamp to interlock switch 3A9S6 and remove wire support clamp from wires.

(10) Tag filament wires connected to receptacles 3A9J5 and 3A9J6. Remove nuts, washers and lockwashers securing the lug terminated filament wires to receptacles 3A9J5 and 3A9J6 and disconnect filament wires.

(11) Pull the two wire, removed in step (8) above, through the rubber grommet (mounted in the rear of the connector mounting bracket) and removed the wire support clamp from underneath the connector mounting bracket by removing the self-locking nut securing it.

(12) Grasp and remove both module enclosure 3A9A12 and connector mounting bracket from the module enclosure as described in step (6) above.

Module enclosure 3A9A12 and the connector mounting bracket must be removed together because of the harness cable connected to both items.

(13) Note positions of loose hardware, consisting of two round spacers, a flat shim and a cable guide. Remove the hardware.

b. Reassembly of Module Enclosures 3A9A12 and 3A9A13 (fig. 5.1 and 5.6).

(1) Position both module enclosure 3A9A12 and connector mounting bracket on the front and rear module enclosure mounting brackets noting that the grounding switch rod must align with and go through the connector mounting bracket insulator hole.

(2) Lift the grounding switch rod and reposition the connector mounting bracket so that the grounding switch rod is placed through the hole in the insulator.

(3) During this step, care must be taken to prevent any hardware from falling into bottom portion of the cabinet. Lift module enclosure 3A9A12 and position the two spacers, cable guide and flat shim (remove in step a (13) above) on the front and rear module enclosure mounting brackets. Then carefully position module enclosure 3A9A12 onto the spacers and flat shim.

(4) Secure module enclosure 3A9A12 to front and rear module enclosure mounting brackets using the four bolts and the washers removed in step a (5) above.

(5) Redress and guide the two tagged wires, removed in step a (8) above, through the rubber grommet mounted on the connector mounting bracket and to their respective terminals on interlock switch 3A9S6.

(6) Replace the two wire support clamps which were removed in steps a (9) and a (11) above.

(7) Solder the wires (step (5) above) to interlock switch 3A9S6.

(8) Position the connector mounting bracket and secure in place using the two screws (rear) and two lock nuts (front) removed in step a (7) above.

(9) Replace the two tagged lug terminated filament wires removed in step a (10) above to receptacles 3A9J5 and 3A9J6 and secure with nuts, washers and lockwashers.

(10) Replace two round spacers, cable guide, and flat shim (removed in step a (6) above) to their respective positions on the front and rear module enclosure mounting brackets.

(11) Carefully position module enclosure 3A9A13 over the two spacers and the flat shim. Care must be taken during this procedure to prevent the hardware from falling into the bottom of power amplifier cabinet 3A9.

(12) Secure module enclosure mounting brackets using the four bolts and two washers removed in step a (5) above.

(13) Dress the harness into the trough located on the right side of module enclosure 3A9A13.

(14) Replace plug-in modules 3A1 through 3A7 (TM 11,-820-695-12).

(15) Replace inverter module 3A8 (TM 11-5820-595-12).

(16) Replace magnet support 3A9A7 (para 5-8 f, as described in paragraph 5-8f).

(17) Energize the radio set (para 3-13) and perform operator status and alarm indicator checks (TM 11-5820495-12).

5-10. Replacement of Plate Assembly 3A9A33 (fig. 5-7, 5-7.1, 5-12, 5-14, and 7-56)

NOTE

Replacement to figure 5-7 also applies to figure 5-7.1.

a. Removal.

(1) Remove module enclosures 3A9A12 and 3A9A13 (para 5-9a).

(2) Loosen two coupling nuts securing two high voltage wires to terminals 3 and 4 of high voltage transformer 3A9A1T2 (fig. 7-68), tag, remove the two high voltage wires.

(3) Remove four bolts and washers (fig. 5-7) securing the front of plate assembly 3A9A33 to the rear module enclosure mounting bracket (fig. 5-14).

(4) Remove two screws, lockwashers, and flat washers (fig. 5-7) securing component board assembly 3A9A33A1 to the two front standoffs on plate assembly 3A9A33.

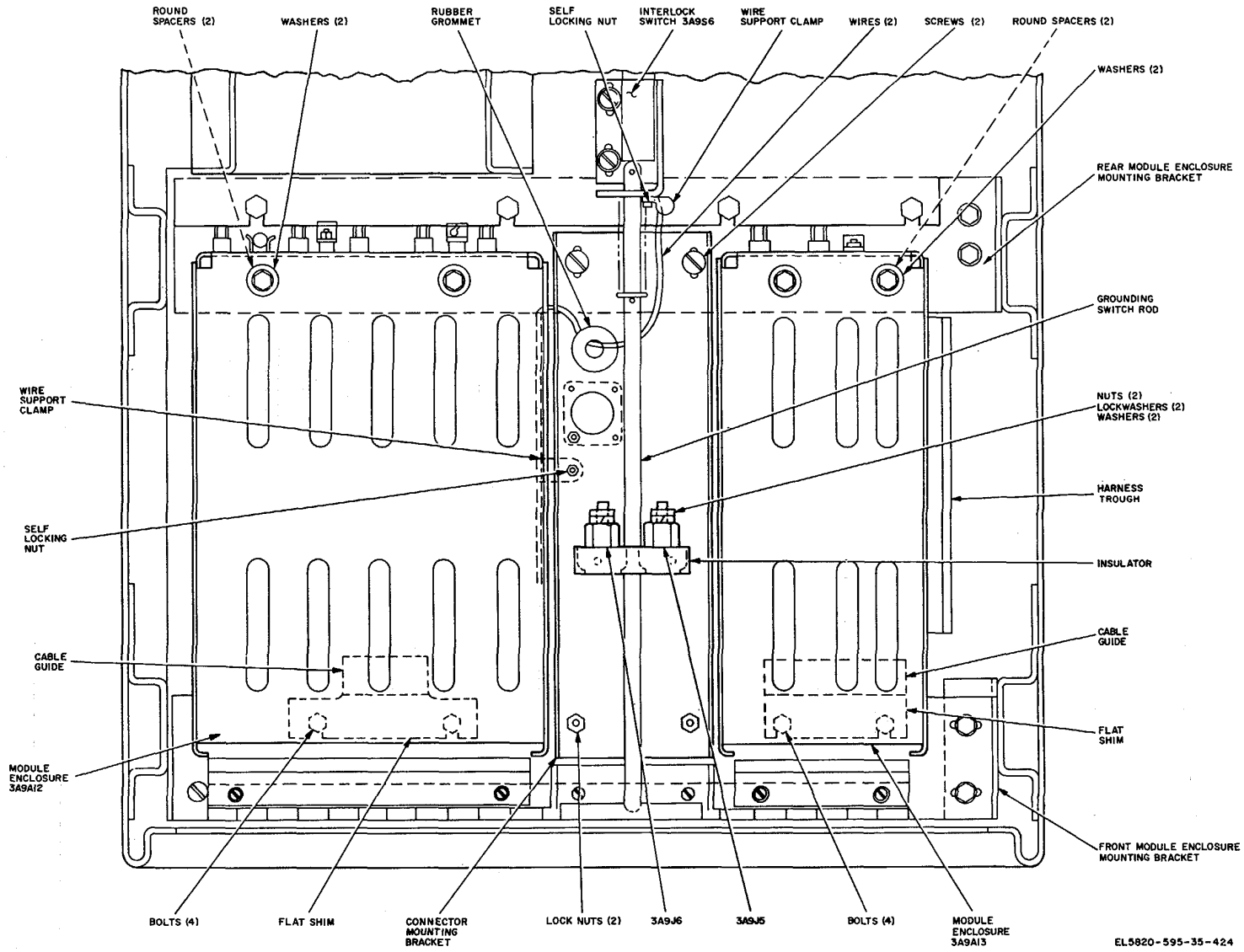


Figure 5-6. Module enclosures 3A9A12 and 3A9A13 mounted in power amplifier cabinet 3A 9 top view.

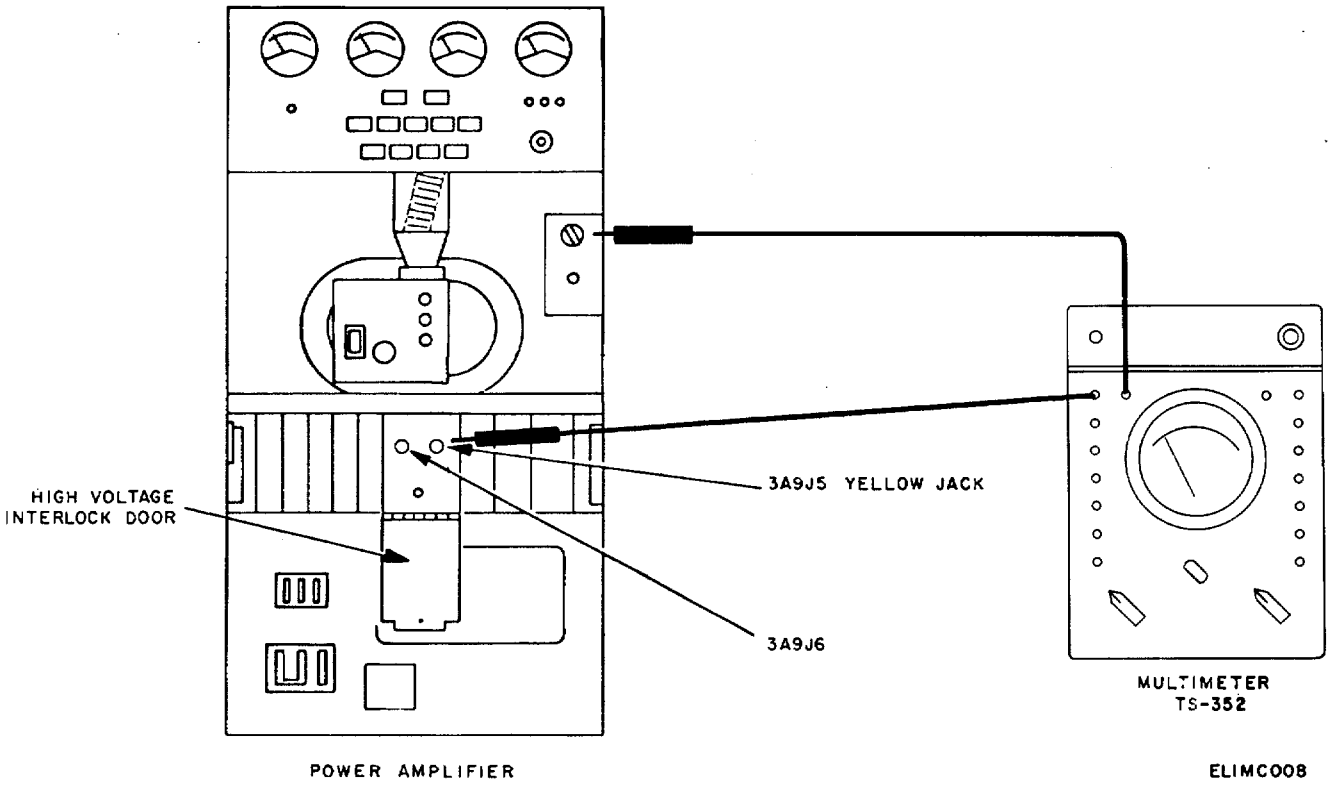


Figure 5-6.1 High Voltage Interlock Test.

(5) Loosen the two captive screws securing component board assembly 3A9A33A1 to the two rear standoffs on plate assembly 3A9A33.

(6) Remove two screws from clamp (fig. 5-12) that secures flexible waveguide 3A9W5 to rear cabinet wall and position 3A9W5 in an upward direction, away from plate assembly 3A9A33.

(7) Tag and unsolder three wires connected to resistor 3A9A33A1R14 (fig. 5-7).

(8) Tag leads and remove nut that secures the two terminal lugs to 3A9A33AlE1 and E2 on component board assembly 3A9A33A1 and disconnect lugs.

(9) Tag and remove component board assembly 3A9A33A1 ground lead from 3A9MP4 (fig. 5-12).

(10) Using a 3/8 inch socket wrench, remove three bolts (fig. 56-7) securing rear section of plate assembly 3A9A33 to the cross support at the rear of power amplifier cabinet 3A9. Component board assembly 3A9A33A1 must be tilted to gain access to the bolt at rear right corner of plate assembly 3A9A33.

(11) Slowly work plate assembly 3A9A33 out of power amplifier cabinet 3A9.

(12) Remove two screws and lockwashers securing interlock switch assemble 3A9S6 to plate assembly 3A9A33. Remove interlock switch assembly 3A9S6 from plate assembly 3A9A33 and store it in a safe place.

b. Replacement.

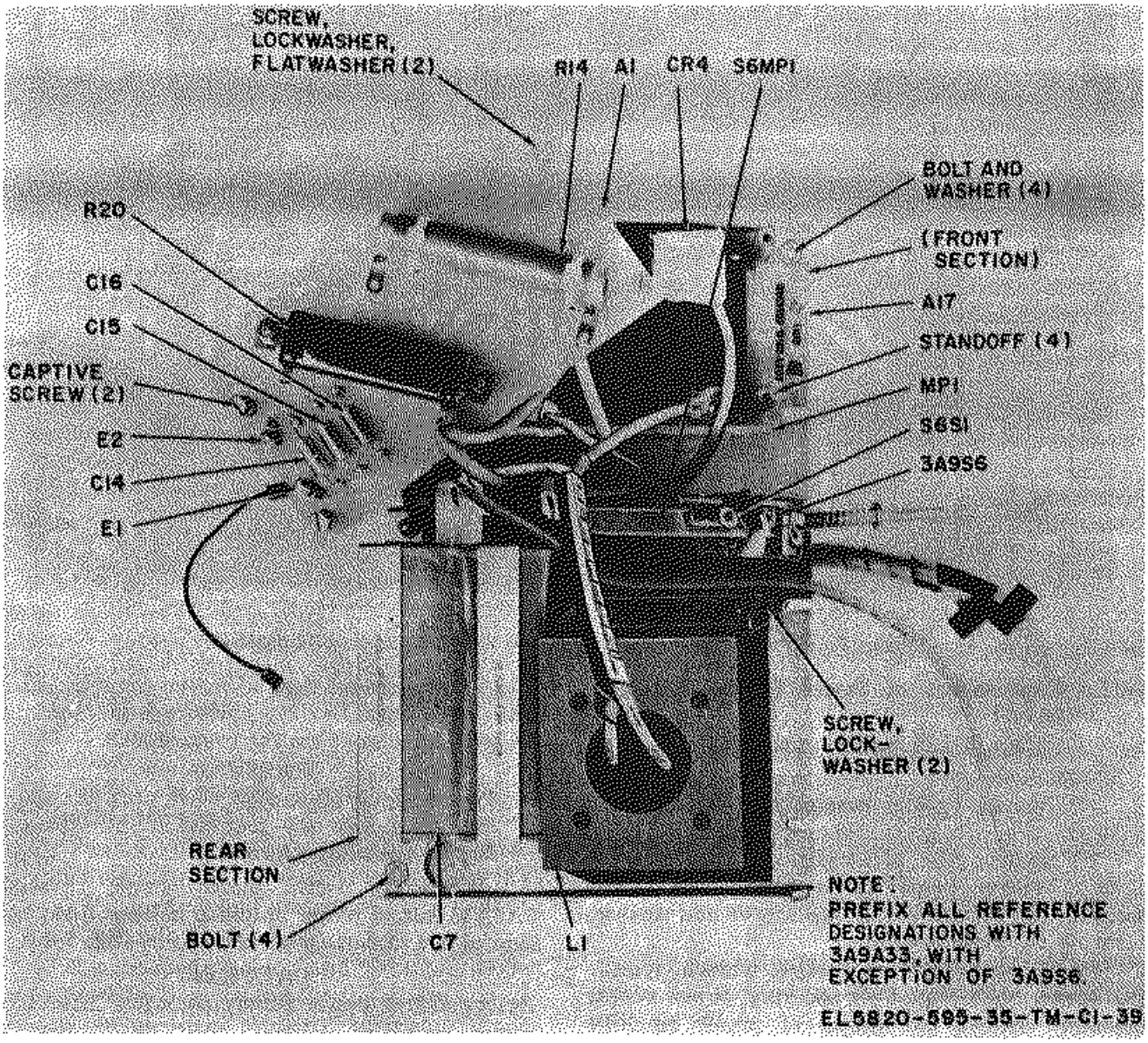
(1) Using the two screws and lockwashers removed in step a (12) above, secure interlock switch assembly 3A9S6 (fig. 5-7) in place on replacement plate assembly 3A9A33.

(2) Remove two screws, lockwashers, and flat washers securing component board assembly 3A9A33A1 to two front section standoffs of replacement plate assembly 3A9A33.

(3) Loosen two captive screws securing component board assembly 3A9A33A1 to the rear two standoffs.

(4) Carefully insert replacement plate assembly 3A9A33 into power amplifier cabinet 3A9 making certain that four holes in rear module enclosure mounting bracket (fig. 5-14) line up with the four holes on the front section of plate assembly 3A9A33 (fig. 5-7).

(5) Tilt component board assembly 3A9A33A1 to gain access to the mounting holes at the rear right corner of plate assembly 3A9A33 and secure 3A9A33 using the bolt removed in step a(10) above (6) Replace and tighten the two remaining



bolts which were removed in step a(10) above.

(7) Solder the three tagged wires removed in step a (7) above, to resistor 3A9A33AlR14.

(8) Replace the two terminal lugs on 3A9A33AlE1 and E2 and secure with nut removed in step a (8) above.

(9) Connect ground lead to 3A9MP4.

(10) Position component board assembly 3A9A33A1 on the four standoffs and secure in place with two captive screws loosened in step a (5) above.

(11) Replace and tighten four bolts and washers removed in step a (3) above to secure the front of plate assembly 3A9A33.

(12) Connect the two high voltage wires, removed in step a (2) above, to terminals 3 and 4 of transformer 3A9A1T2.

(13) Position flexible waveguide 3A9W5 (fig. 5-12) in downward direction (towards plate assembly 3A9A33) and secure with clamp to rear cabinet wall using two screws removed on step a (6) above.

(14) Replace module enclosures 3A9A12 and 3A9A13 as described in paragraph 5-9b (1) through (15).

(15) Replace magnet support 3A9A7 (para 5f).

(16) Energize the radio set (para 3-13). Perform the operator status and alarm indicator checks (TM 11-5820-95-12).

Figure 5-7. Plate assembly 3A9A33, top view, parts location.

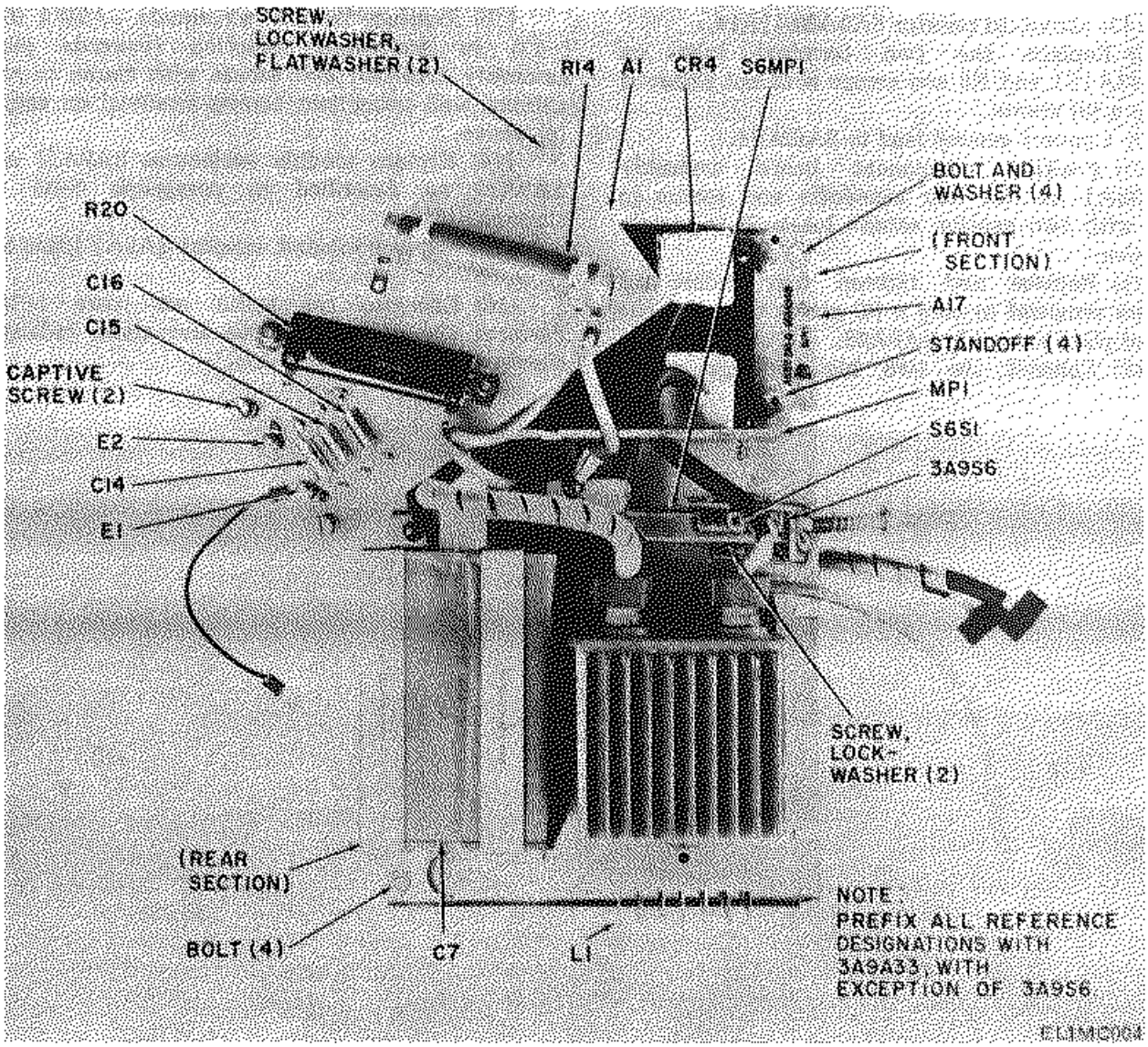


Figure 5-7.1. Plate assembly 3A9A33, top view, parts location, (part N0. 653434B).

5-11. Replacement of Power Supply Assembly 3A9A1

(figs. 5-1, 58, 5-12, and 5-13)

a. Removal

(1) Remove plate assembly 3A9A33 (para 5-10a).

(2) Remove the plate (fig. 5-12) above the circuit breaker panel by removing two screws securing the plate top and two screws and washers securing the plate bottom.

(3) Using a 7/16 inch socket wrench, remove the seven bolts (fig. 5-8) securing power supply assembly 3A9A1 to bottom of power amplifier cabinet 3A9. A mirror and light will aid in locating the bolts for removal.

(4) Check that all wires on power supply 3A9A1 are dressed clear of power amplifier cabinet 3A9 and that module enclosures 3A9A12 and 3A9A13 are clear from the front of 3A9.

WARNING

Power supply assembly 3A9A1 weighs 150 lbs. Two men are required to lift power supply assembly 3A9A1.

(5) Slowly work power supply assembly 3A9A33 out of power amplifier cabinet 3A9, being careful not to damage switch 3A9S9 (fig. 5-13).

CAUTION

Before sliding power supply assembly 3A9A1 into power amplifier cabinet 3A9, check that the bottom portion of power amplifier cabinet 3A9 is clear of all foreign matter such as metal filings, washers, nuts, bolts, etc.

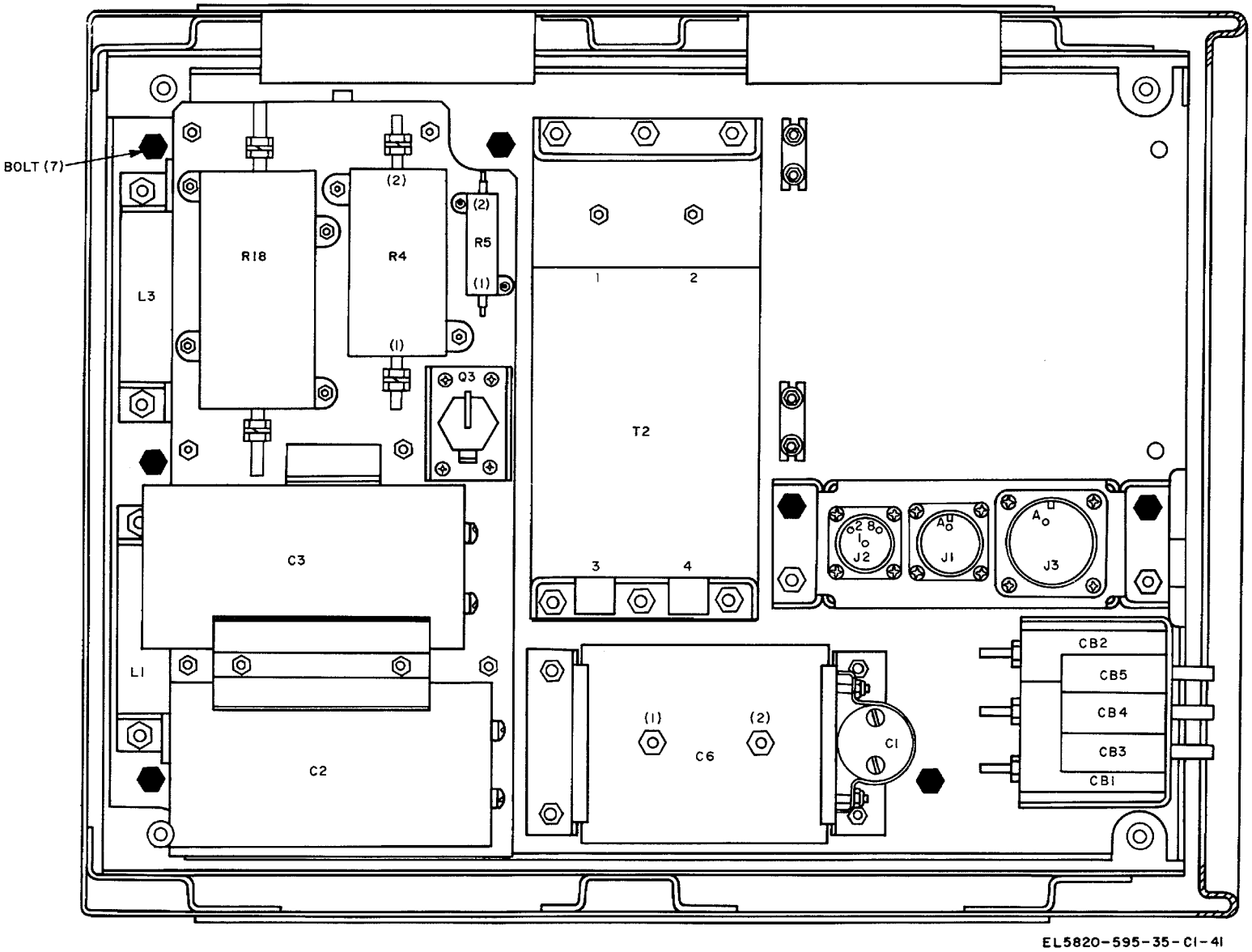


Figure 5-8. Power supply 3A9A1. mounting bolts location

(1) Lift replacement power supply assembly 3A9A1 and carefully slide it into power amplifier cabinet 3A9.

(2) Replace the seven bolts, removed in step a(3) above.

(3) Replace and secure the plate above circuit breaker panel using the four screws and two washers removed in step a (2) above.

(4) Replace plate assembly 3A9A33 as described in paragraph 5-10b (1) through (14).

(5) Energize the radio set (para 3-13) and perform the operator status and alarm indicator checks (TM 11-5820-595-12).

5-12. Replacement of Input Filter Assembly 3A9A8
(figs. 5-4 and 5-9)

a. Removal.

(1) Deenergize the radio set (para 3-12).
(2) Remove magnet assembly 3A9A7 as described in paragraph 5-8a(2) through (11).
(3) Loosen hose clamp securing tuner cooling hose to blower motor assembly 3A9B1 (fig. 5-4) and disconnect tuner cooling hose.
(4) Remove three screws and washers securing 230 volt protective shield (fig. 5-9) and remove the 230 volt protective shield.
(5) Tag and remove the four wire lugs connected to lower terminals of filters 3A9A8FL1 and 3A9A8FL3.
(6) Tag and remove the two wire lugs connected to the filter support bracket.
(7) Remove the two screws securing the filter support bracket to the right side wall of power amplifier cabinet 3A9.
(8) Remove six screws securing input filter assembly 3A9A8 to top of power amplifier cabinet 3A9.
(9) Carefully remove input filter assembly 3A9A8 from power amplifier cabinet 3A9.

b. Replacement.

(1) Carefully insert replacement input filter assembly 3A9A8 (fig. 5-9) into its proper position in power amplifier cabinet 3A9.

(2) Replace and tighten six screws removed in step a(8) above.

(3) Replace and tighten two screws removed in step a(7) above.

(4) Connect and secure two tagged wire lugs removed in step a(6) above, to the filter support bracket. TM 11-5820-595-35 (5) Connect and secure the four tagged wire lugs, removed in step a(5) above, to terminals of filters 3A9A8FL1 through 3A9A8FL3.

(6) Replace and secure the 230 volt protective shield with the three screws removed in step a(4).

(7) Connect tuner cooling hose (fig. 5-4) to blower motor assembly 3A9B1 and tighten hose clamp.

(8) Replace magnet support 3A9A7 (para 5-8f).

(9) Energize the radio set (para 3-13) and perform the operator status and alarm indicator checks (TM 11-5820-595-12).

5-13. Replacement of Blower Assembly 3A9B1
(figs. 5-10 and 5-12)

a. Removal.

(1) Remove input filter assembly 3A9AS8 (para 5-12a).

(2) Disconnect plug 3A9W11P5 from connector 3A9BlJ9 (fig. 5-10).

(3) Remove screw securing clamp that retains the wires connected to diode heat sinks 3A9A23CR10 and 3A9A29CR11 (fig. 5-12).

(4) Remove two screws, two nuts and washers securing diode heat sink 3A9A23CR11 to rear wall of power amplifier cabinet 3A9 and carefully move heat sink away from blower assembly 3A9B1.

(5) Remove two locknuts from locknut holes (fig. 5-10). The locknuts secure blower assembly 3A9B1 to rear wall of power amplifier cabinet 3A9.

(6) On top of power amplifier cabinet 3A9, remove five screws on washers from locknuts (fig. 5-10). The screws secure blower assembly 3A9B1 to top of power amplifier cabinet 3A9. Lower the blower assembly 3A9B1.

(7) Tilt blower assembly 3A9B1 toward left side of power amplifier cabinet 3A9 and carefully pull blower assembly 3A9B1 out of power amplifier cabinet 3A9.

b. Replacement.

(1) Carefully insert replacement blower assembly 3A9B1 into power amplifier cabinet 3A9 and position it against the top rear wall of power amplifier cabinet 3A9.

(2) While holding blower assembly 3A9B1 (fig. 5-12) in position, replace and tighten five screws and washers removed in step a(b) above.

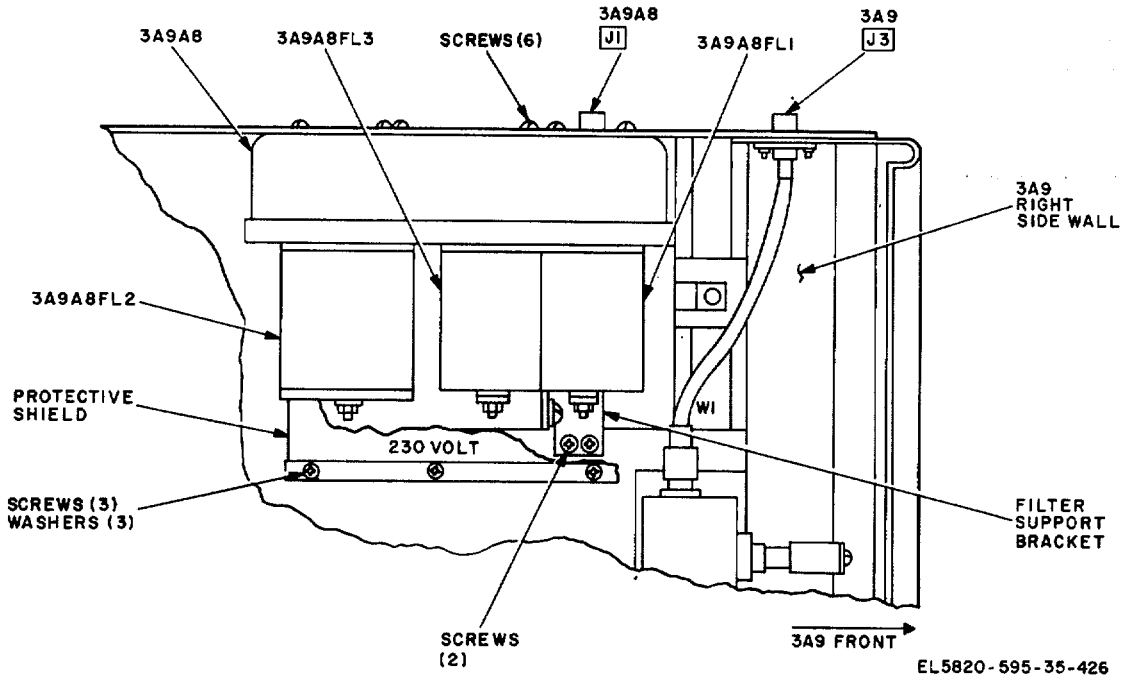


Figure 5-9. Input filter assembly 3A9A8, parts location.

(3) Replace and tighten the two locknuts, removed in step a (5) above, securing blower assembly 3A9B1 to the rear wall of power amplifier cabinet 3A9.

(4) Replace diode heat sinks 3A9A23CR11 removed in step a(4) above.

(5) Position and secure clamp with screw removed in step a (3) above.

(6) Connect plug 3A9W11P5 to connector 3A9BlJ9 (fig. 5-10) on blower assembly 3A9B1.

(7) Replace input filter assembly 3A9A8 as described in paragraph 5-12b (1) through (8).

(8) Energize the radio set (para 3-13).

(9) Place a hand over the power amplifier exhaust port on top of power amplifier cabinet 3A9 and check that air is being blown out of exhaust port.

5-14. Replacement of Vaneaxial Fans 3A9A26B2 through 3A9A26B5

(figs. 5-11, 5-12, and 5-15)

a. Removal of Fan Assembly 3A9A26.

(1) Deenergize radio set as described in paragraph 3-12.

(2) Loosen the four captive screws (fig. 5-12) that secure air filter 3A9A25 to fan assembly 3A9A26.

(3) Remove air filter 3A9A25.

(4) Tag and remove four wire lugs connected to lower terminals of terminal board 3A9A26TB1 (fig. 5-11).

(5) Remove seven locknuts from studs protruding through locknut stud holes (fig. 5-11).

(6) Feed wires removed from terminal band 3A9A26TB1 through access hole provided in fan assembly 3A9A26.

(7) Remove fan assembly 3A9A26 from power amplifier cabinet 3A9.

b. Removal of Vaneaxial Fans 3A9A26B2 through 3A9A26B5 from Fan Assembly 3A9A26.

(1) Tag and disconnect wire lugs connected to the terminal board on each vaneaxial fan.

(2) While supporting each fan loosen, but do not remove, the three screws securing each fan to the fan assembly 3A9A26. Each screw has a synclamp nut which secures the fan in position.

(3) Remove vaneaxial fans 3A9A26B2 through 3A9A26B5 from fan assembly 3A9A26.

c. Replacement of Vaneaxial Fans 3A9A26B2 through 3A9A26B5.

(1) Position one replacement fan at a time onto the fan assembly 3A9A26 and secure by tightening the three screws loosened in step b (2) above.

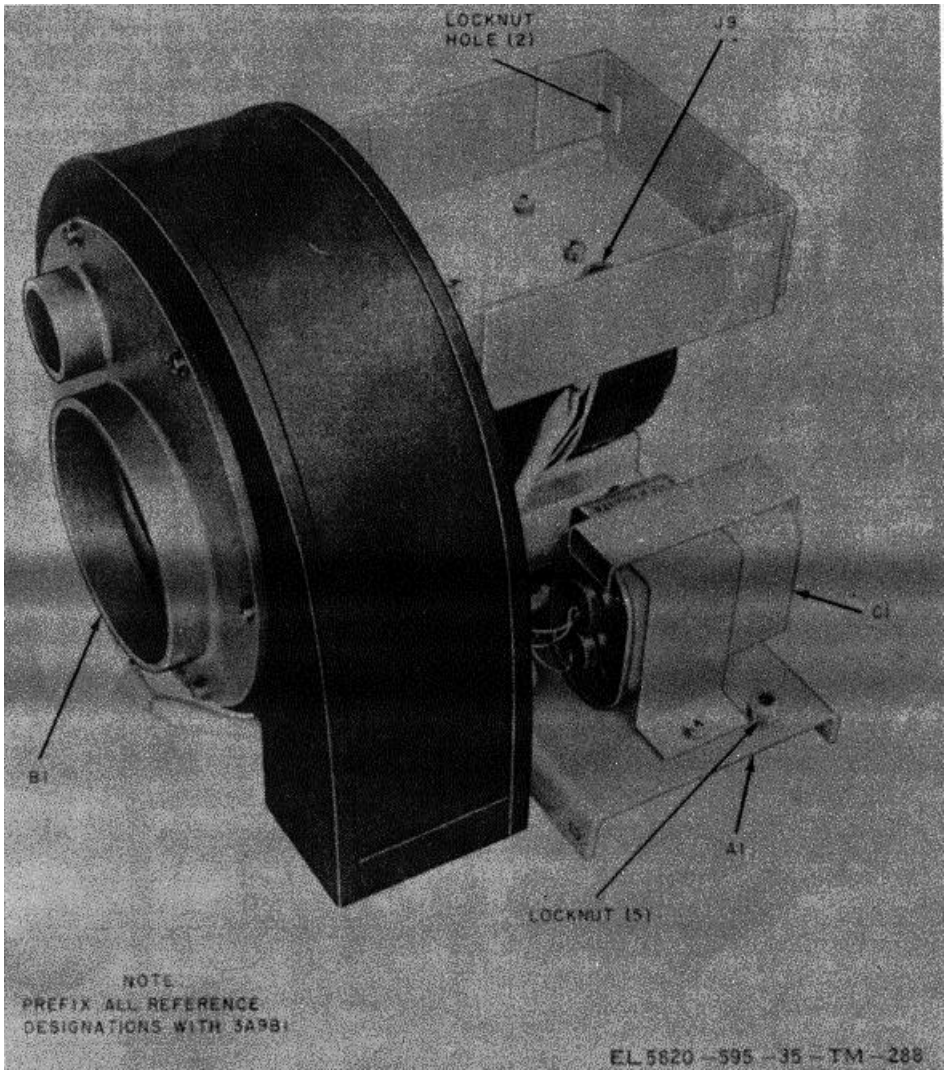


Figure 5-10. Blower assembly 3A9B1, right side view, parts location.

(2) Connect tagged wire lugs, removed in step b(l) above, to their respective terminals on vaneaxial fan terminal boards.

d. Replacement of Fan Assembly 3A9A26.

(1) Position fan assembly 3A9A26 on lower right side of power amplifier cabinet 3A9 and feed the four wires, removed from 3A9A26TB1 in step a(4) above, through access hole provided in center of fan assembly 3A9A26.

(2) Replace and tighten the seven locknuts, removed in step a(5) above.

(3) Connect the four wire lugs removed in step a(4) above, to lower terminals , on 3A9A26TB1.

(4) Insert air filter 3A9A25 into its holder and secure in place with the four captive screws loosened in step a(1) above.

(5) Energize the radio set (para 3-13) and check operation of fan assembly 3A9A26 by placing hand close to air filter 3A9A25 and sense air movement.

5-15. Repair and Replacement of Power Amplifier Cabinet Connectors

a. General. Repair of connectors in the power amplifier cabinet 3A9 requires either the replacement of the defective connector (solder type nonremovable contacts) or the replacement of defective connector contacts (crimp type removable contacts). A complete listing of power amplifier

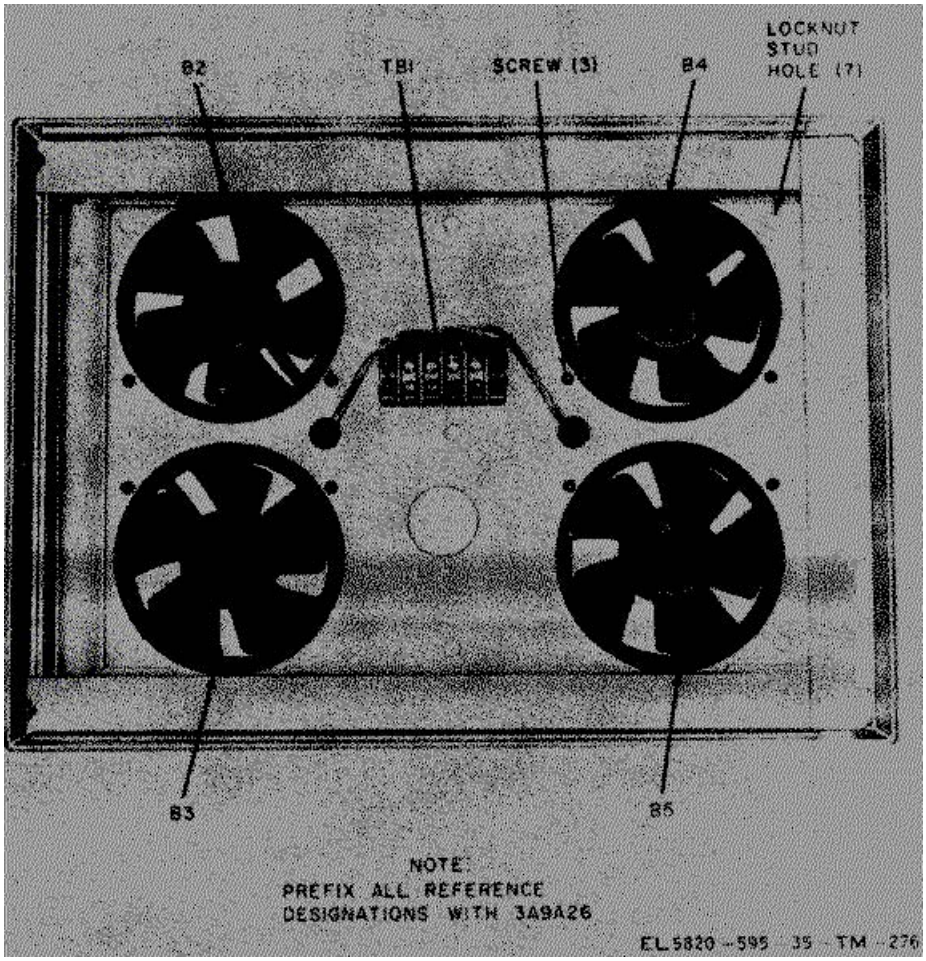


Figure 5-11. Fan assembly 3A9A26, viewed from filter side, parts location.

cabinet connectors is provided in b below. This chart specifies each connector type, the required repair procedure, the applicable tools and figure reference. Procedures for replacing the different type connector contacts are provided in paragraphs 3-32e and 5-15c and d. A continuity check should be performed after a connector pin is replaced.

b. Power Amplifier Cabinet Connectors.

Connector	Extraction /insertion tool	Crimping tool	Procedure paragraph	Figure reference
3A9J2	MS24256 R20/A20	None required	5-15c	5-4
3A9J4	MS24256 R20/A20	None required	5-15c	5-4
3A9J7	MS24256 R20/A20	None required	5-15c	5-14
3A9A1J1	MS24256 R12/A12	None required	5-15c	5-8
3A9A1J2	MS24256 R12/A12	MS3191-3 with head assy W1	3-32e	5-8
3A9A1J3	MS24256 R12/A12	None required	5-15c	5-8
	MS24256 R20/A20	None required	5-15c	5-8
3A9A8J1	MS24256 PR2/A12	None required	5-15e	5-9
3A9B1J9	MS24256 R12/A12-	None required	5-15c	5-10
	MS24256 R16/A16	None required	5-15c	5-10
3A9W11P1	MS24256 R12/A12	None required	5-15c	5-14
3A9W11P2	MS24256 R12/A12	MS3191-3 with head assy W1	3-32e	4-14
3A9W11P5	MS24256 R20/A20	None required	5-15c	5-14
3A9XA1 through XA7	None required	None required	5-15d	5-12

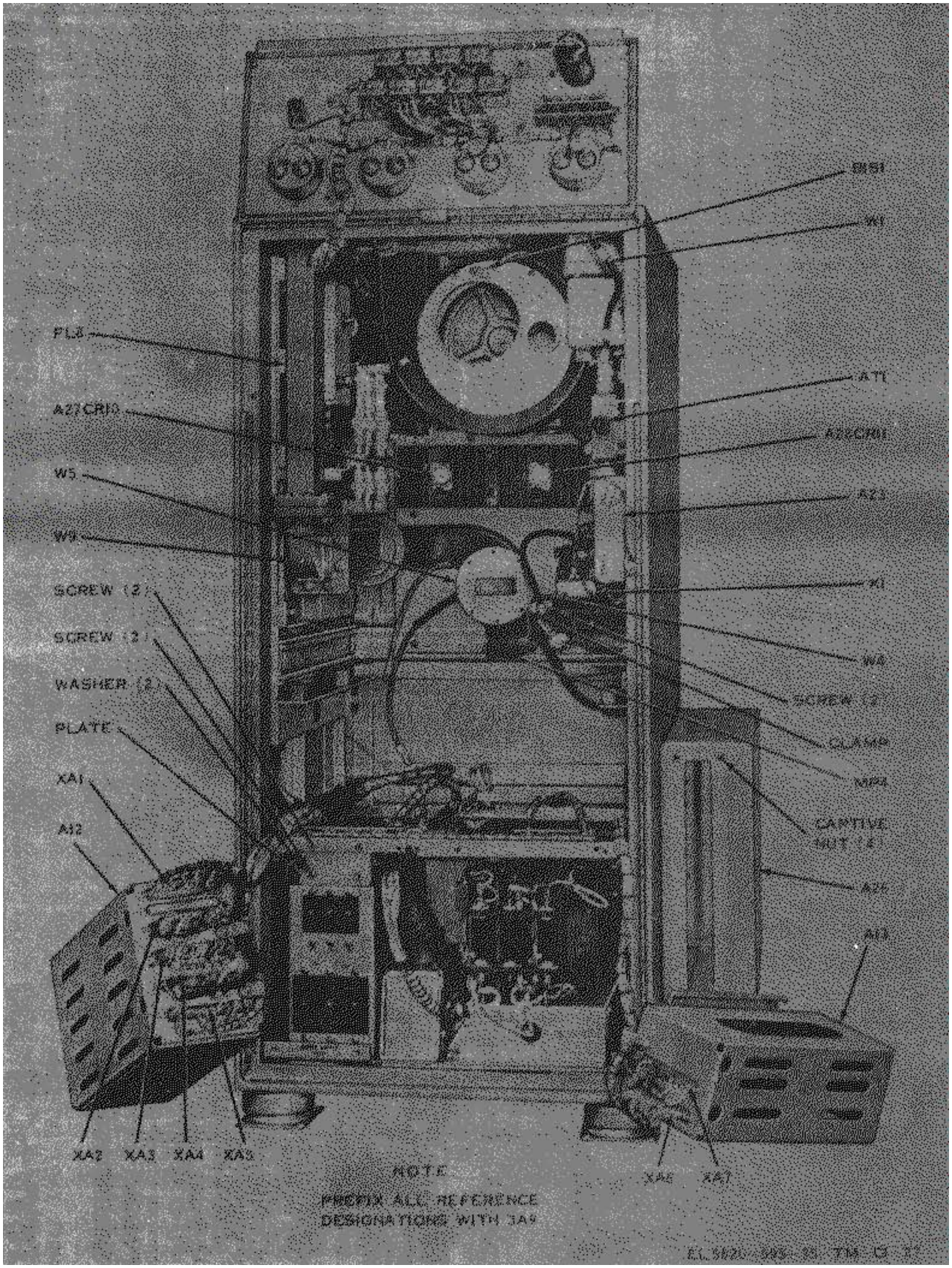


Figure 5-12. Power amplifier cabinet 3A9, front view, partially disassembled, parts location.

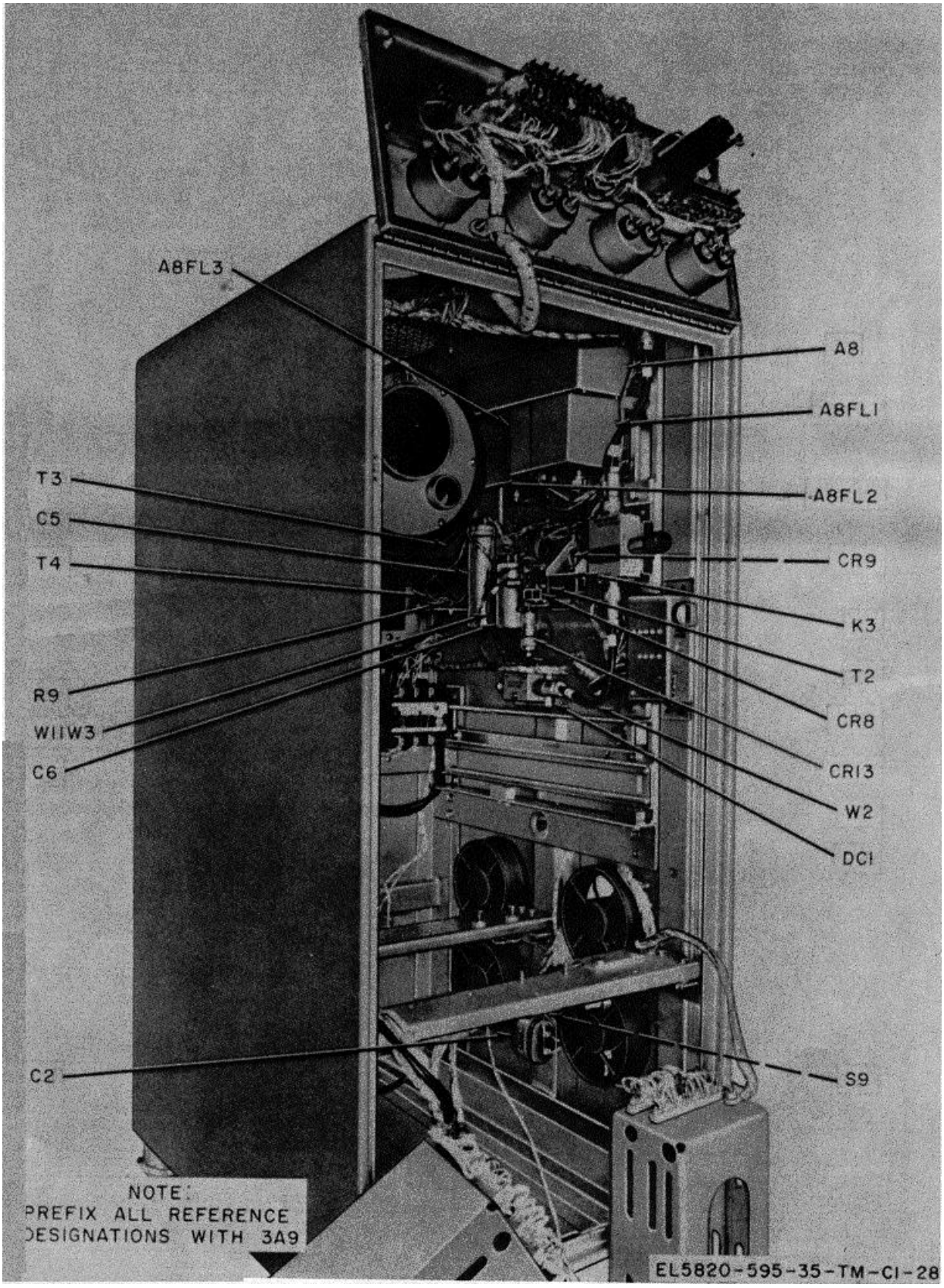


Figure 5-13. Power amplifier cabinet 3A9, left oblique view, parts location.

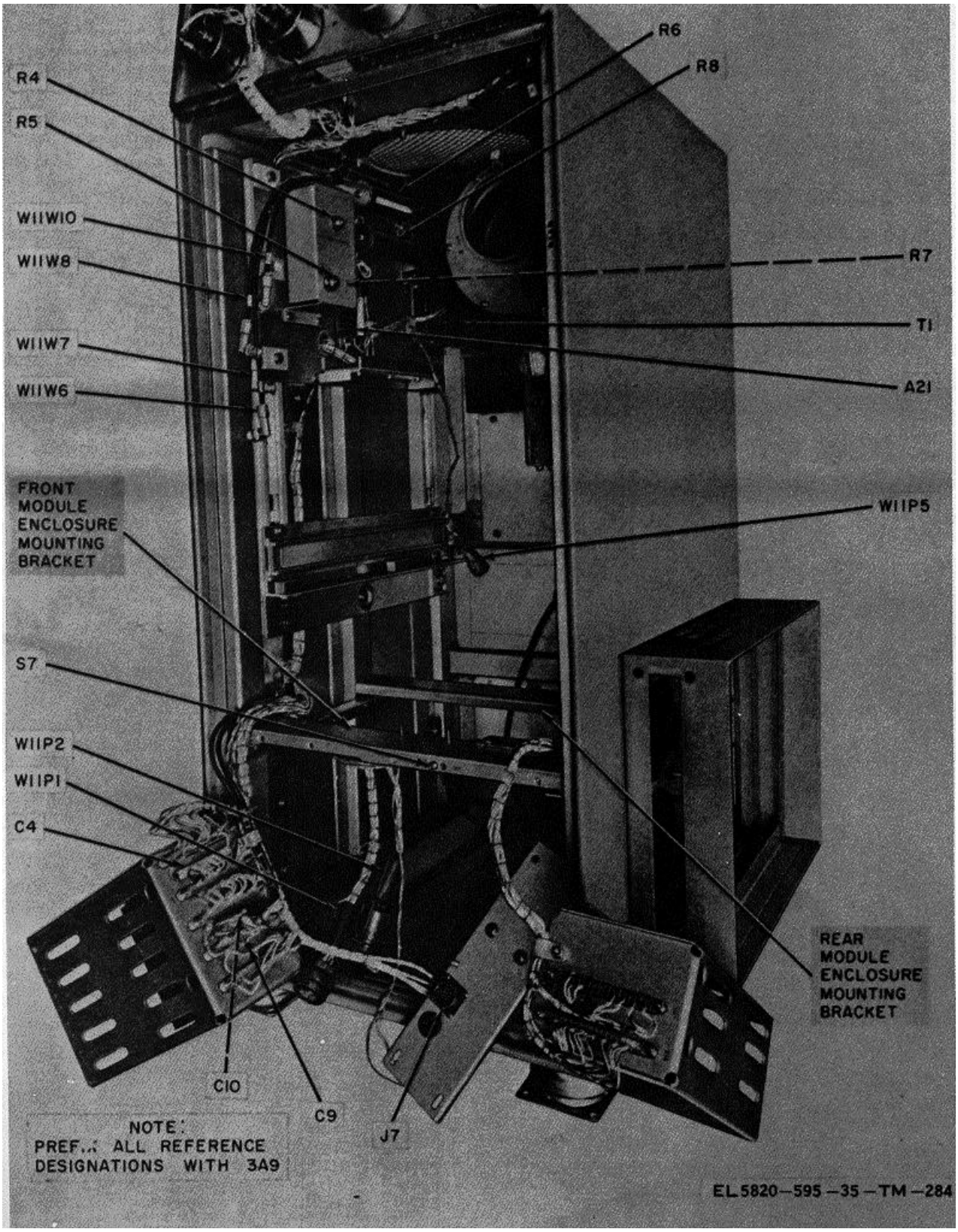


Figure 5-14. Power amplifier cabinet 3A9, right oblique view, parts location.

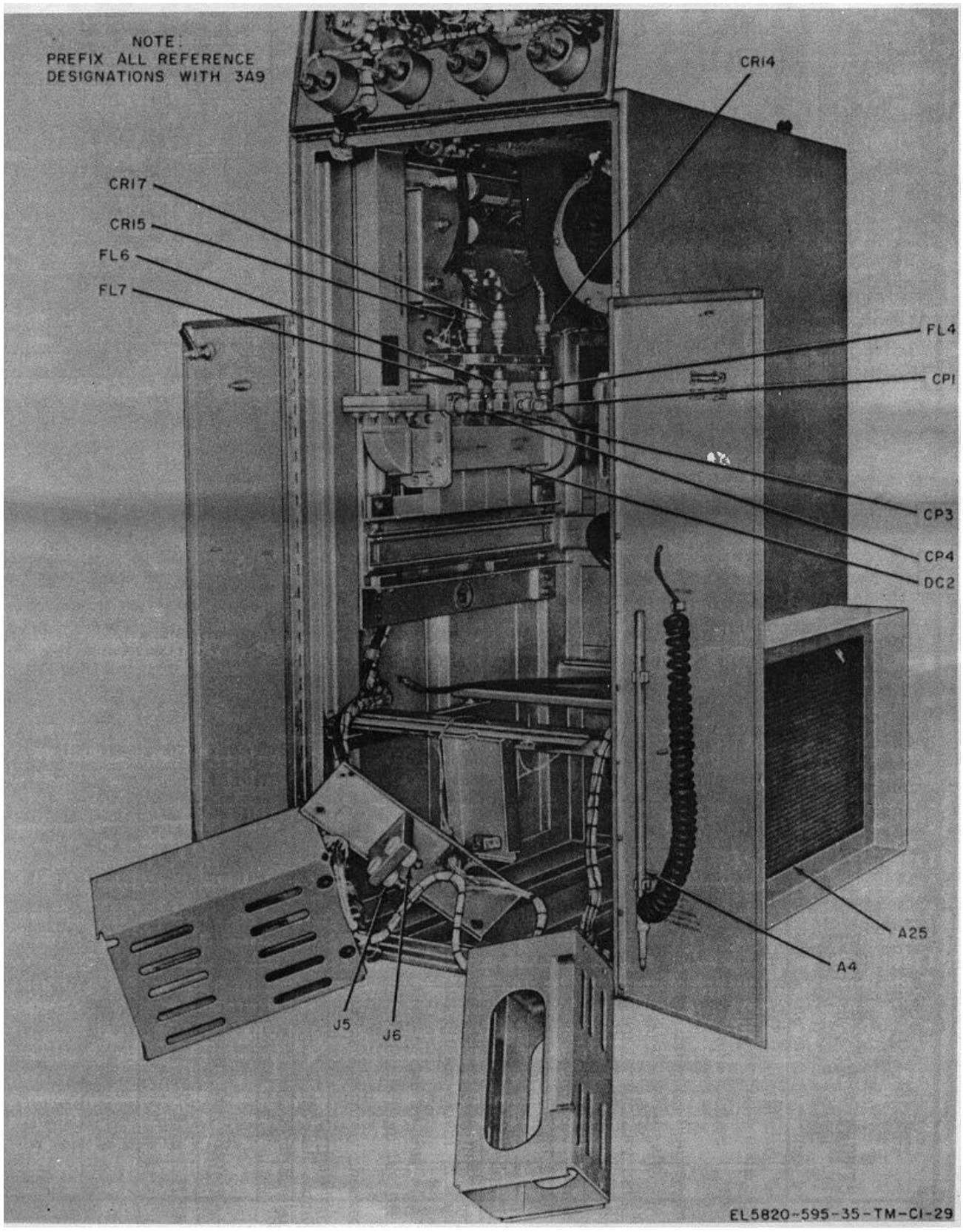


Figure 5-15. Power amplifier cabinet 3A9, left inside view, parts location.

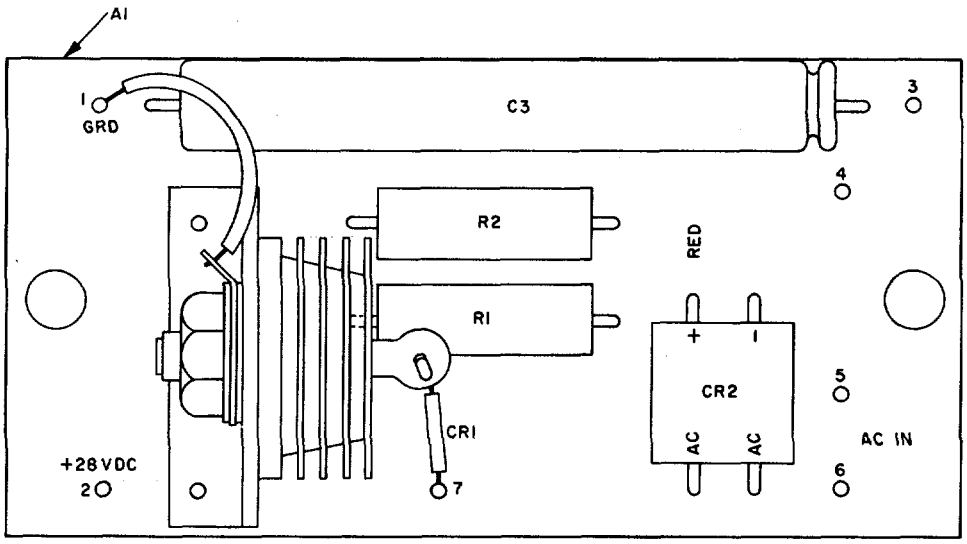


Figure 5-16. Rectifier assembly 3A9A21, front view, parts location.

c. Solder Type Removable Contact (Round Connectors). The procedure for removing any of the contacts from this type of connector is identical to the procedure given in paragraph 3-32c (1). Replacement of the contact is performed as follows:

(1) Unsolder the contact pin from the wire.

(2) Insert .the wire to the replacement contact pin.

(3) Solder the wire to the contact pin.

(4) Use the insertion tool listed in the chart (b above) to insert the contact pin into its connector.

d. Solder Type Nonremovable Contact (Rectangular Connectors). The individual contacts of these connectors cannot be removed. Therefore, when any contact in the connector is defective, the connector must be replaced. To replace any of these connectors, proceed as follows:

(1) Remove the module inclosures (3A9A12 and 3A9A13) from the power amplifier cabinet (para 5-9a).

(2) Remove the two screws, nuts, and washers securing the connector to the module inclosure (3A9A12 or 3A9A13) and carefully remove the connector from the module inclosure.

(3) Insert new connector in position on module inclosure and secure it in place using the two screws, nuts, and washers removed above.

(4) One at a time, unsolder a wire from the defective connector and solder it to the same pin on the new connector.

(5) Repeat this procedure until all wires have been transferred to the new connector and then reinstall the module inclosures (para 5-9b).

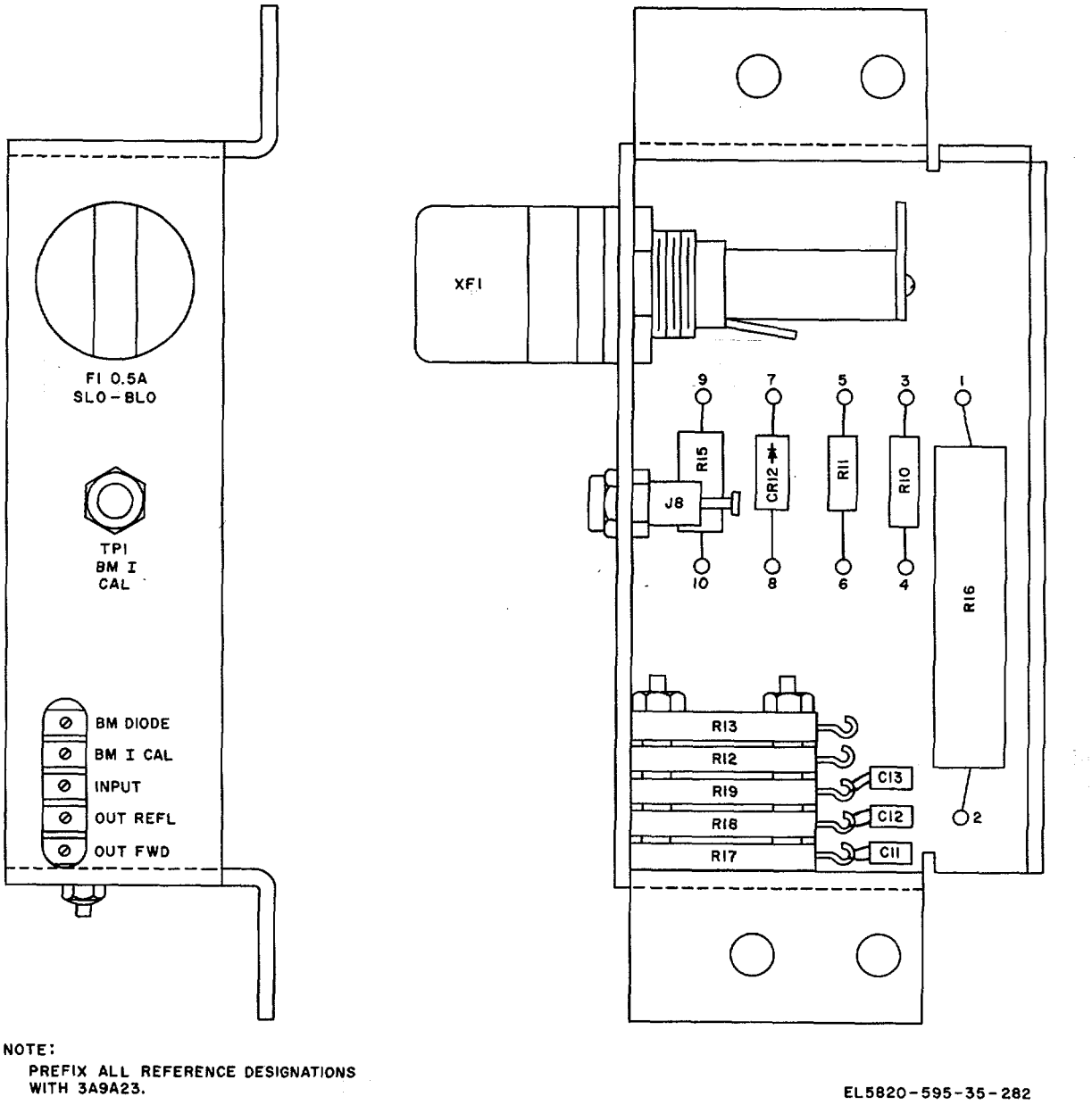


Figure 5-17. Bracket assembly 3A9A23, parts location.

Section III. POWER AMPLIFIER CALIBRATION AND ADJUSTMENT

5-16. General

a. This section contains procedures for calibrating, adjusting, and checking the power amplifier. The calibration and adjustment procedures (except calibration of power amplifier frequency tuner drum dial readout, para 5-23) are performed at periodic maintenance intervals (para 2-4) to maintain the calibration accuracy of the power amplifier metering circuits and adjust its alarm circuits. The calibration and adjustments procedures are also performed when indicated in the power amplifier troubleshooting chart (para 5-3d) to aid in troubleshooting. The power amplifier frequency tuner drum dial readout calibration procedure (para 5-23) must be performed when power amplifier klystron tube 3A9V1 or frequency tuner 3A9A6 is replaced. The power amplifier filament current sensing check (para

5-27) is performed at periodic maintenance intervals (para 2-4) to check that the filament current alarm circuit is operational.

b. All of the procedures contained in this section assume that the radio set is turned on and connected for normal operation at the start of each procedure. Prior to performing any of the procedures, the maintenance man should notify the Multiplexer TD-240/U and distant radio set operators that radio communications will be temporarily interrupted.

c. If trouble is encountered during performance of a procedure, or if the indications specified in the procedure are not obtained, refer to the power amplifier troubleshooting chart (para 5-3d) for corrective action.

5-17. Calibration of Power Amplifier FILAMENT VOLTAGE Meter 3A9M2

a. Turn the TS-656/U on and allow a 10-minute warmup period.

b Set the ME-202B/U RANGE control to 500, AC-DC polarity control to +, voltage readout dials to 0, and the power switch to ON. Allow a 10-minute warmup period.

c. Turn the power amplifier off by performing the procedures in paragraph 3-12 c and d.

d. Tag and remove the wires connected to the terminals of meter 3A9M2 (fig. 5-2).

e. Connect a jumper wire between the two terminals of meter 3A9M2 and adjust the meter zero screw on the front of meter 3A9M2 (fig. 5-1) for a zero meter indication.

f. Remove the jumper wire from terminals of meter 3A9M2.

g. Set the TS-656/U FUNCTION switch to AC Volts, the VOLTAGE switch to 10OV.

h. Advance the ME-202B/U OPERATECALIBRATE control to CALIBRATE position and while holding the control in that position adjust the CALIBRATE control for a zero indication on VOLTS meter.

i. Set the ME-202B/U AC-DC polarity switch' to AC.

j. Connect the test setup shown in figure 5-17.1.

k. Rotate the TS-656/U DECREASE/INCREASE control until the 3A9M2 meter indicates 8 volts.

l. Set the ME-202B/U RANGE control to 50.

NOTE

The ME-202B/U A voltage readout dial control changes the internal voltage of the ME-202B/U the greatest amount and the El voltage readout dial control changes the internal voltage the least amount.

m. Repeat h and k above and then check to make certain the ME-202B/U VOLTS meter indicates zero. If not, readjust voltage readout dial controls.

n. Determine the actual voltage being used to cause the 3A9M2 meter to show an indication of 8 volts by reading the ME-202B/U voltage readout dials. Be sure to note location of decimal indication. If the voltage readout dials indicate less than 7.8 volts or greater than 8.2 volts, replace meter 3A9M2 (fig. 5-2) and repeat the entire calibration procedure.

o. Connect the wires removed in d above to the terminals of meter 3A9M2.

p. Energize the power amplifier (para 3-13).

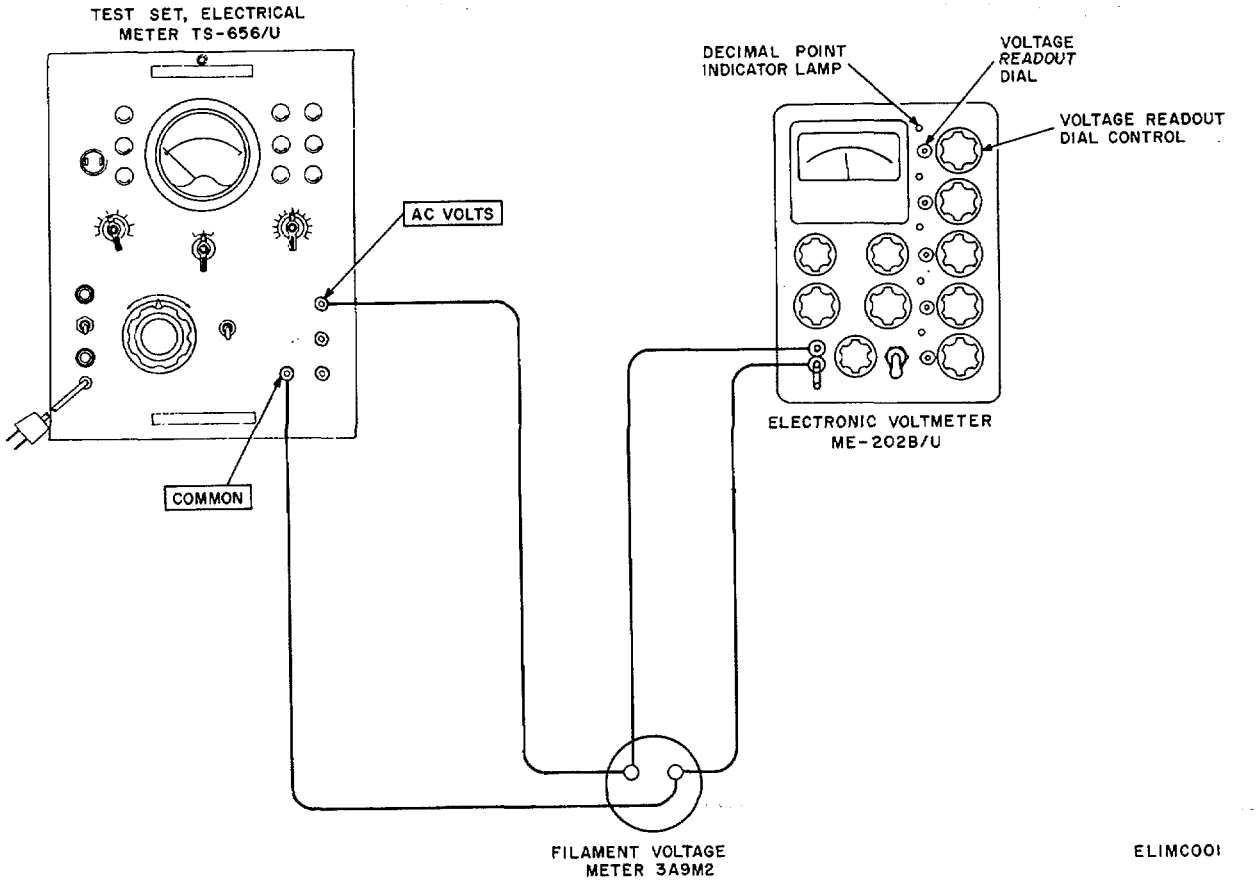


Figure 5-17.1. Power amplifier filament voltage meter 3A9M2 calibration test setup.

5-18. Calibration of Power Amplifier BEAM VOLTAGE Meter 3A9M3

a. Turn the TS-656/U on and allow a 5-minute warmup period.

b. Turn the power amplifier off by performing c and d of paragraph 3-12.

c. Tag and remove the wires connected to the terminals of meter 3A9M3 (fig. 5-2).

d. Connect a jumper wire between the two terminals of meter 3A9M3 and adjust the meter zero screw on the front of meter 3A9M3 (fig. 5-1) for a zero meter indication.

e. Remove the jumper wire from terminals of meter 3A9M3.

f. On the TS-656/U, set the FUNCTION switch to DIR CUR, set the CURRENT switch to 2.5 MA, and rotate the DECREASE/INCREASE control counterclockwise until the mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the + (positive) terminal of meter 3A9M3.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on the COMMON terminal on TS-656/U and the (negative) terminal of meter 3A9M3.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing j and k below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter 3A9M3 indicates 10.

k. Record the meter indication on TS-656/U and then release the TEST switch.

l. Turn the IS656/U off and disconnect the test leads.

m. Meter indication recorded in k above should be 1.0 + 0.02 milliamperes. If it is not, replace meter 3A9M3 (fig. 5-2) and repeat the entire calibration procedure.

n. Connect the wires removed in c above to the terminals on the rear of meter 3A9M3.

o. Energize the power amplifier (para 3-13).

5-19. Calibration of Power Amplifier BEAM CURRENT Meter 3A9M4

a. Turn the TS-656/U on and allow a 5minute warmup period.

b. Turn the power amplifier off by performing c and d of paragraph 3-12.

c. Tag and remove the wires connected to the terminals of meter 3A9M4 (fig. 5-2).

d. Connect a jumper wire between the two terminals of meter 3A9M4 and adjust the meter zero screw on the front of meter 3A9M4 (fig. 5-1) for a zero meter indication.

e. Remove the jumper wire from terminals of meter 3A9M4.

f. On the TS-656/U, set the FUNCTION switch to DIR CUR, set the CURRENT switch to 250 MICRO-RAMP, and rotate the DECREASE/ INCREASE control counterclockwise until the mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the + (positive) terminal of meter 3A9M4.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the -(negative) terminal of meter 3A9M4.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing j and k below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until 3A9M4 indication is 1.

k. Record the meter indication on TS-656/U and then release the TEST switch.

l. Turn the TS-656/U off and disconnect the test leads.

m. Meter indication recorded in k above should be 200 $\pm$ 5 microamperes. If it is not, replace meter 3A9M4 (fig. 5-2) and repeat the entire calibration procedure.

n. Connect the wires removed in c above to the terminals on the rear of meter 3A9M4.

o. Energize the power amplifier (para 3-13).

5-20. Calibration of Power Amplifier RF Monitor Meter 3A9M5

a. Turn the TS-56-456/U on and allow a 5-minute warmup period.

b. Turn the power amplifier off by performing c and d of paragraph 3-12.

c. Tag and remove the wires connected to the terminals of meter 3A9M5 (fig. 5-2).

d. Connect a jumper wire between the two terminals of meter 3A9M5 and adjust the meter zero screw on the front of meter 3A9M5 (fig. 5-1) for a zero meter indication.

e. Remove the jumper wire from terminals of meter 3A9M5.

f. On the TS-656/U, set the FUNCTION switch DIR CUR, set the CURRENT switch to 250 MICRO-AMP, and rotate the DECREASE/INCREASE control counterclockwise until the mechanical stop is reached.

g. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and the + (positive) terminal of meter 3A9M5.

h. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and the (negative) terminal of meter 3A9M5.

i. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing j and k below.

j. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until 3A9M5 indication is 150.

k. Record meter indication on TS-656/U and then release the TEST switch.

l. Turn the TS-656/U off and disconnect the test leads.

m. Meter indication recorded in Ak above should be 200 5 microamperes. If it is not, replace meter 3A9M5 (fig. 5-2) and then repeat the entire calibration procedure.

n. Connect the wires removed in c above to the terminals on the rear of meter 3A9M5.

o. Energize the power amplifier (para 3-13).

5-21. Calibration of Power Amplifier Input Power Metering Circuit

a. Turn the AN USM-161 on and allow a 30minute warmup period. After the warmup period, calibrate the AN USM-161 using the procedure given in TM 11-6625-498-12.

b. Record the transmitter operating frequency.

c. On the transmitter, set the control on frequency synthesize. 11A14 and 4.4 to 5.0-GHz bandpass filter 1 F13 to 4800.0 MHz

d. Press the BEAM SWITCH and MAIN POWER SWITCH on the power amplifier meter panel. The BEAM SWITCH shall light red and then be extinguished when the MAIN POWER SWITCH lights white.

e. On the power amplifier, set attenuator control 3A9AT1 (fig. 5-18) fully counterclockwise for maximum attenuation.

f. Refer to the calibration plate on CN-845/ USM-161 (fig. 5-18) and calculate the correction factor for a 4800 MHz input. Record.

g. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 10 MW 4-10 DBM, set the COMP ATTENUATOR dial to the value recorded in f above, and set the POWER indicator dial for a dial scale indication of .40 on the outermost scale.

h. Disconnect coaxial cable 3A9W4 from RF input connector 3A9V1P1 (fig. 5-5) and then connect the test equipment as shown in figure 5-18.

i. On the power amplifier meter panel, press the INPUT FORWARD MILLIWATT pushbutton on RF MONITOR SELECT switch 3A9S8.

j. Turn attenuator control 3A9AT1 clockwise until a null indication is obtained on the AN,/ USM-161 NUI,L INI)ICATOR meter.

k. Indication on power amplifier RF MONITOR meter 3A9M5 should be 40. If it is not, perform the adjustment given 'in I below. Otherwise, proceed to m below.

l. Using a screwdriver, adjust INPUT potentiometer 3A9A23R19 (fig. 5-18) for a RF MONITOR meter indication of 40. If a meter indication of 40 cannot be obtained, refer to the power amplifier troubleshooting chart (item 25, para 5-3d) for corrective action upon completion of this procedure.

m. Turn attenuator control 3A9AT1 fully counterclockwise for maximum attenuation.

n. Turn the AN/USM-161 off and disconnect the test equipment.

o. Connect coaxial cable 3A9W4 to RF input connector 3A9VlP1 (fig. 5-5).

p. Set the controls on transmitter frequency synthesizer 1A14 and 4.4to 5.0-GHz bandpass filter 1FL3 to the original operating frequency recorded in b above.

q. Press the MAIN POWER SWITCH and BEAM SWITCH on the power amplifier meter panel. The MAIN POWER SWITCH shall light green and the BEAM SWITCH shall light green.

5-22. Calibration of Power Amplifier Forward Power Metering Circuit

WARNING

High frequency electromagnetic radiation is present in the power amplifier. Do not work on the power amplifier or its waveguide RF output while the power amplifier is turned on.

a. Turn the AN/USM-161 on and allow a 30 minute warmup period. After the warmup period, calibrate the AN/USM-161 using the procedure given in TM 11-6625-498-12.

b. Deenergize the power amplifier (para 3-12).

WARNING

Be sure that all waveguide connections made in c, d, or e below are tightened securely to prevent RF radiation.

c. If the power amplifier is mounted in Shelter S-336/TRC-112, disconnect the shelter mounted waveguide section normally installed between points A and B in figure 5-19 and install the directional coupler 11DC1 and waveguide assembly 11W6 in its place. Use the waveguide screws supplied with MK-1207/GRC to secure directional coupler 11DC1 and waveguide assembly 11W6 in the waveguide. Use four screws to secure each section. Be sure that directional coupler 11DC1 is installed with the end marked INPUT closest to the power amplifier and its type N connector facing down.

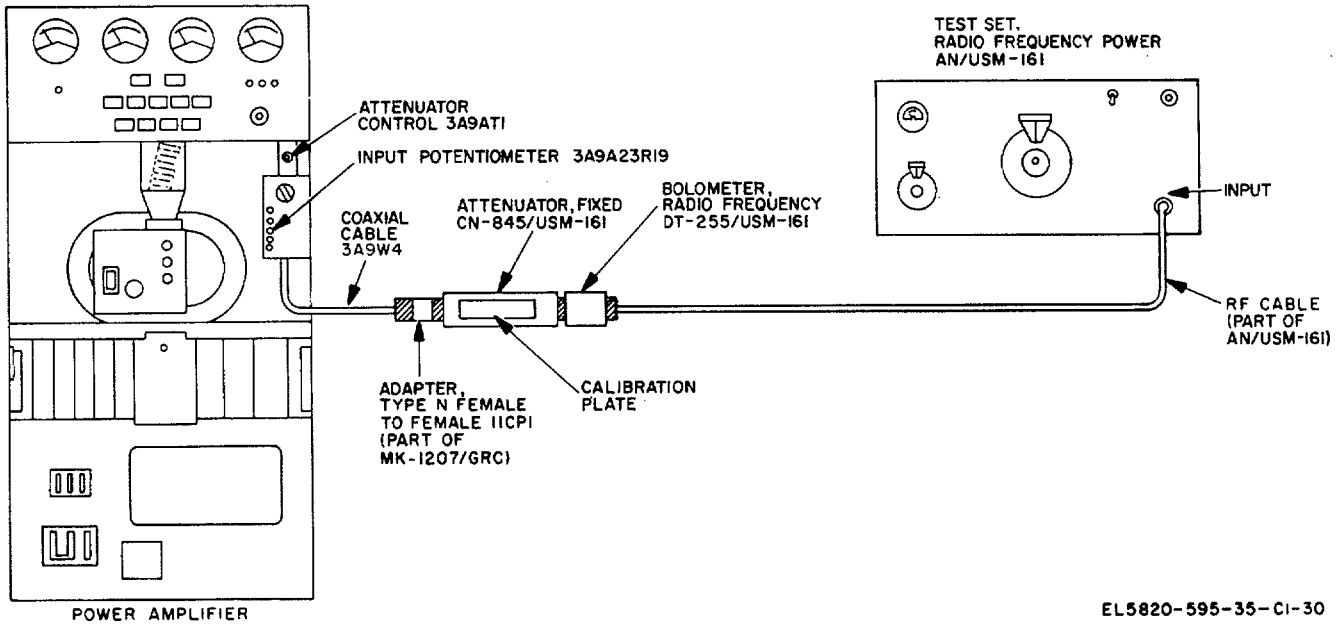


Figure 5-18. Power amplifier input power metering circuit calibration test set up.

d. For the power amplifier mounted on the curbside of Shelter S-338/TRC-121, disconnect the shelter mounted waveguide section normally installed between points A and B of figure 5-20 and install waveguide assembly 11W4 and the directional coupler 11DC1 in its place. Use the waveguide screws supplied with MK-1207/ GRC to secure directional coupler 11DC1 ant waveguide assembly llW6 in the waveguide. I four screws to secure each section. Be sure the directional coupler 11DC1 is installed with end marked INPUT closest to the power amplifier and its type N connector facing toward the front of the power amplifier.

e. For the power amplifier mounted on the roadside of Shelter S-338/TRC-121, disconnect the shelter mounted waveguide section normally installed between points A and B of figure 5-21 and install waveguide assembly llW5 and the directional coupler 11DC1 in its place. Use the waveguide screws supplied with MK-1207/ GRC to secure directional coupler 11DC1 and waveguide assembly 11W6 in the waveguide. Use four screws to secure each section. Be. s that the directional coupler 11DC1 is installer with the end marked INPUT closest to the pov amplifier and its type N connector facing the front of the power amplifier.

f. Connect Bolometer, Radio Frequency DT-255/USM-161 to the type N connector on directional coupler 11DC1 figs. 5-19, 5-20,or 5-21.

g. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 3 MW + 5 DBM, set the COMP ATTENUATOR dial for a dial scale indication of 0, and set the POWER indicator dial for a dial scale indication of 1.0 on the center scale.

h. Energize the power amplifier (para 3-13).

i. Record the transmitter operating frequency and then set the controls on frequency synthesizer 1A14 and 4.4to 5.0-GHz bandpass filter 1FL3 to 4800.0 MHz.

j. Tune the power amplifier (TM 11-5820-595-12) to the same operating frequency as the transmitter.

k. Adjust the BEAM VOLT ADJ control on inverter regulator control module 3A1 until a null indication is obtained on the AN/USM-161 NULL INDICATOR meter.

l. Press the ANTENNA FORWARD WATTS X 10 pushbutton on the power amplifier meter panel.

m. Indication on RF MONITOR meter 3A9M5 e should be 100. If it is not, perform the adjustment given in n below. Otherwise, proceed to o below.

n. Adjust OUT FWD potentiometer 3A9A23R17 (fig. 5-17) for a RF MONITOR meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the power amplifier troubleshooting chart (item 26, para 5-3d) for corrective action.

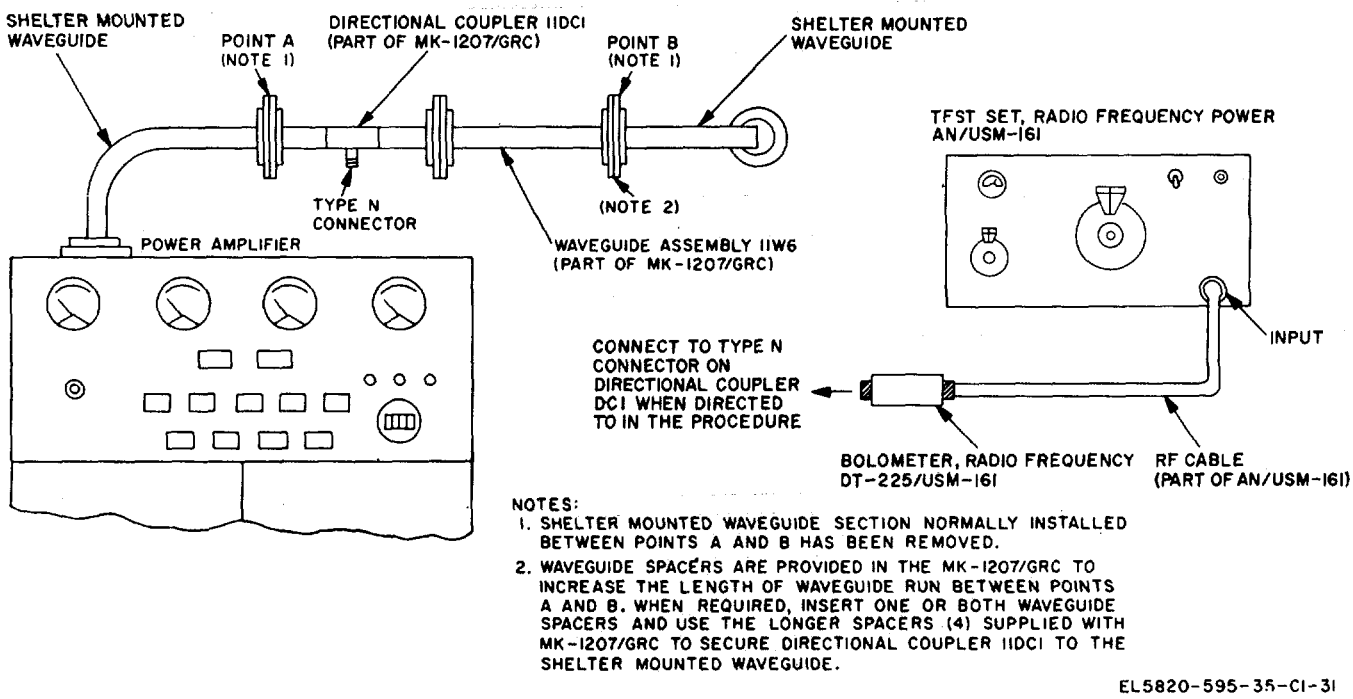


Figure 5-19. Power amplifier forward power metering circuit calibration test setup for power amplifier mounted in Shelter S-336/TRC-112.

o. Repeat *i* through m above for transmitter and power amplifier operating frequencies of 4.4 and 5.0 GHz. RF MONITOR meter indication must remain between 70 and 140.

p. Deenergize the power amplifier (para 3-12).

q. Turn the AN/USM-161 off and disconnect the test equipment.

WARNING

Be sure that all waveguide connections made in r below are tightened securely to prevent RF radiation.

r. Reinstall the shelter mounted waveguide section removed in c, d, or e above.

s. On the transmitter, set the controls on frequency synthesizer 1A14 and 4.4to 5.0-GHz bandpass filter 1FL3 to the original operating frequency recorded in i above.

t. Energize the power amplifier (para 3-13).

u. Tune the power amplifier (TM 11-5820595-12) to the same operating frequency as the transmitter.

5-23. Calibration of Power Amplifier Frequency Tuner Drum Dial Headout

a. Record the transmitter operating frequency.

b. On the transmitter, set the controls on frequency synthesizer 1A14 and 4.4to 5.0-GHz bandpass filter 1FL3 to 4800.0 MHz.

c. On the power amplifier, set MAIN TUNING control knob (fig. 5-5) for a 4.8-GHz indication and tune the power amplifier (TM 11-5820-595-12).

NOTE

Care must be exercised to insure that the power amplifier tuning controls are not moved after the power amplifier is tuned. If any control is moved in the following steps, return to c above.

d. Deenergize the power amplifier (para 3-12).

e. Loosen the four screws securing frequency tuner'3A9A6 to magnet support 3A9A7 (fig. 5-5).

f. Slide frequency tuner 3A9A6 toward the right side of magnet support 3A9A7.

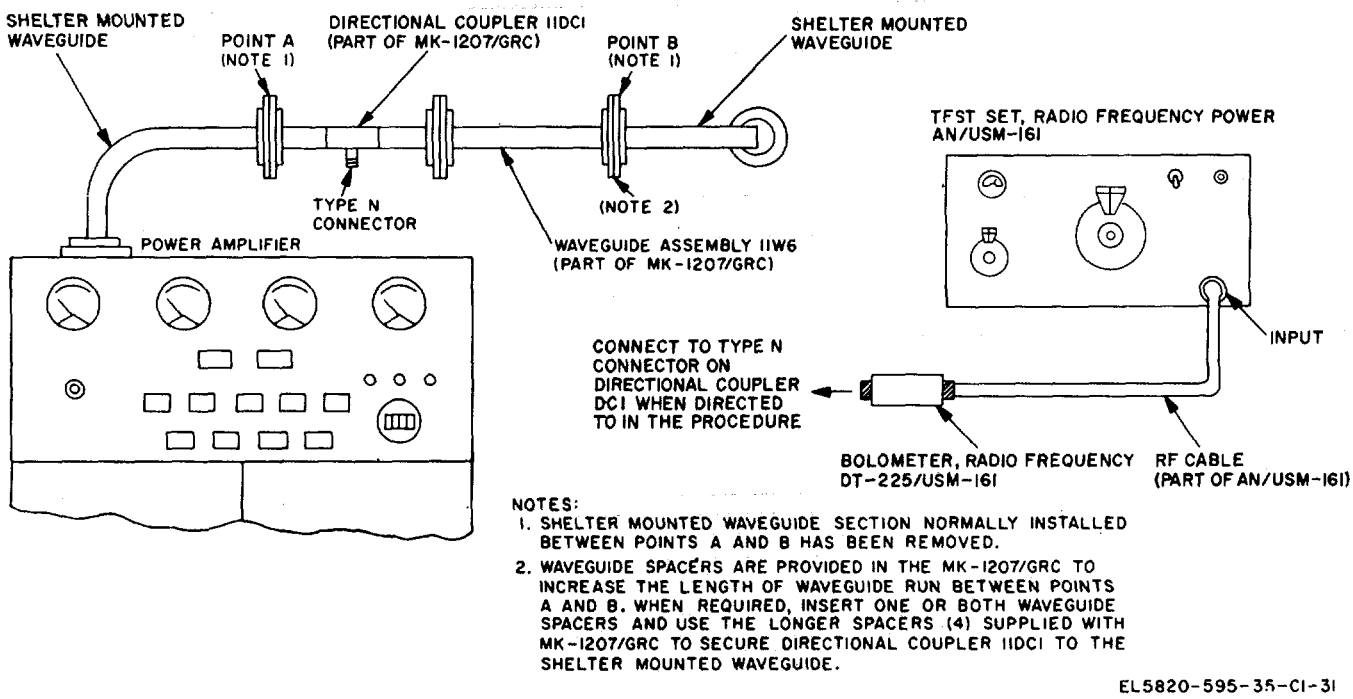


Figure 5-20. Power amplifier forward power metering circuit calibration test setup for power amplifier mounted on cubeside of Shelter S-3S8/TRC-121

g. Using care that position of MAIN TUNING control knob 3A9A6MP14 is not disturbed, slip sprocket chain 3A9MP14 off of miniature sprocket 3A9A6MP17 (fig. 5-5).

h. With sprocket chain 3A9MP14 removed, turn MAIN TUNING control knob 3A9A6MP14 until drum dial readout is 4.8 GHz.

i. Hold MAIN TUNING control knob 3A9A6MP14 in position with one hand and slip sprocket chain 3A9MP14 onto miniature sprocket 3A9A6MP17.

j. Slide frequency tuner 3A9A6 toward the left side of magnet support 3A9A7 until sprocket chain 3A9MP14 is taut, then tighten the four screws securing frequency tuner 3A9A6 to magnet support 3A9A7.

k. On the transmitter, set the controls on frequency synthesizer lA14 and 4.4to 5.0-GHz bandpass filter 1FL3 to 4400.0 MHz.

l. Energize the radio set (para 3-13) and set the power amplifier MAIN TUNING control to 4.4 GHz and tune the power amplifier (TM 11-5820-595-12).

m. Observe that frequency tuner drum dial readout is 4.4 GHz + 50 MHz (2 divisions on frequency tuner drum dial readout). If it is not, return to c above and carefully reset the frequency tuner drum dial readout.

n. Repeat k through m above for the following frequencies: 4700 MHz, 5000 MHz, and the original transmitter operating frequency recorded in a above.

5-24. Power Amplifier DC Overload Trip Point Adjustment and Beam Current Metering Circuit Calibration

a. -Turn meter calibration test set 11Al (part of !K-1207/GRC) on and allow a 5-minute warmup period.

b. Press the BEAM SWITCH on the power amplifier meter panel. The BEAM SWITCH and BEAM indicators on the power amplifier meter panel shall light red.

c. Set BEAM POWER circuit breaker 3A9A1CB2 (fig. 5-22) to OFF.

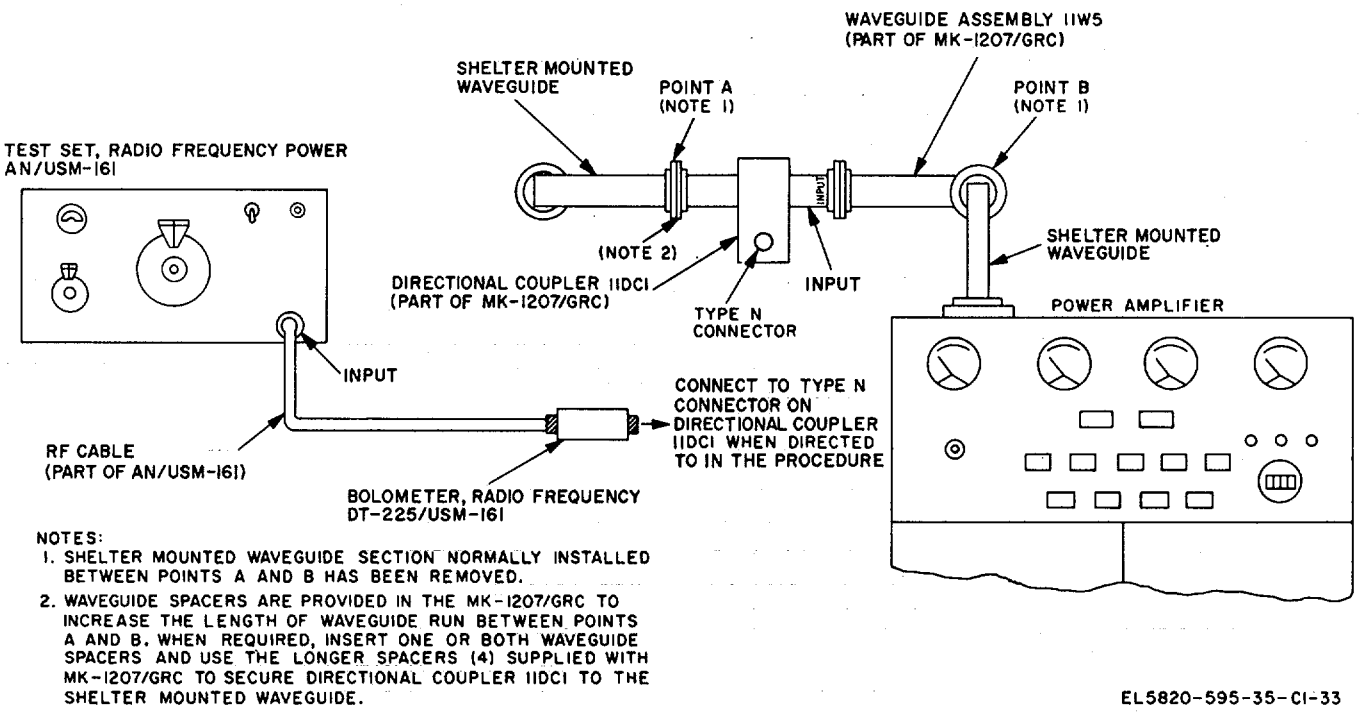


Figure 5-21. Power amplifier forward power metering circuit calibration test setup for power amplifier mounted on roadside of Shelter S-438/TRC-121.

WARNING

Voltages in excess of 7,000 volts are present in the power amplifier when beam power is applied to power amplifier klystron tube 3A9V1. Do not set the BEAM POWER circuit breaker 3A9AiCB2 (fig. 5-22) to ON while performing this procedure.

d. Turn the CURRENT ADJUST control on meter calibration test set 11Al fully counterclockwise.

e. Connect the equipment as shown in figure 5-22.

f. Turn DC OVLD ADJ potentiometer 3A6R19 (fig. 5-22) fully counterclockwise.

g. Slowly turn the CURRENT ADJUST control on meter calibration test set 11A1 clockwise until the reference meter indication on meter I calibration test set 11A1 reaches. 55 amperes.

h. Power amplifier BEAM CURRENT meter indication should be .55 amperes. If it is not, perform the adjustment given in i below. Otherwise, proceed to j below.

i. Using a screwdriver, adjust BM I CAL potentiometer 3A9A23R12 (fig. 5-22) for a BEAM CURRENT meter indication of .55. If a meter indication of .55 cannot be obtained, refer to the power amplifier troubleshooting chart (item 27, para 5-3d) for corrective action.

j. (Not used.)

k. Slowly turn DC OVLD ADJ potentiometer 3A6R19 (fig. 5-22) clockwise until DC OVERLOAD indicator on power amplifier meter panel lights red. If DC OVERLOAD indicator does not light red for full adjustment of potentiometer 3A6R19, refer to the power amplifier troubleshooting chart (item 27, para 5-3d) for corrective action.

l. Turn the CURRENT ADJUST control on meter calibration test set 11A1 fully counter clockwise

m. Press the RESET pushbutton on the power amplifier meter panel. The DC OVERLOAD indicator should light green.

n. Slowly turn the CURRENT ADJUST control on meter calibration test set 11A1 clockwise until DC

OVERLOAD indicator on power amplifier meter panel lights red.

o. BEAM CURRENT meter indication should be .55 ± 0.02 amperes. If it is not, return to d above and perform the adjustment/calibration again.

p. Slowly rotate the CURRENT ADJUST control on meter calibration test set 11Al clockwise until reference meter indication on meter calibration test set 11Al reaches 1. 0 ampere.

q. Observe indication on power amplifier BEAM CURRENT meter. If indication is not .95, perform the adjustment given in r below. Otherwise, proceed to s below.

r. Using a screwdriver, adjust BM DIODE potentiometer 3A9A23R13 (fig. 5-22) for a BEAM CURRENT meter indication of .95. If a .95 meter indication cannot be obtained, refer to the power amplifier troubleshooting chart (item 28, para 5-3d) for corrective action.

s. Turn meter -calibration test set 11A1 off and disconnect the test leads (fig. 5-22).

t. Press the RESET pushbutton on the power amplifier meter panel. The DC OVERLOAD indicator should light green.

u. Set BEAM POWER circuit breaker 3A9A1CB2 (fig. 5-22) to ON.

v. Press the BEAM SWITCH on the power amplifier meter panel. The BEAM SWITCH and BEAM indicators on the power amplifier meter panel should light green.

5-25. Power Amplifier Antenna Mismatch Trip Point Adjustment and Reflected Power Metering Circuit Calibration

a. Turn the AN/USM-161 on and allow a 30minute warmup period. After the warmup period, calibrate the AN/USM-161 using the procedure given in TM 11-6625-498-12.

b. On the power amplifier, press the BEAM SWITCH and then the MAIN POWER SWITCH. The BEAM SWITCH will light red and then be extinguished when the MAIN POWER SWITCH lights white.

c. Record the transmitter operating frequency and then set the controls on frequency synthesizer 1A14 and 4.4to 5.0-GHz bandpass filter 1FL3 to 4800.0 MHz.

d. On the power amplifier, set attenuator control 3A9AT1 (fig. 5-23) fully counterclockwise for maximum attenuation.

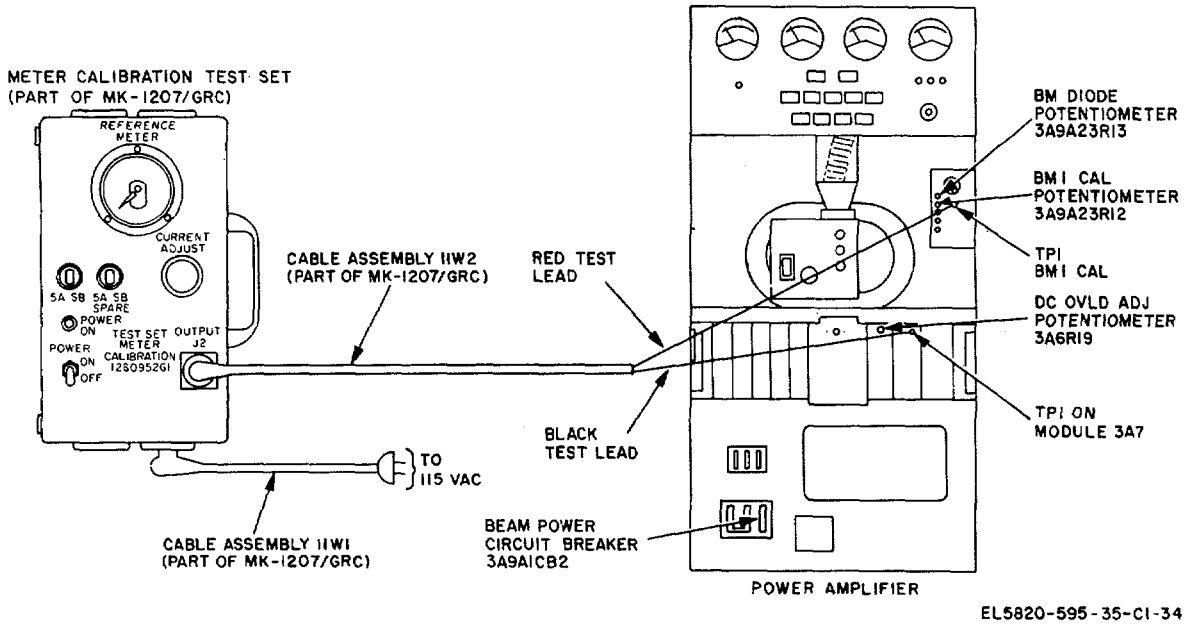


Figure 5-22. Power amplifier do overload trip point adjustment and beam current metering circuit calibration test setup.

e. Refer to the calibration plate on CN-845/USM-161 (fig. 5-23) and calculate the correction factor for a 4800-MHz INPUT. Record.

f. On the AN/USM-161, set the BIAS-READ switch to READ, turn the POWER RANGE switch to 10 MW +10 DBM, set the COMP ATTENUATOR dial to the value recorded in e above, and set the POWER indicator dial for a dial scale indication of .375 on the outermost scale.

g. Disconnect coaxial cable 3A9W4 from RF input connector 3A9VIP1 (fig. 5-5) and then connect 3A9W4 to the test equipment as shown in figure 5-23.

h. Turn attenuator control 3A9AT1 clockwise until a null indication is obtained on the AN/USM-161 NULL INDICATOR meter.

i. Remove the blue cap over ANT MIS potentiometer 3A4R16 (fig. 5-23) and turn the potentiometer fully counterclockwise.

j. Disconnect connector adapter 3A9CP1 from connector J1 on directional coupler 3A9DC2 (fig. 5-23).

k. Disconnect type N female to female adapter 11CP1 from CN-845/USM-161 and connect type N female to female adapter 11CPl to connector adapter 3A9CP1.

l. Turn the AN/USM-161 off and disconnect the test equipment.

m. Press the ANTENNA REFLECTED WATTS pushbutton on the power amplifier meter panel.

n. Adjust OUT REFL potentiometer 3A9A23R18 (fig. 5-23) for a RF MONITOR meter indication of 100. If a meter indication of 100 cannot be obtained, refer to the power amplifier troubleshooting chart (item 30, para 5-d) for corrective action.

o. Press the MAIN POWER SWITCH on the power amplifier meter amplifier meter panel. The MAIN POWER SWITCH shall light green and the BEAM SWITCH shall light red.

p. Press the RESET pushbutton on the power amplifier meter panel if the ANTENNA MISMATCH indicator is lighted red.

q. Turn ANT MIS potentiometer 3A4R16 clockwise until the ANTENNA MISMATCH indicator lights red. RF MONITOR meter indication should be 101.5 i 11.5. If it is not, refer to the power amplifier troubleshooting chart (item 29, para 5-3d) for corrective action.

r. Turn attenuator control 3A9AT1 counterclockwise until RF MONITOR meter indication reaches 50.

s. Press the MAIN POWER SWITCH on the power amplifier meter panel. The BEAM SWITCH shall be extinguished and the MAIN POWER SWITCH shall light white.

t. Disconnect type N female to female adapter 11CP1 from connector adapter 3A9CP1 and reconnect 3A9CP1 to connector J1 on directional coupler 3A9DC2.

u. Disconnect Adapter UG-29B/U from coaxial cable 3A9W4 and then reconnect 3A9W4 to RF input connector 3A9V1P1 (fig.5-5).

v. Press the MAIN POWER SWITCH on the power amplifier meter panel. The MAIN POWER SWITCH shall light green and the BEAM SWITCH shall light green and the BEAM SWITCH shall light red.

w. When the TIME DELAY indicator on the power amplifier meter panel lights green (approximately 4 minutes after the MAIN POWER SWITCH was pressed), press the BEAM SWITCH on the power amplifier meter panel. It should light green.

x. Reset the transmitter and power amplifier controls to the original operating frequency recorded in c above, and tune the power amplifier (TM 11-5820-12).

5-26. Power Amplifier Filament Voltage Adjustment and Metering Circuit Calibration

a. If a shelter-mounted precision ammeter is used to monitor either side of the balanced 230 vac input to the power amplifier, proceed to f below.

b. Deenergize the power amplifier (para 3-12).

c. Set the ME-202B/U RANGE control to 500, AC-DC polarity control to +, voltage readout dials to 0, NULL control to VTVM, and the power switch to ON. Allow a 10ninute warmup period.

d. Connect the ME-202B/U test leads to FILAMENT VOLTAGE meter 3A9M2 terminal 1 (terminal nearest the front panel) (fig. 5-2 and 5-14). Set the ME-202B/U AC-DC control to AC, and advance the OPERATE-CALIBRATE control to CALIBRATE position and while holding the control in that position adjust the CALIBRATE control for a zero indication on the VOLTS meter.

e. Energize the power amplifier (para 3-13).

NOTE

The ME-202B/U A voltage readout dial control changes the internal voltage of the ME-202/U the greatest amount and the E voltage readout dial control changes the internal voltage the least amount.

f. Set the ME-202B/U NULL control to 1 and adjust the voltage readout dial controls for a zero indication on the VOLTS meter. Repeat this step with the NULL control set to .10 and then to .01.

g. Record the voltage indicated .by the ME-202B/U voltage readout dials. Be sure to note the location of the decimal indication. This is the ac input voltage on one side of the balanced 2301

vac input to the power amplifier. Position ME-202B/U Null control to 10.

h. Deenergize the power amplifier(para 3-12).

i. Refer to figure 5-24 and determine the power amplifier filament voltage required for the ac input voltage recorded in g above is 115 vac, then the filament voltage required is 6.4 vac as indicated in figure 5-24.

j. Loosen the captive screw securing high voltage interlock door in position (fig. 5-1) and lower the high voltage interlock door.

k. Connect the ME-202B/U test leads to terminals of 3A9J5 and 3A9J6 (fig. 5-6 and 5-25).

WARNING

Voltages in excess of 7,000 volts are applied to 3A9J5 and 3A9J6 when beam power is applied to power amplifier klystron tube 3A9V1. Do not set BEAM POWER circuit breaker 3A9A1C2 to ON when energizing the power amplifier in 1 below.

l. Energize the power amplifier as follows: (1) Connect the external ac power input cable to AC POWER INPUT connector J1 (fig. 5-9).

(2) Set MAIN POWER, KLYSTRON BLOWER, CONTROL POWER, and CABINET FANS circuit breakers to ON.

(3) Press the MAIN POWER SWITCH on .the power amplifier meter panel. The MAIN POWER SWITCH indicator shall light green.

(4) Wait approximately 4 minutes (until TIME DELAY indicator lights green) and proceed to m below.

m. Advance the ME-202B/U OPERATECALIBRATE control to CALIBRATE position and while holding the control in that position adjust the CALIBRATE control for a zero indication on the VOLTS meter.

n. Set the ME-202B/U RANGE control to 50 and the NULL control to 1.

o. Adjust the ME-202B/U voltage readout dial controls for a zero indication on the VOLTS meter. Repeat this step with the NULL control set at .10 and then at .01. Read the voltage indicated on the voltage readout dial. Be sure to note the location of the decimal indication. If the indication is not the same as the filament voltage required (determined in i above), perform the adjustment given in p below. If the indication is the same, proceed to q below.

p. On the ME-202B/U, adjust the voltage readout dial controls so that the voltage readout dials indicate the same voltage as determined in i above. Using a screwdriver, adjust FILAMENT VOLT ADJ potentiometer 3A9R4 (fig. 5-14) for a zero indication on the ME-202B/U VOLTS meter. If potentiometer 3A9R4 cannot be adjusted to obtain the filament voltage required, refer to the power amplifier troubleshooting chart (item 31, para 5-3d) for corrective action.

q. Observe indication on power amplifier FILAMENT VOLTAGE meter 3A9M2. If its indication is not the same as the indication on the ME-202B/U voltage readout dials, perform the adjustment given in r below. Otherwise, proceed to s below.

r. Using a screwdriver, adjust FIL M CAL potentiometer 3A9R5 (fig. 5-14) for a FILAMENT VOLTAGE meter indication that corresponds to the voltage indicated on the ME-202B/U voltage readout dials. If potentiometer 3A9R5 cannot be adjusted to obtain the required FILAMENI VOLTAGE meter indication, refer to the power amplifier troubleshooting chart (item 32, par 5-3d) for corrective action.

s. Deenergize the power amplifier (para 3-12).

t. Disconnect the ME-202B/U test leads from terminals on 3A9J5 and 3A9J6.

u. Close the high voltage interlock door (fig. 5-1) and secure it with the captive screw.

v. Energize the power amplifier (para 3-13).

5-27. Power Amplifier Filament Current Sensing Check

a. Press the BEAM SWITCH on the power amplifier meter panel. The BEAM SWITCH and BEAM indicators on the power amplifier meter panel shall light red.

b. Set BEAM POWER circuit breaker 3A9A1CB2 (fig. 5-22) to OFF.

c. Connect a test lead (supplied with TS-656/U) between TP2 and TP3 on the time-delay control module 3A5.

d. Observe that the FILAMENT indicator on the power amplifier meter panel is lighted red. If the FILAMENT indicator does not light red, replace time delay control module 3A5 (TM 11-5820-595-12) and repeat the filament current check. If the FILAMENT indicator still does not light red, replace indicator control module 3A2 and repeat the filament current. sensing check. If the FILAMENT indicator still does not light red, refer to the power amplifier troubleshooting chart (item 33, para 5-3d) for corrective action.

e. Remove the test lead from TP2 and TP3 on time-delay control module 3A5.

f. Set BEAM POWER- circuit breaker 3A9A1CB2 (fig. 5-22) to ON.

g. Press the BEAM SWITCH on the power amplifier meter panel. The BEAM SWITCH and BEAM indicators on the power amplifier meter panel shall light green.

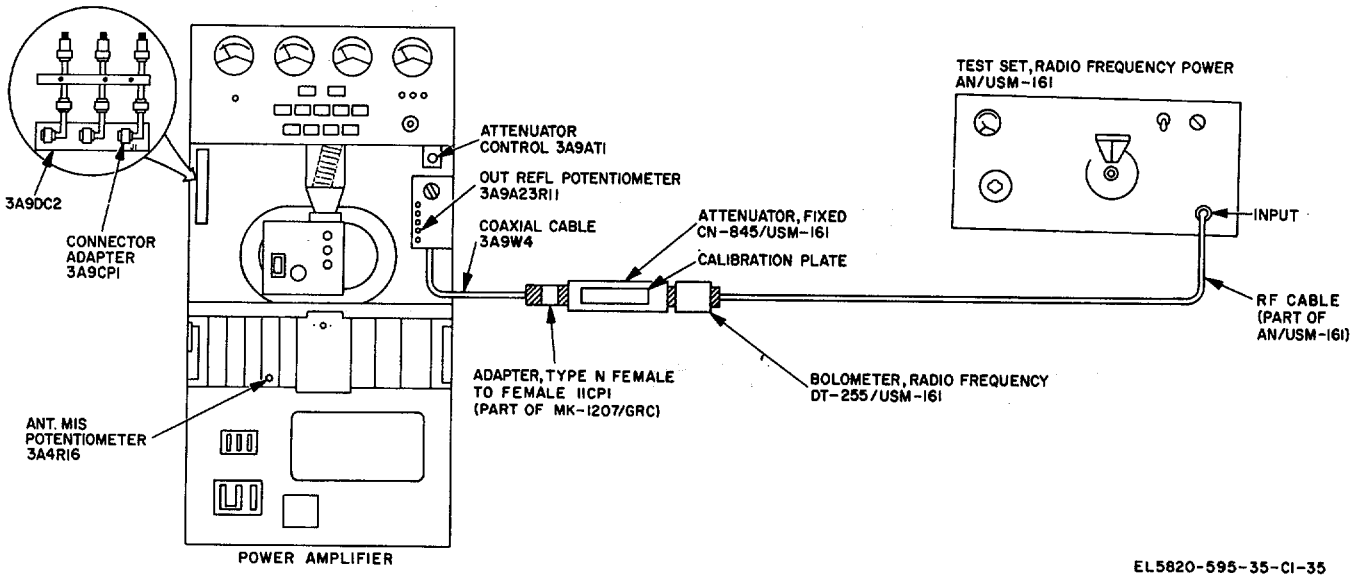


Figure 5-23. Power amplifier antenna mismatch trip point adjustment and reflected power metering circuit calibration test setup.

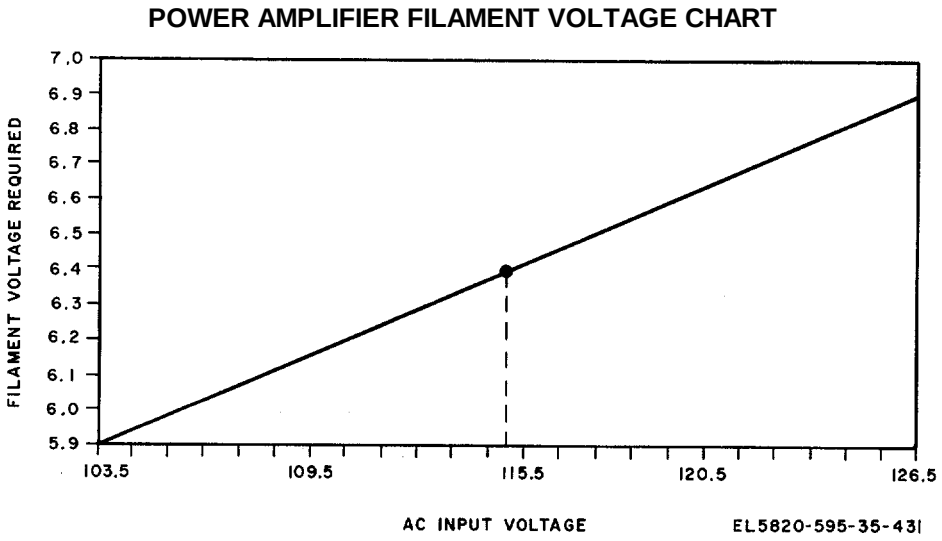


Figure 5-24. Determining power amplifier filament voltage.

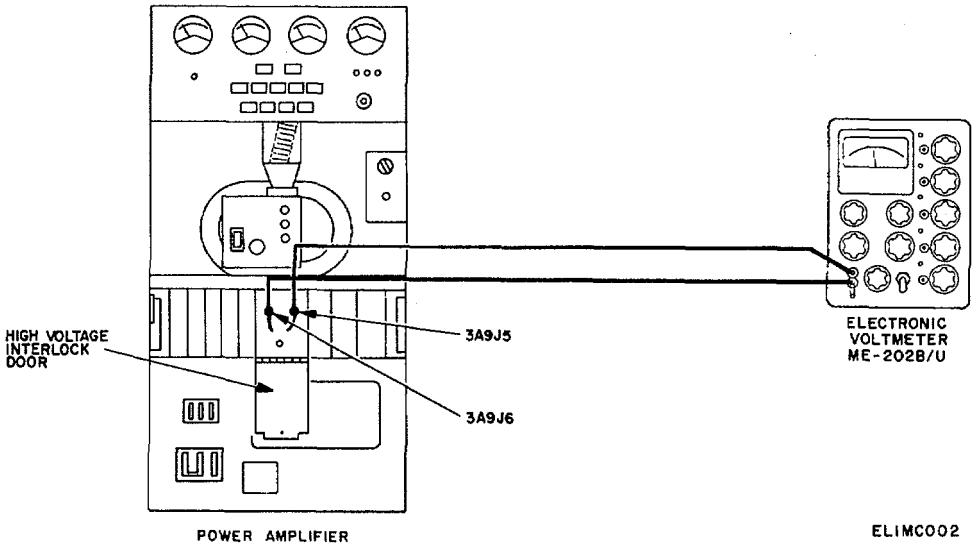


Figure 5-25. Power amplifier filament voltage adjustment and metering circuit calibration test setup.

CHAPTER 6
DIRECT SUPPORT MAINTENANCE FOR ANCILLARY EQUIPMENT

6-1. General Information

This chapter contains the maintenance instructions required to maintain the antenna alignment indicator. The maintenance instructions include alignment indicator 4A7 meter calibration and replacement of parts. Maintenance repair parts for Handset A-156/U are in TM 11-5820-595-35P.

6-2. Calibration of Antenna Alignment Indicator Meters 4A7M1 and 4A7M2

a. Turn the TS-656/U on and allow a 5-minute warmup period.

b. Set ON-OFF (TRANSIT) switch on antenna alignment indicator 4A7 to OFF (TRANSIT).

c. Adjust the meter zero screw on front of meters 4A7M1 and 4A7M2 for a zero meter indication on the respective meters.

d. On the TS-656/U, set the FUNCTION switch to DIR CUR, set the CURRENT switch to 100 MICRO-AMP, and rotate the DECREASE/ INCREASE control counterclockwise until the mechanical stop is reached.

e. Connect the red test lead supplied with TS-656/U between the DIR CUR terminal on TS-656/U and pin A of connector 4A7P1 (fig. 6-1).

f. Connect the black test lead supplied with TS-656/U between the COMMON terminal on TS-656/U and pin B of connector 4A7P1.

g. Set the ON-OFF (TRANSIT) switch on antenna alignment indicator 4A7 to ON.

h. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing i and j below.

i. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter 4A7M1 indicates 100.

j. Record the meter indication on TS-656/U and then release the TEST switch.

k. Disconnect the red test lead supplied with TS-656/U from pin A of connector 4A7P1 and connect it to pin E of connector 4A7P1.

l. Disconnect the black test lead supplied with TS-656/U from pin B of connector 4A7P1 and connect it to pin D of connector 4A7P1.

m. Rotate the DECREASE/INCREASE control on TS-656/U counterclockwise until the mechanical stop is reached.

n. Hold the TEST switch on TS-656/U in the raised (TEST) position while performing o and p below.

o. Rotate the DECREASE/INCREASE control on TS-656/U clockwise until meter 4A7M2 indicates 100.

p. Record the meter indication on TS-656/U and then release the TEST switch.

q. Turn the TS-656/U off and disconnect the test leads.

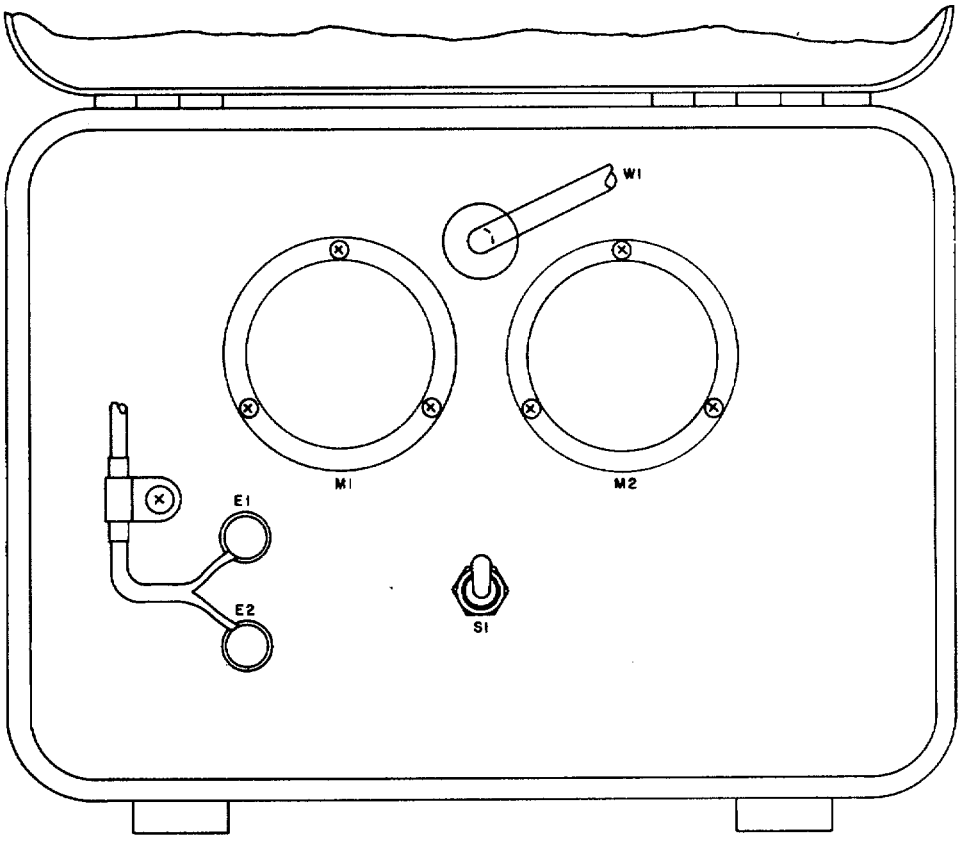
r. Meter indication recorded in j above should be 50 $\pm$ 10 microamperes. If it is not, replace meter 4A7M1 and repeat the calibration procedure.

s. Meter indication recorded in p above should be 50 $\pm$ 10 microamperes. If it is not, replace meter 4A7M2 and repeat the calibration procedure.

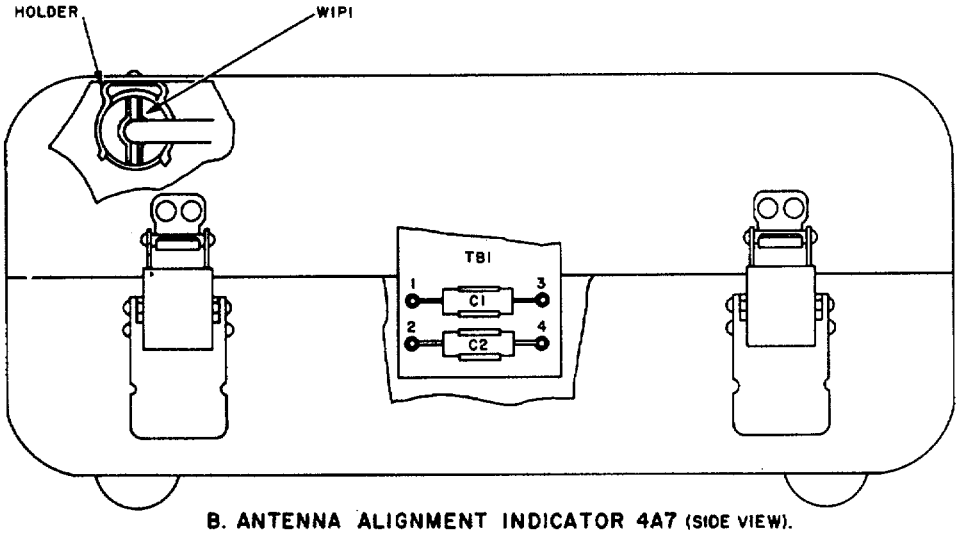
t. Set the ON-OFF (TRANSIT) switch on antenna alignment indicator 4A7 to OFF (TRANSIT).

6-3. Replacement of Parts in Antenna Alignment Indicator 4A7

The parts in antenna alignment indicator 4A7 (fig. 6-1) are easily removed and replaced and require no special removal or replacement procedures. To gain access to parts mounted beneath the antenna alignment indicator meter panel (fig. 6-1), remove the 12 screws securing the meter panel to the chassis inclosure; then lift the meter panel and turn it over to expose all the parts.



A. ANTENNA ALIGNMENT INDICATOR 4A7 (TOP VIEW).



B. ANTENNA ALIGNMENT INDICATOR 4A7 (SIDE VIEW).

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 4A7.

EL5820-595-35-220

Figure 6-1. Antenna alignment indicator 4A7, pa location.

CHAPTER 7

DEPOT MAINTENANCE

Section I. REPAIRS

7-1. General

a. This chapter provides procedures to be accomplished as depot maintenance and supplements those covered for lower categories of maintenance. Repair instructions in this section are supplied only for those assemblies requiring special techniques or a sequence of steps which are not readily obvious.

b. Assembly repair consists primarily of removal and replacement procedures for defective subassemblies or piece parts, as applicable. Instructions for transmitter assemblies are covered in paragraphs 7-4 through 7-9; receiver assemblies are covered in paragraphs 7-9 through 7-12; and power amplifier assemblies are covered in paragraphs 7-13 and 7-14. Repair and replacement of connectors are covered in paragraph 7-15.

c. Page-sized illustrations (figs. 7-1 through 7-60), pertaining to depot maintenance are located at the end of this chapter. Other illustrations required for depot maintenance are fold out illustrations and are located in chapter 8. Wiring diagram and parts location illustrations for the transmitter are shown in figures 7-7 through 7-40 and 8-74 through 8-102; receiver illustrations are figures 7-41 through 7-48 and 8-103 through 8-115; power amplifier illustrations are figures 7-49 through 7-59 and 8-116 through 8-124. Diagrams covering integrated circuits are shown in figure 8-18.

7-2. General Parts Replacement Techniques

a. General instructions on parts replacement techniques for direct support maintenance (para 3-11, transmitter; 4-12, receiver; and 5-6, power amplifier) must also be observed during depot maintenance activity.

b. Procedures for the replacement of conformal coating removed from printed wiring boards during repair are covered in paragraph 7-16.

7-3. Equipment Required

Tools and materials required to perform repairs in this section are listed below:

a. Toolkit, Radio Repair TK-100/G, FSN 5180-605-0079.

b. Toolkit, Electronic Equipment TK-105/G, FSN 5180-610-8177.

c. Crimping tool MS 3191-4 with head assembly W25, FSN 5120-230-3771.

d. Extraction tool MS 18278, Size 20, FSN 5120-230-3770.

e. Extraction tool CET-C6B, FSN 5120-963-7661.

7-4. Repair of Frequency Mixer 1A9

Frequency mixer 1A9 contains 4.4to 5.0-GHz circulator 1A9HY1, replaceable at direct support level (para 3-23) and is nonrepairable, and crystal mixer 1A9A1, replaceable at organizational maintenance level (TM 11-5820-595-12). For depot repair of crystal mixer lA9A1, specific instructions are provided for the replacement of crystal diode 1A9A1CR1. A parts location diagram for frequency mixer 1A9 is provided in figure 882. Instructions for the removal and replacement of crystal diode 1A9A1CR1 are provided in a and b below.

CAUTION

Before handling crystal diode 1A9A1CR1, ground yourself to equipment case ground in order to dissipate any static charge.

a. Removal of Crystal Diode 1A9A1CR1.

(1) Remove 1A9A1 from case of 1A9 and remove the four screws securing connector 1A9A1J2 to crystal mixer 1A9A1 and pull connector 1A9A1J2 out of crystal mixer 1A9A1.

(2) Using long-nose pliers, extract crystal diode 1A9A1CR1 from connector 1A9A1J2.

b. Replacement of Crystal Diode 1A9A1CH1.

NOTE

Check solder connections on connector 1A9A1J2 for signs of cracks or looseness. If there is any sign of cracks or looseness, resolder connections.

(1) Observe orientation when replacing crystal diode 1A9A1CR1. The correct orientation is stamped on the cover of crystal mixer 1A9A1. Coat the cathode of diode 1A9A1CR1 with Dow Corning No. 340 heat sink compound and insert the anode end into diode holder on connector 1A9AlJ2.

(2) Insert 1A9AlJ2, with lA9A1CRI, into cavity 1A9AlZ1, being certain that the cathode of 1A9A1CR1 is seated properly within 1A9AlZ1, and that choke is installed in an upward position.

(3) Secure connector 1A9AlJ2 in place with four screws removed in a (1) above and replace 1A9A1 into 1A9.

7-5. Repair of Frequency Multiplier Group 1A10 (figs. 7-1 and 8-83)

The 2d frequency multiplier 1A10A1 and 3d frequency multiplier lAlOA2 are replaced at the organizational maintenance level (TM 11-5820-595-12). The 2275to 2425-.MHz circulator 1A10HY1 is replaced at the direct support maintenance level (para 3-4). Depot repair of these assemblies consists of replacing defective piece parts. Precautionary measures should be observed in replacement of varactor diodes 1A10A1CR1 and 1A10A2CR1. Removal and replacement procedures for 1A10A1CRI and 1A10A2CR1 are provided below. See figure 883 for frequency multiplier group lA10 parts location.

a. Removal and Replacement of Varactor Diode 1A10A1CR1. To replace varactor diode 1A10A1CR1 proceed as follows:

(1) Remove the 10 screws securing cover on 2d frequency multiplier 1A10A1 and remove cover (fig. 8-83).

(2) Rotate tuning plunger adjustment screw for cavity 1A10A1Z1C counterclockwise to pull tuning plunger (fig. 7-1) into contact plunger. Continue until tuning plunger is inside contact plunger.

(3) It should be noted that as (2) above was performed, a spring within the sleeve pushed out on the coupling and kept the cup in contact with the tuning' plunger. The end of the spring is now out well beyond the end of the sleeve and is flexible. Lift the coupling and cup (as a unit) off end of spring. Do not separate the coupling and cup: there are three small nylon spacers between them which must not be lost.

(4) Remove the spring from the sleeve. Rotate the sleeve one turn clockwise, as viewed from cavity lAlOAlZ1C.

(5) Remove the hex nut securing the contact plunger in cavity 1A10A1Z1C. Unscrew the contact plunger and remove it from cavity 1A10A1Z1C.

(6) Remove setscrew from access hole in outside wall of cavity 1A10A0Z1C.

(7) Insert small screwdriver through access hole ((6) above) and unscrew the nut securing coupling disc (fig. 7-1, view b) to capacitor lAlOAlC3 assembly. Remove the nut, coupling disc, diode holder strap and varactor diode 1A10A1CR1.

(8) Apply a small amount of Dow Corning No. 340 heat sink compound to the cathode of replacement varactor diode 1A10A1CR1.

(9) Observe cathode orientation of the new varactor diode; the correct orientation for insertion is shown in figure 7-1. Insert the cathode end of varactor diode 1A10A1CR1 into seat in wall of cavity 1A10A1Z1C.

(10) Replace diode holder strap, coupling disc and tighten nut on shaft of capacitor 1A10A1C3 assembly.

(11) Replace contact plunger in cavity 1A10A1Z1C. Be sure it is screwed all the way in, then secure it in place with the hex nut removed in (5) above. Tighten hex nut firmly.

(12) Rotate sleeve ((4) above) one turn counterclockwise.

(13) Insert spring into sleeve, then replace cup and coupling.

(14) Replace setscrew, removed in (6) above, in the access hole. Check that setscrew is flush with inside surface of cavity wall and does not extend into cavity 1A10A1Z1C.

(15) Replace cover and secure with the 10 screws removed in (1) above.

b. Removal and Replacement of Varactor Diode 1A10A2CR1.

(1) Hold 3d frequency multiplier 1A10A2 in the vertical position with connector 1A10A2J1 facing up and unscrew diode holder (center screw, fig. 7-2) approximately three complete turns.

(2) Unscrew plunger and pull plunger, diode holder, and varactor diode 1A1OA2CR1 out of cavity. (If necessary use tweezers to extract 1AlOA2CR1 from seat in crossbar.)

(3) Coat cathode of new varactor diode with heat sink compound Dow Corning No. 340 and install cathode end of varactor diode 1A1OA2CR1 into diode holder. (Refer to fig. 7-2 to determine 1A1OA2CR1 orientation.)

(4) Unscrew diode holder from plunger until several turns of diode holder threads are visible.

(5) Hold 3d frequency multiplier 1A1OA2 in the vertical position and screw the plunger with the attached varactor diode 1A1OA2CR1, and diode holder, into the cavity until plunger bottoms; then, screw in the diode holder until 1A1OA2CR1 gently, but firmly, bottoms into position.

7-6. Repair of Amplifier-Frequency Multiplier 1A11

Depot repair of amplifier-frequency multiplier 1A11 consists of defective parts replacement. Parts location for amplifier-frequency multiplier 1All is provided in figure 8-85. Particular instructions for replacement of varactor diodes and transistors are provided below.

a. Removal and Replacement of Varactor Diodes 1A11 CR4 and CR5.

(1) Remove the 22 screws securing top cover on amplifier-frequency multiplier 1All and remove cover (fig. 8-85).

(2) Remove the 30 screws securing heat sink on amplifier-frequency multiplier 1All and remove heat sink.

(3) Locate the diode holder of the defective varactor diode (CR4 or CR5) on the bottom of amplifier-frequency multiplier 1All and unscrew diode holder from the module.

(4) Remove defective varactor diode from diode holder.

(5) Observe cathode orientation of the new varactor diode; the correct orientation for insertion is shown in figure 7-3.

(6) Fill diode cathode cavity of diode holder approximately half full of Dow Corning No. 34 heat sink compound and insert cathode end of varactor diode into diode holder.

(7) Insert diode holder and varactor diode into the module. Be certain that the anode end of the varactor diode is properly seated in diode retainer and screw diode holder into the base of the module.

b. Replacement of Transistors. Several transistors require special attention when replaced:

(1) For transistors Q1, Q2, Q4 and Q5, keep emitter leads as shorts as possible and solder fill to the termination point.

(2) On transistors Q3, Q4 and Q5 use the entire length of the base lead to form a loop to the top of the variable capacitor.

7-7. Repair of Digital Data Modem 1A12

a. General. The digital data modem contains 12 plug-in printed boards replaceable at the organizational maintenance level. Digital data modem depot repair entails parts replacement on printed wiring boards 1A12A2 through 1A2A13 and on digital data modem chassis 1A12A15. Location of parts on printed wiring boards is shown in figures 8-86 through 8-96. No special instructions are required for printed wiring board parts replacement. Digital data modem chassis 1A12A15 parts location is provided in figures 7-20, 7-21, and 7-22.

b. Disassembly of Digital Data Modern Chassis 1A12A15.

(1) Remove four screws on rear cover of digital data modem chassis and remove test cover.

(2) Remove two screws; each one located between each jack pair, J1 and J2, and J3 and J4.

(3) Turn digital data modem chassis upside down and remove two screws on outside of chassis case.

(4) On printed wiring board connector rack, remove four screws securing digital data modem chassis to chassis case.

(5) Slide digital data modem chassis out back end of chassis case thereby allowing access to all parts.

c. Reassembly of Digital Data Modem Chassis 1A12A15.

(1) Slide the digital data modem chassis into chassis case.

(2) Replace and tighten four screws securing printed wiring board connector rack to chassis case.

(3) Replace and tighten two screws removed in b(2) above.

(4) Turn digital data modem chassis upside down. Replace and tighten two screws removed in b(3) above.

(5) If a printed wiring board connector (lA12Ai5XA2 through 1A12A15XA13) has been

replaced, use the printed wiring board that mates with the connector as a gauge in aligning the replacement printed wiring board connector as follows:

(a) Loosen two screws securing replacement printed wiring board connector on printed wiring board connector rack.

(b) Insert mating printed wiring board into guide rails for replacement of printed wiring board connector and slowly slide it back until firmly seated in printed wiring board connector. Tighten two screws securing printed wiring connector to printed wiring board connector rack. Remove printed wiring board.

(c) Repeat (a) and (b) above for each of the replacement printed wiring board connectors (1A12A15XA2 through 1A12A15XA13).

(6) Insert rear cover on back of digital data modem chassis and secure with four screws removed in b(1) above.

7-8. Repair of Order Wire Assembly 1A13

Order wire assembly 1A13 contains one plug-in printed wiring board (1A13A1) module and four plug-in printed wiring boards (1A13A2 through 1A13A5) replaceable at organizational level, and an order wire chassis (1A13A7) replaceable at direct support level. Depot repair of these assemblies is piece part replacement. Parts location for printed wiring boards 1A13A1 through 1A13A5 is provided in figures 8-97 through '8-102. Parts location for order wire chassis 1A13A7 is shown in figure 7-25. No special instructions are required for depot level disassembly and piece part replacement.

7-9. Repair of Frequency Synthesizer 1A14 and 2A21

With the exception of reference designators, frequency synthesizer 1A14 in the transmitter is identical to frequency synthesizer 2A21 in the receiver. Frequency synthesizer lA14 contains six repairable plug-in printed wiring board modules (lA14A1 through 1A14A6) and two nonrepairable plug-in modules (1A14A7 and 1A14A8) all replaceable at organizational level (TM 11-5820-595-12). Main chassis lA14A10 is replaceable at direct support level. With the exception of the two nonrepairable plug-in modules, depot repair of these assemblies is piece part replacement. Parts location and wiring diagrams for printed wiring board modules 1A14A1 through 1A14A6 are shown in figures 7-29 through 7-40. Electrical parts locations on main chassis 1A14A10 are shown in figures 7-27 and 7-28. No special instructions are required for depot level disassembly and piece part replacement.

7-10. Repair of Mixer Preamplifier 2A4 and 2A11

Depot repairs to mixer preamplifier 2A4 and 2All (figs. 7-41 and 8-103) consists of replacement of defective parts. Special consideration must be given to the replacement of matched pair crystal diodes ZlCR1 and Z1CR2 as indicated below.

CAUTION

Before handling crystal diodes, ground yourself to equipment case ground to dissipate any existing static charge.

a. Removal of Crystal Diodes ZICR1 or Z1CR2.

(1) Using a screwdriver, unscrew and remove diode cover screw covering the defective crystal diode (fig. 7-41).

(2) With long-nose pliers, grasp the diode base and extract the diode base and the crystal diode from the assembly.

(3) Pull crystal diode from diode base.

b. Replacement of Crystal Diodes Z1CR1 or Z1CR2.

(1) Note cathode orientation when replacing the crystal diode. Orient the replacement crystal diode in accordance with the polarity stamped on the assembly and insert crystal diode into the diode base, insuring positive seating.

(2) Insert crystal diode .(with base) into the mixer preamplifier.

(3) Replace and firmly secure diode cover screw.

7-11. Repair of Frequency Multiplier Group 2A7

Frequency multiplier Group 2A7 (fig. 8-106) repair is comprised of replacing defective 4550to 4850-MHz power divider 2A7HY2, and defective parts in 2d frequency multiplier 2A7A1 and 3d frequency multiplier 2A7A2. Varactor diode replacement procedures are similar to those for frequency multiplier group A1o0 ;(para 7-L5) as indicated below.

a. Removal and Replacement of Varactor Diode CR1, 2d Frequency Multiplier 2A,7A1. Remove the nine screws securing cover on 2d frequency multiplier 2A7A1 and remove cover (fig. 8-106).

Follow the procedures in paragraph 7-5a for replacement of varactor diode CR1 and see figure 7-4 for paragraph 7-5a (2) and (7).

b. Removal and Replacement of Varactor Diode CR1, 2d Frequency Multiplier 2A7A2. The 3d frequency multiplier, 2A7A2, is physically similar to 3d frequency multiplier 1A1OA2 (fig. 7-2). With reference to paragraph 7-5b for replacement of CR1 see figures 8-106 and 7-2.

7-12. Repair of Amplifier-Multiplier 2A8

Amplifier-multiplier 2A8 (figs. 8-107 and 8-108) depot repair is the replacement of defective parts. Special instructions for replacement of transistors and varactor diodes are provided below.

a. Replacement of Transistors Q1 and Q2.

(1) Remove the 12 screws securing the top cover on amplifier-multiplier 2A8 and remove top cover.

(2) Check orientation of transistors Q1 and Q2. The transistor case is marked with a dot or the letter C near the collector lead; also, the collector lead is notched.

(3) Cut transistor Q1 emitter leads as short as possible to minimum requirement lengths.

(4) Coat mounting studs of replacement transistors with Dow Corning No. 340 heat sink compound and replace transistors.

(5) Replace top cover and secure with the 12 screws removed in (1) above.

b. Replacement of Varactor Diodes.

(1) Remove the 12 screws securing the bottom cover on amplifier-multiplier 2A8 and remove bottom cover.

(2) Locate the diode holder of the defective varactor diode (CR2 or CR3) on the bottom of amplifier-multiplier 2A8 and unscrew the diode holder from the base of the assembly.

(3) Remove defective varactor diode from diode holder.

(4) Coat replacement varactor diode cathode with Dow Corning No. 340 heat sink compound and insert cathode end into the diode holder. Figure 7-3 is applicable for identifying varactor diode cathode.

(5) Reinsert the diode holder with the varactor diode, into the assembly. Ascertain that the anode is properly seated in the diode retainer and screw the diode holder into the assembly until tight.

(6) Replace bottom cover and secure with the 12 screws removed in (1) above.

7-13. Repair of Inverter 3A8 (figs. 7-54, 7-55, and 8-123)

During removal and replacement of defective parts care should be exercised that rectifier diodes CR6 and CR8 are not interchanged with physically similar rectifier diodes CR5 and CR7. The mounting stud is the cathode on diodes CR5 and CR7. On diodes CR6 and CR8 the mounting stud is the anode which is further identified by the suffix R after the type number.

7-14. Repair of Frequency Tuner 3A9A6 (fig. 7-5)

Frequency Tuner 3A9A6 is replaced at the direct support maintenance level (para 5-8) and repaired by replacement of defective parts at depot level. Frequency tuner 3A9A6 disassembly and reassembly procedures are provided below.

a. Disassembly of Frequency Tuner 3A9A6.

NOTE

Mark the rear top side of gear housing (21) before disassembling the frequency tuner to provide a reference during reassembly.

(1) Loosen the two setscrews securing control knob (1) to main tuning shaft (2) and remove control knob.

(2) Remove locknut (28) and lockwasher (8) securing each of the three chassis bushings (4) to front panel (3), and remove the three chassis bushings from the front panel.

(3) Remove four machine screws (5) securing front panel (3) to tuner bracket (7).

(4) Remove four machine screws (6) securing gear housing (21) to tuner bracket (7), and remove gear housing.

(5) Remove machine screw (16) and flat washer (17) securing drum (18) to gear shaft (20), and remove drum from gear shaft.

NOTE

Mark the position of collars (23 and 26) and worm gear (24) on gear shaft (20) before disassembling these parts.

(6) Drive out spring pin (25) securing worm gear (24) to gear shaft (20).

(7) Loosen the setscrews securing collars (23and 26) to gear shaft (20).

(8) Place one hand underneath bottom of gear housing (21) and pull gear shaft (20) out of gear housing (21). Set the two bearings (22 and 27), two collars (23 and 26), and worm gear (24) aside.

NOTE

Mark the position of collars (10 and 13), worm (11) and miniature sprocket (15) on main tuning. shaft (2) before disassembling these parts.

(9) Drive out spring pin (12) securing worm (11) to main tuning shaft (2).

(10) Loosen the setscrews securing collars (10 and 13) to main tuning shaft (2).

(11) Loosen setscrew securing miniature sprocket (15) to main tuning shaft (2), and remove miniature sprocket from main tuning shaft.

(12) Place one hand underneath bottom of gear housing (21) and pull main -tuning shaft (2) out of gear housing (21). Set the two bearings (9 and 14), two collars (10 and 13), and worm (11) aside.

b. Reassembly of Frequency Tuner 3A9A6.

(1) Insert main tuning shaft (2) through hole on front side of gear housing (21) and install bearing (9), collar (10), worm (11), collar (13), and bearing (14) on main tuning shaft in the sequence and position shown in figure 7-5.

(2) Align collars (10 and 13) and worm (11) with marks on main tuning shaft (2).

(3) Align worm (11) with hole in main tuning shaft and secure by driving spring pin (12) into hole.

(4) Secure collars (10 and 13) to main tuning shaft (2) by applying light pressure with setscrews. Do not firmly tighten setscrews at this time.

(5) Insert gear shaft (20) through hole on right side of gear housing (21) and install bearing (22),' collar (23), worm gear (24), collar (26), and bearing (27) on gear shaft in the sequence and position shown in figure 7-5.

(6) Align collars (23 and 26) and worm gear (24) with marks on gear shaft (20).

(7) Align worm gear (24) with hole in gear shaft (20) and secure worm gear to gear shaft by driving spring pin (25) into hole.

(8) Secure collars (23 and 26) to gear shaft (20) by applying light pressure with setscrews. Do not firmly tighten setscrews.

(9) Turn-main tuning shaft (2) by hand and' check that gears mesh and operate smoothly without undue binding. If gears do not mesh or tuning is difficult, check positioning of bearings and collars on gear shaft and main tuning shaft and readjust their positions as required.

(10) When main tuning shaft (2) can be turned smoothly, tighten the setscrew on each of the following collars (10, 13, 23, and 26).

(11) Install miniature sprocket (15) on main tuning shaft (2) and align the miniature sprocket with marking on main tuning shaft.

(12) Secure miniature sprocket (15) to main tuning shaft (2) by tightening the setscrew.

(13) Install drum (18) on protruding end of gear shaft (20).

(14) Replace and tighten flat washer (17) and machine screw (16) to secure drum (18) to gear shaft (20).

(15) Insert main tuning shaft (2) through hole in tuner bracket (7) and align the four holes on front of gear housing (21) with mounting holes on tuner bracket (7).

(16) Replace and tighten' machine screws (6) securing gear housing (21) to tuner bracket (7).

(17) Install front panel (3) to tuner bracket (7) and secure by tightening four machine screws (5) removed in a(3) above.

(18) Install chassis bushings (4) removed in a(2) above and secure each chassis bushing with a lockwasher (8) and locknut (28).

(19) Install control knob (1) on main tuning shaft (2) and tighten setscrews on control knob.

7-15. Repair and Replacement of Connectors

a. General. Connector repair consists of the replacement of the defective connector (solder type nonremovable contacts) or the replacement of the defective connector contacts (crimp type removable contacts). Connectors on assemblies to be repaired at depot level are identified in b (transmitter), c (receiver), and (power-amplifier) below. Also specified are applicable tools and reference paragraphs which detail the required repair procedures.

b. Transmitter Module Connectors.

Connector	Extraction /insertion tool	Crimping tool	Procedure paragraph	Figure reference
1A2P3	MS 18278 Size 20/none	MS 3191-4 with head assy W25	3-32c	8-75
1A3P1	Same	Same	32c	7-14(1)
1A4P1	Same	Same	3-32c	7-16(1)
1A5P1	Same	Same	3-32c	8-77(1)
1A7P1	Same	Same	3-32c	8-79(1)
1A8P3	Same	Same	3-32c	8-81
1AllP3	Same	Same	3-32c	8-85
1A12A15A1P1	Same	Same	3-32c	7-21
1A12A15A2P2	Same	Same	3-32c	7-21
1A13A7P2	Same	Same	3-32c	7-25
1A14A9XA4J1	Same	Same	3-32c	7-27
1A14A9XA5J1	MS 18278 Size 20/none	MS 3191-4 with head assy W25	3-32c	7-27
1A5P2-	CET-C6B/none	None required	3-32d	8-77
1A13A7P1	Same	None required	3-32d	7-25
1A14Pl	Same	None required	3-32d	7-28
1A14A9XA1J1	Same	None required	3-32d	7-27
1A14A9XA2J1	Same	None required	3-32d	7-27
1A14A9XA3J	CET-C6B-,/none	None required	3-32d	7-27
1A12A15XA2 through 1A12A15XA13	None required	None required	3-32f	7-21
1A13A7XA1 through 1A13A7XA5	None required	None required	3-32f	7-25
1A14A9XA6J1	None required	None required	3-32f	7-27
1A14XA7	None required	None required	3-32f	7-27
1A14XA8	None required	None required	3-32f	7-27
1A12A15A1XA1	None required	None required	3-32f	7-20
1A12A15A2XA2	None required	None required	3-32f	7-22

c. Receiver Module Connectors.

Connector	Extraction/insertion tool	Crimping tool	Procedure paragraph	Figure reference
2A4P1	MS18278 Size 201 none	MS 3191-4 with Head Assy W25	3-32c	7-41
2A6P5	Same	Same	3-32c	7-43
2A8P2	Same	Same	3-32c	8-108
2A9P5	Same	Same	3-32c	7-43
2A11Pl	Same	Same	3-32c	7-41
2A12P3	Same	Same	3-32c	8-109(1)
2A13P1	Same	Same	3-32c	8-111
2A14P1	Same	Same	3-32c	8-111
2A15P3	MS18278 Size 201 none	MS 3191-4 with Head Assy W25	3-32c	8-109(1)
2A17P1	MS 18278 Size 20,/none	MS 3191-4 with Head Assy W25	3-32c	8-115(1)
2A19P1	MS 18278 Size 20 /none	MS 3191-4 with Head Assy W25	3-32c	7-14(1)
2A20P1	MS18278 Size 20 /none	MS 3191-4 with Head Assy W25	3-32c	8-77
2A21A9XA4J1	MS 18278 Size 20/none	MS 3191-4 with Head Assy W25	3-32c	7-27
2A21A9XA5J1	MS 18278 Size 20/none	MS 3191-4 with Head Assy W25	3-32c	7-27
2A20P2	CET-C6B/none	None required	3-32d	8-77
2A21P1	CET-C6B/none	None required	3-32d	7-28
2A21A9XA1J1	CET-C6B/none	None required	3-32d	7-27
2A21A9XA2J1	CET-C6B/none	None required	3-32d	7-27
2A21A9XA3J1	CET-C6B/none	None required	3-32d	7-27
2A16P1	None required	None required	3-32f	8-114
2A21A9XA6J1	None required	None required	3-32f	7-27
2A21A7	None required	None required	3-32f	7-27
2A21XA8	None required	None required	3-32f	7-27

d. Power Amplifier Assembly Connectors. Refer to paragraph 3-32e for repair of connectors 3A8WIP1 and 3A8W2P2.

7-16. Repair of Conformal Coating

The following procedure describes the process and material requirements to apply a flexible polyurethane (PUR) coating to printed wiring board assemblies.

WARNING

Materials used in the following procedures are flammable and the associated vapors are explosive. All cleaning and spraying operations must be done under a hood ventilated to outside. Protective clothing, rubber gloves and eye protection must be worn. Avoid breathing vapors and skin contact with polyurethane and or catalyst. In event of contact, wash immediately with soap and water.

CAUTION

Cleanliness of the work area, work surfaces, implements, and surrounding air is essential and must be maintained during preparation and application of the conformal coating. The surrounding air must also have a relative humidity of 50 percent or less at 77 F° or equivalent.

a. Printed Circuit Board Preparation.

(1) Using medium grade sandpaper remove all sharp edges and ridges from the repaired area on the printed wiring board assembly.

(2) Make certain that all leads are bent and cut short, and replaced piece parts have been properly soldered.

(3) Clean the repaired area on the printed wiring board assembly, using Freon' TMC solution and a medium stiff nylon brush. Remove all extraneous materials such as solder flux, dust, dirt or finger prints.

(4) Use a forced drying method to remove all traces of solvent or moisture.

(5) Place repaired printed wiring board assembly under an ultraviolet light and verify that dirt and other foreign matter are removed.

(6) Vacuum bake the printed wiring board assembly at a temperature of 180° F for 4 hours.

(7) After baking, mask all areas of the printed wiring board assembly which do not require conformal coating.

(8) Vacuum clean printed wiring board assembly immediately prior to coating application.

b. Con formal Coating Preparation.

(1) The components of the coating must be mixed in accordance with the proportions listed in the chart below. To insure proper coating characteristics, a minimum Weight of 100 Grams of polyurethane (part A) must be used.

Polyurethane type	Mfr.	Components (Note, I and 2)	Pot life (Note 3)	Parts by weight
PUR	Hysol Corp.			
	PC-26M	Part A	112 Hrs.	100
		Part B		36
	PC-29M	Part A	6 Hrs.	100
		Part B		69
.	Conap Inc	Part A	6 Hrs.	100
		Part B		70

Notes:

1. Polyurethane (Part A) must be stored at the temperature specified by the manufacturer. The material should be free of any film, cloudiness, crystals or lumps. If the material exhibits any evidence of deterioration, it should be discarded.

2. Catalyst (Part B) must be stored at the temperature specified by the manufacturer. If the material exhibits any evidence of deterioration, it should be discarded.

3. Pot life is the unsable time of the mixture during which viscosity still allows application to the printed wiring board assembly.

(2) Weigh the larger quantity, Part A, first and then add Part B; using a tongue depressor, thoroughly mix part B into part A.

(3) Place container with coating solution on a clean bench and using a stir-master, stir for 15 minutes; then, allow 15 minutes for solvent gasses to leave the solution.

c. Conformal Coating Application, Circuit Side.

(1) Coating may be applied by brushing or spraying. If the spraying method is used, a Zicon Corp. closed system or equivalent should be used. The Zicon Corporation equipment permits spraying of solventless 1007c solid materials. The coating is atomized by a superheated solvent under high pressure, allowing wet film thicknesses of about .033 to .050 inches to be applied by continuous spraying.

(2) Place printed wiring board assembly on a clean surface with circuit side up.

(3) Application of the coating requires that the applier have some degree of skill to assure that thorough coverage and uniformity of the coating is maintained.

(4) Two or three successive layers of coating may be required thus minimizing the possibility of pinholes which could provide a path for ingress of moisture.

(5) Check the thickness of the coating using a wet gauge. A Imtal buildup of .0035 $\pm$ .0025 inches is adequate.

(6) Place printed wiring board assembly (coated side up) on a clean bench for a period of 2 hours thereby ensuring that all thinning solvents have been vaporized and carried off.

d. Coating Cure, Circuit Side.

(1) Place printed wiring board assembly into an air circulating oven with the coating side up.

(2) Follow the curing time periods for the various materials as indicated in the chart below.

e. Conformal Coating Application, Component Side. Follow steps described under subparagraph c, above, to coat component side.

Mfr.	Printed wiring board	
	Circuit Side	Component Side
Hysol Corp. PC-26M	4 hrs. at 1480° F	Same, plus 2 days at room temp.
PC-29M	3 hrs, at 150° F	Same, plus 2 days at room temp.
CONAP Inc.	3 hrs. at 1380 F	Same, plus 2 days at room temp.

f. Follow the curing time periods for materials used in accordance with the chart in subparagraph d, above.

Section II. TESTING

7-17. General

Testing is limited to verifying the quality of rigid coaxial cables used in the transmitter and receiver cabinets.

7-18. Equipment Required

The equipment required to perform the coaxial cable test (para 7-19) is listed below.

a. Oscilloscope HP-140A.

b. Time Domain Reflectometer, Plug-in HP-1415A.

c. Calibrated Mismatch, 1.10: 1 VSWR (Mecca Model 400-1.10).

d. Adapter, GR874-to-Type N (General Radio 874 GNP).

e. Termination, 50 ohms (Hewlett Packard HP-908A).

f. Adapter, Elbow (General Radio GR874) (two required).

g. Adapter, GR874B-to-OSMJ (Omni Spectra 21210).

h. Adapter, Type N female-to-female (UG29B/U).

7-19. Coaxial Cable Test

a. Coaxial cables are tested using Oscilloscope HP-140A with Time Domain Reflectometer, Plug in HP-1415A. The reflectometer incorporates a step generator which produces a positive-going incident wave which is fed into the coaxial cable undergoing the test. The incident and reflected waveforms are then analyzed to determine if there is a mismatch or if there are any discontinuities along the cable.

b. The oscilloscope high impedance input bridges the cable at its junction with the reflectometer step generator (via the elbow adapters). When a load impedance terminating a coaxial cable matches the cable characteristic impedance, no wave will be reflected and the oscilloscope will display only the incident voltage propagated down the cable. If a mismatch exists, part of the incident wave is reflected. The reflected voltage wave will appear on the oscilloscope display algebraically added to the incident wave. These waveforms are illustrated in views A and B, figure 7-6.

c. The quality criteria for the rigid coaxial cable used in the radio set is a VSWR of 1.1 maximum. This can be measured using the reflectometer as follows:

(1) Connect the two elbow adapters to bridge the STEP OUTPUT jack to the SIGNAL IN jack on the front panel of the reflectometer, and connect the GR874-to-N adaptor and the UG29B/ U adaptor to the SIGNAL OUT jack on the front panel of the reflectometer.

(2) Place POWER switch to ON and set the controls on the reflectometer to the following positions:

Control	*Position*
CM LINE/CM DISPLAY	200
MAGNIFIER	5
MAGNIFIER DELAY	4
REFL COEFFICIENT	0.5
SWEEP	NORMAL

(3) Connect 50 ohm termination HP908A to the SIGNAL OUT jack using the adaptors installed in step (1).

(4) Adjust the incident wave voltage step to coincide with the center screen graticule line of the oscilloscope using the VERT POSITION control.

(5) Remove the 50 ohm termination and

insert the calibrated 1.1 VSWR mismatch (Mecca model 400-1.10). Note the upward deflection point on the oscilloscope, this represents an SWR of 1.1. Therefore, the increments between the 50 ohm terminated center scale and the 1.1 SWR calibrated line indicate values of SWR between the nominal SWR and the 50 ohm termination (typically 1.05 residual SWR) and the calibrated 1.1 SWR reference line. The 1.1 SWR reference point can be adjusted to some convenient graticule line using the VERNIER CAL adjust (inner control of the REFL C,OEFFICIENT controls).

(6) Remove the calibrated mismatch from the SIGNAL OUT jack and connect the coaxial cable to be tested to the SIGNAL OUT jack using the adaptor GR874B-TO-OSM J. Observe the oscilloscope to determine if the coaxial cable being tested meets the 1.1 VSWR criteria.

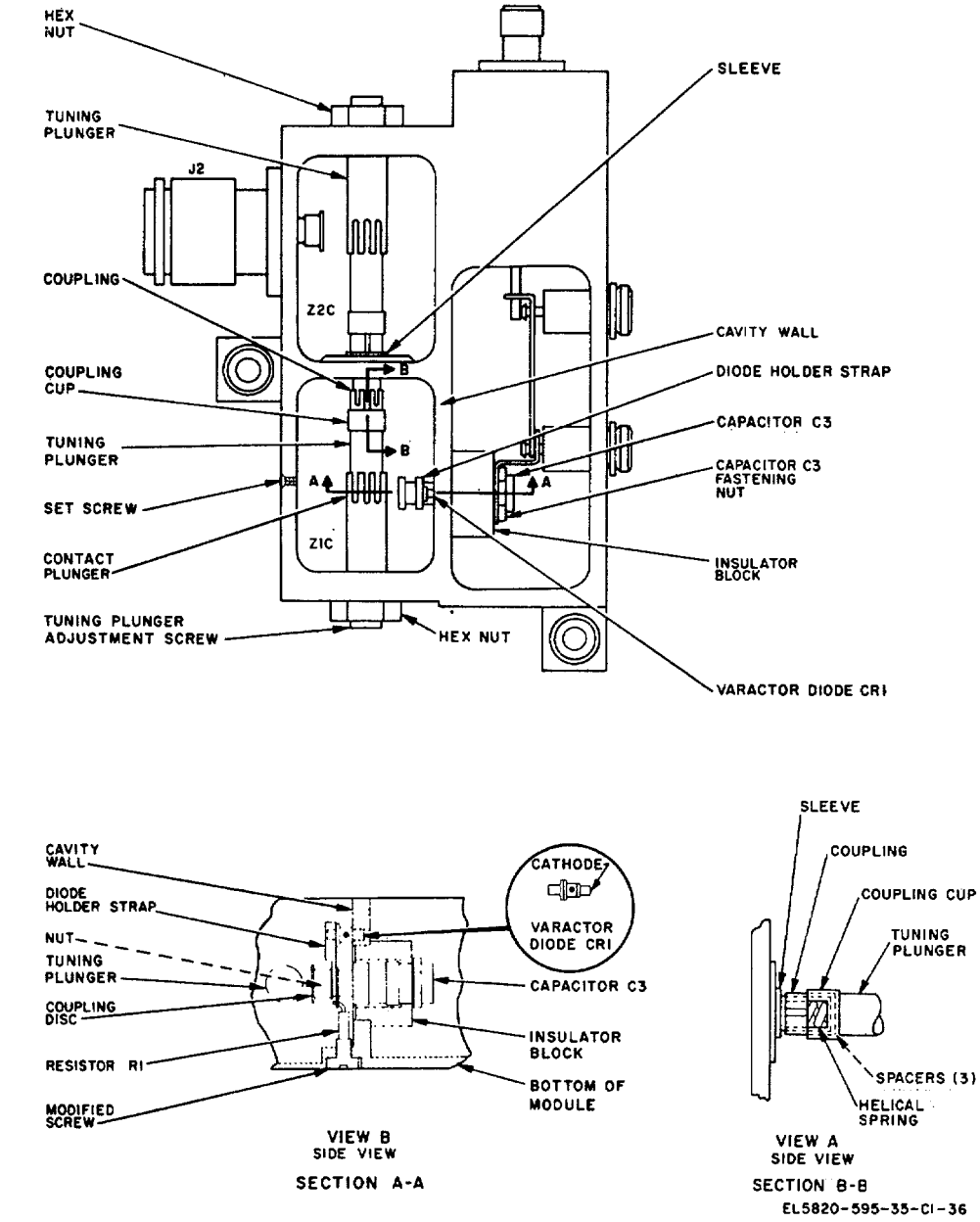


Figure 7-1. 2nd frequency multiplier 1A10A1, varactor diode 1A10A1CR1 replacement.

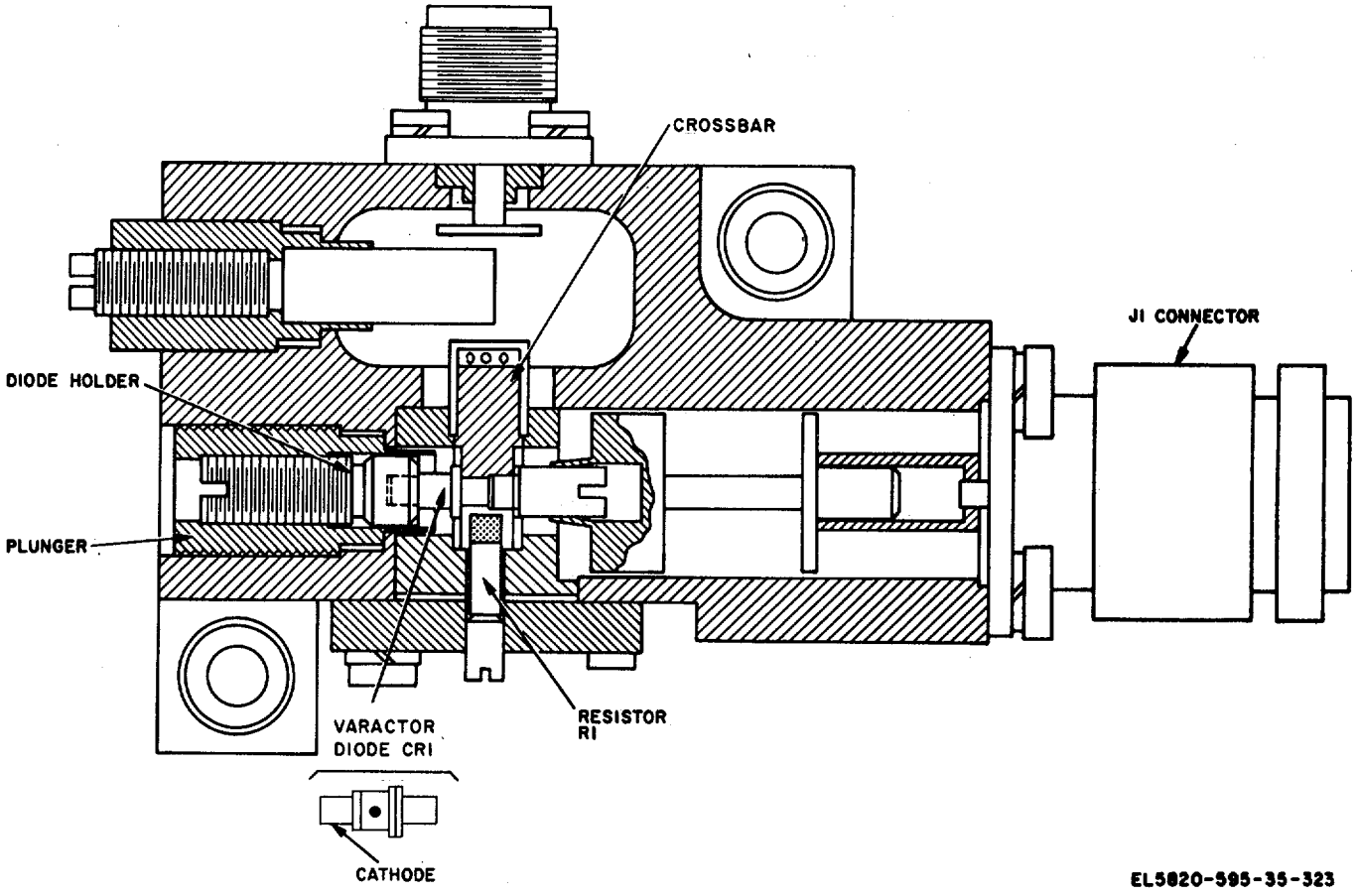


Figure 7-2. 3rd frequency multiplier 1A10A2, varactor diode 1A10A2CR1 replacement.

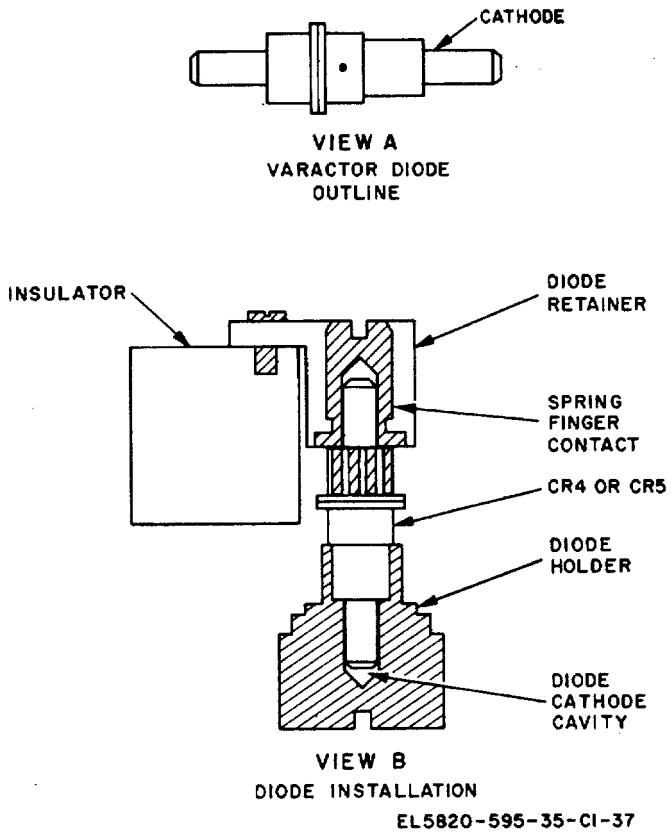


Figure 7-3. Amplifier-frequency multiplier 1A11, varactor diode 1A11CR4 or 1A11CR5 replacement.

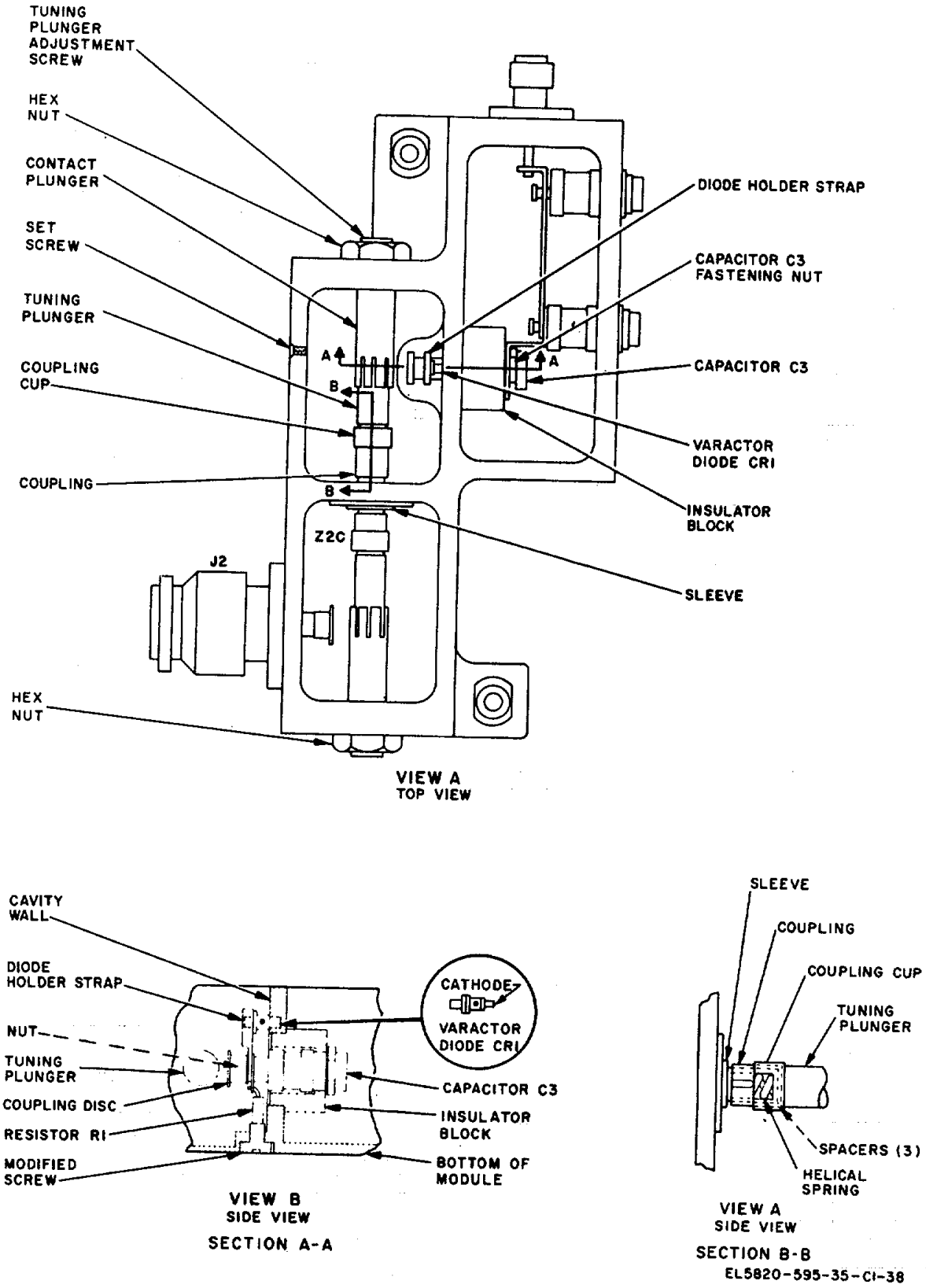
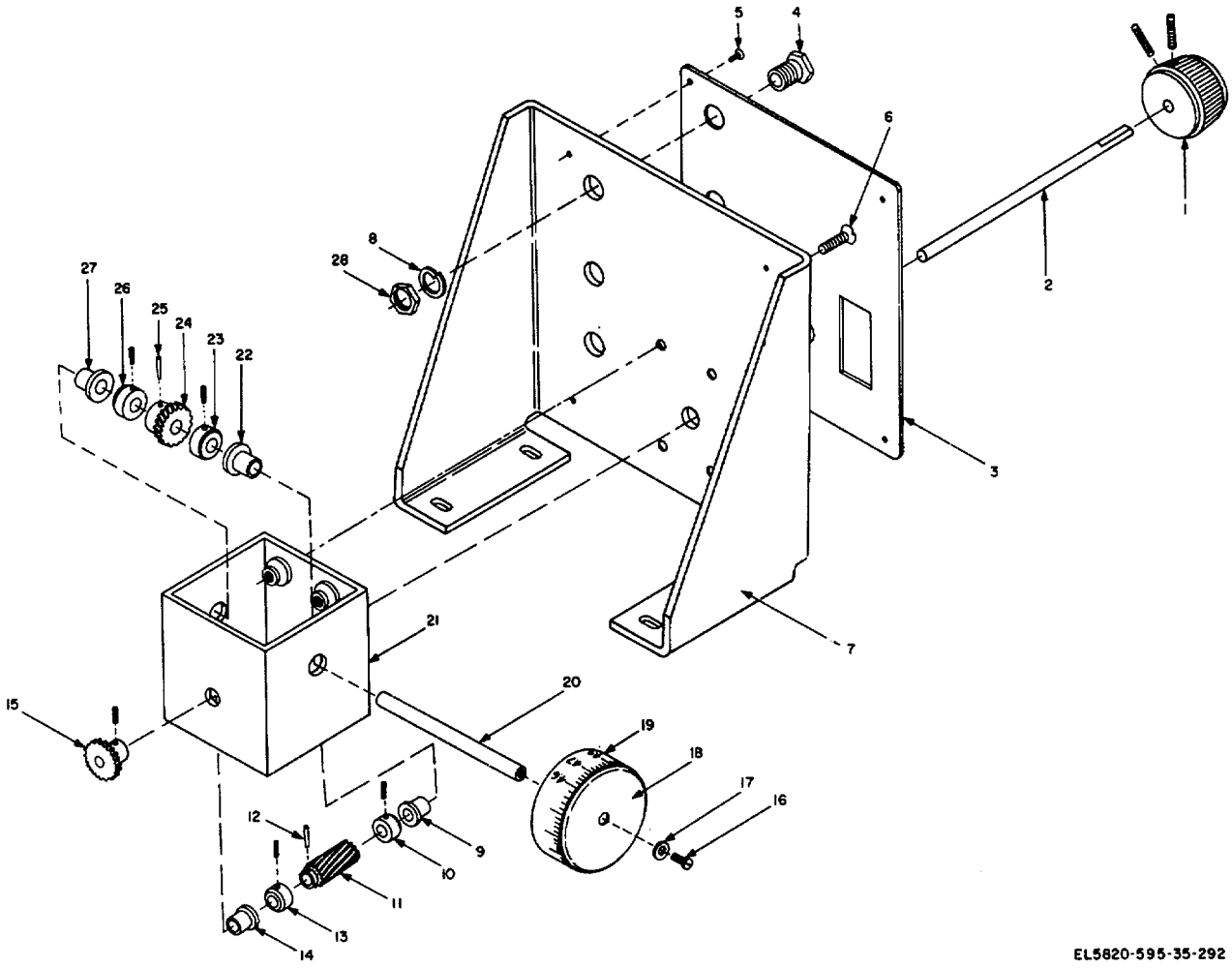


Figure 7-4. 2nd frequency multiplier 2A7A1, varactor diode 2A7A1CR1 replacement.



1 Control knob 3A9A6MP14
2 Main tuning shaft 3A9A6MP16
3 Front panel 3A9A6MP15
4 Chassis bushings 3A9A6MP6 through 3A9A6MP8
5 Machine screws 3A9A6H1 through 3A9A6H4
6 Machine screws 3A9A6A2H1 through 3A9A6A2H4
7 Tuner bracket 3A9A6MP5
8 Lock washers 3A9A6MP18 through 3A9A6MP20
9 Bearing 3A9A6MP1
10 Collar 3A9A6MP11
11 Worm 3A9A6MP21
12 Spring 3A9A6H5
13 Collar 3A9A6MP12
14 Bearing 3A9A6MP2
15 Miniature sprocket 3A9A6MP17
16 Machine screw 3A9A6A1H1
17 Flat washer 3A9A6H1H2
18 Drum 3A9A6A1
19 Drum dial 3A9A6MP13
20 Gear shaft 3A9A6A1MP2
21 Gear housing 3A9A6A2MP1
22 Bearing 3A9A6MP3
23 Collar 3A9A6MP11
24 Worm gear 3A9A6MP22
25 Spring pin 3A9A6H6
26 Collar 3A9A6MP12
27 Bearing 3A9A6MP6
28 Lock nut

Figure 7-5. Frequency tuner 3A9A6, exploded view.

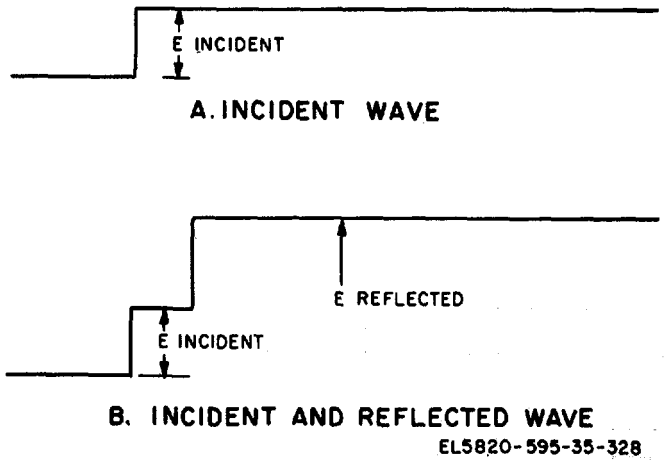


Figure 7-6. Reflectometer test wave forms.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, *PREFIX WITH UNIT NUMBER AND SUB-*ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT BUS WIRE WHICH IS NO.22 SOLID.

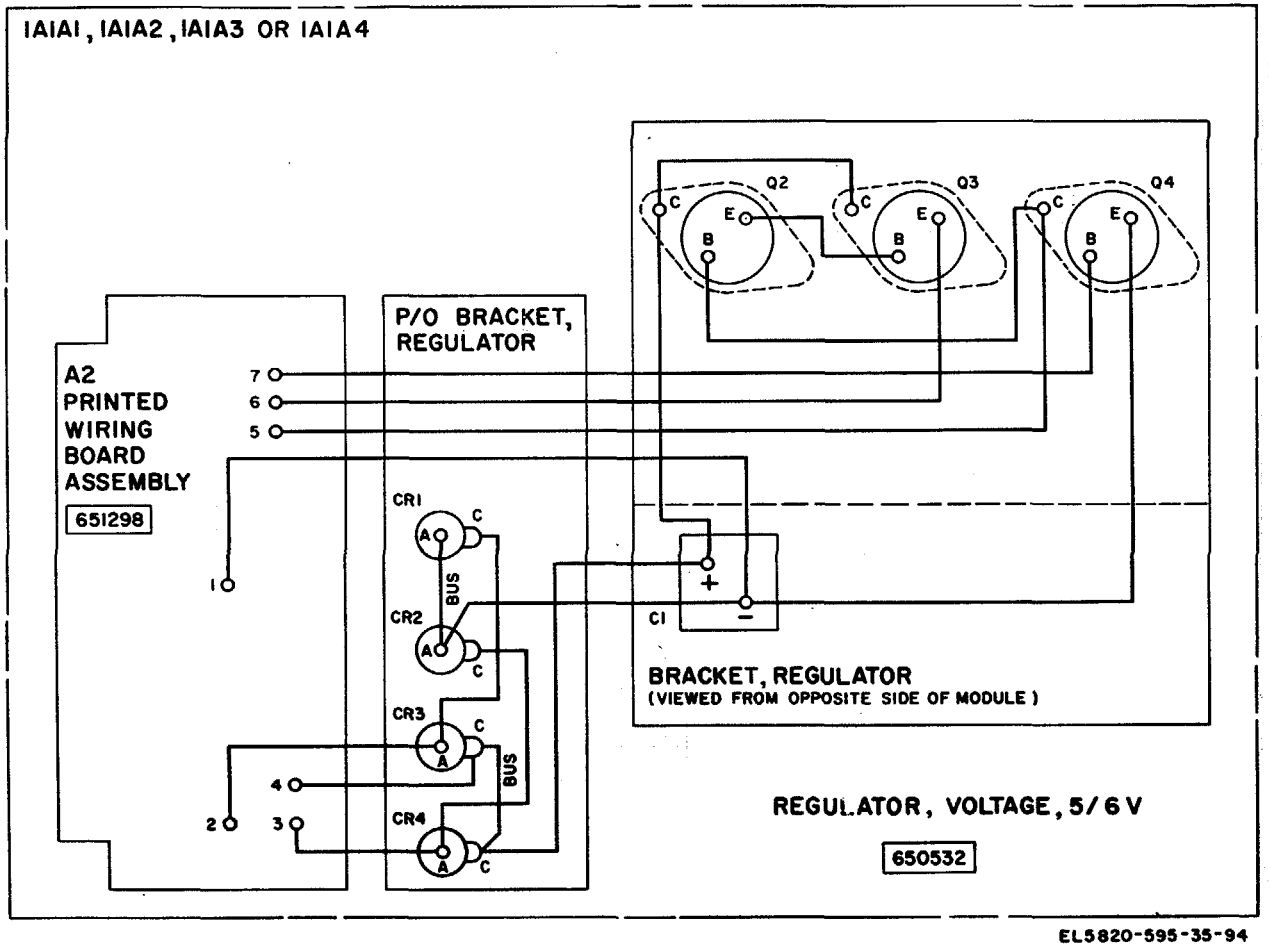
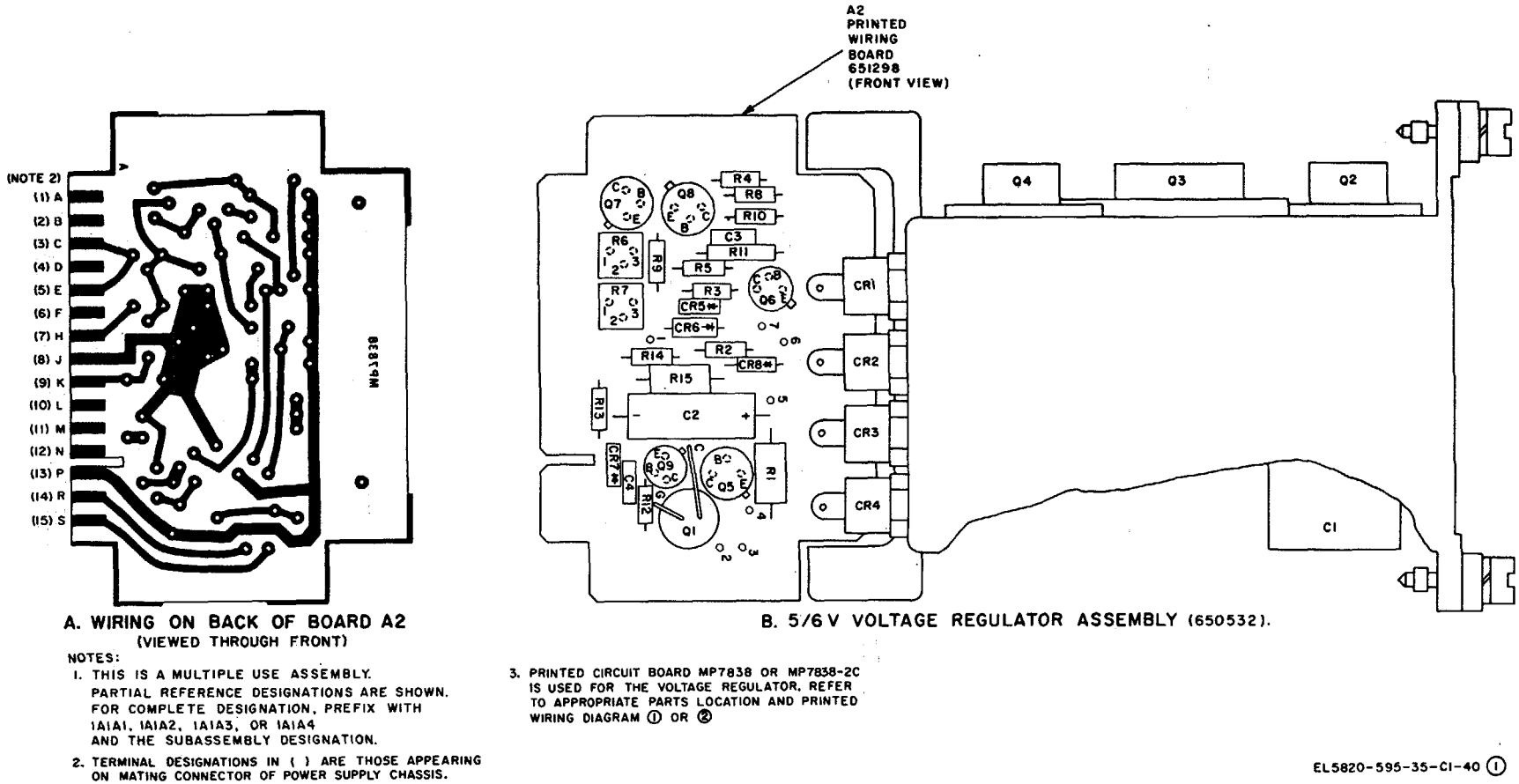


Figure 7-7. 5/6v regulator 1A1A1 through 1A1A4, bracket wiring diagram.



A. WIRING ON BACK OF BOARD A2
(VIEWED THROUGH FRONT)

B. 5/6 V VOLTAGE REGULATOR ASSEMBLY (650532).

NOTES:
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A1, 1A1A2, 1A1A3, OR 1A1A4 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②

EL5820-595-35-CI-40 ①

Figure 7-8 (1). 5/6v regulator 1A1A1 through 1A1A4, parts location and printed wiring diagram.

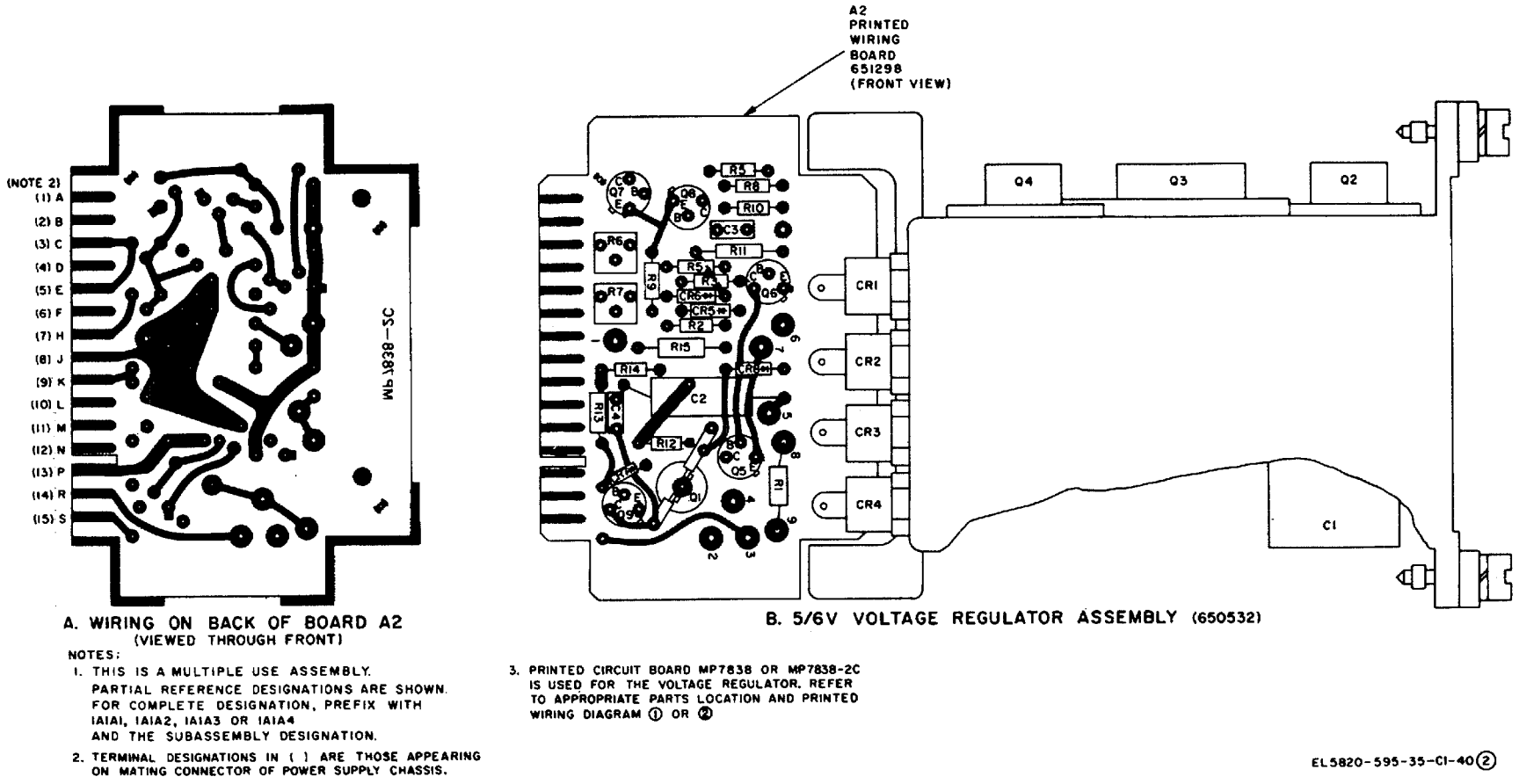


Figure 7-8 (2). 5/6v regulator 1A1A1 through 1A1A4, parts location and printed wiring diagram.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT BUS WIRE WHICH IS NO. 22 SOLID.

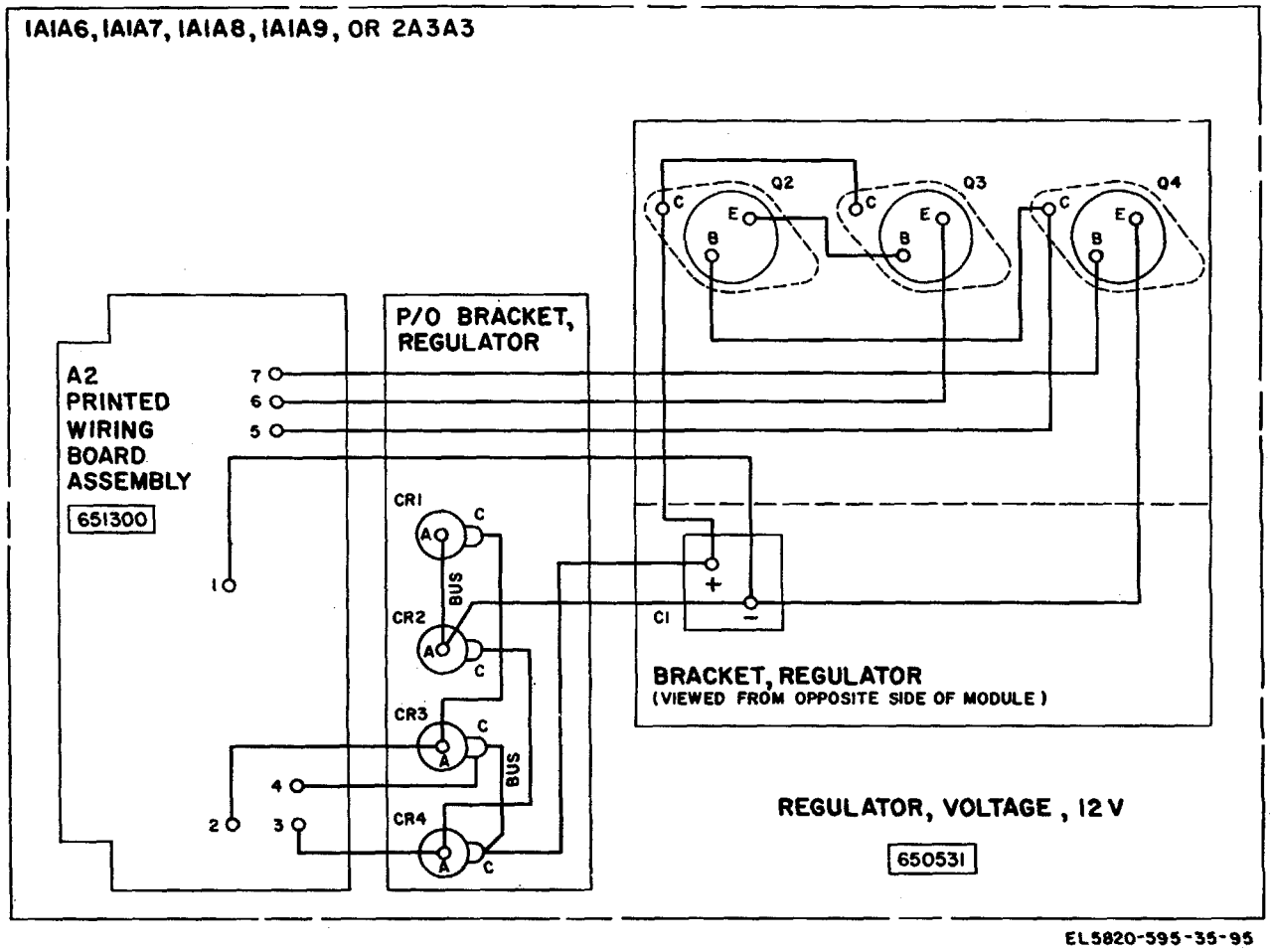
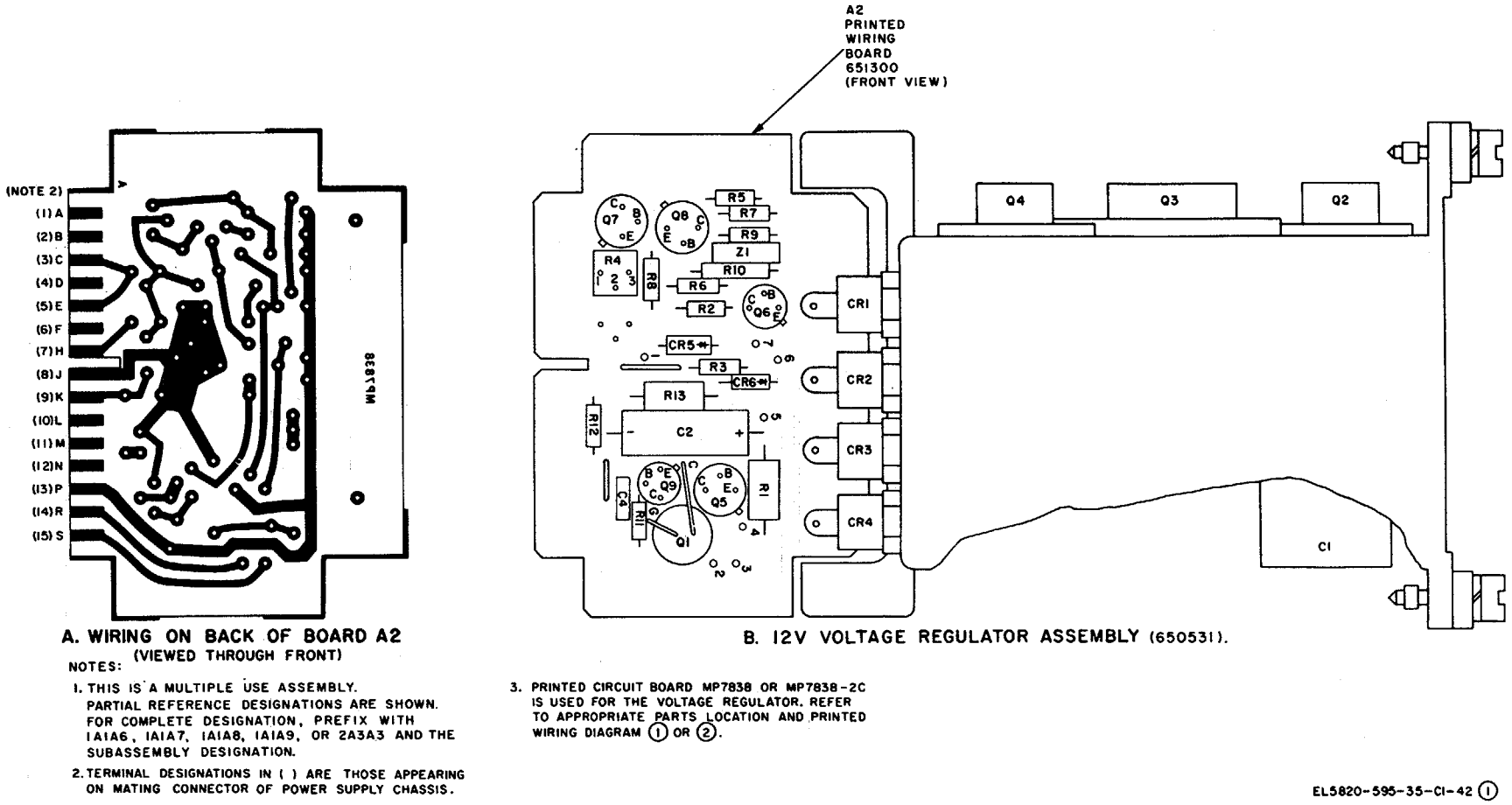


Figure 7-9. 12v regulator 1A1A6 through 1A1A9 and 2A3A3, bracket wiring diagram.



A. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT)

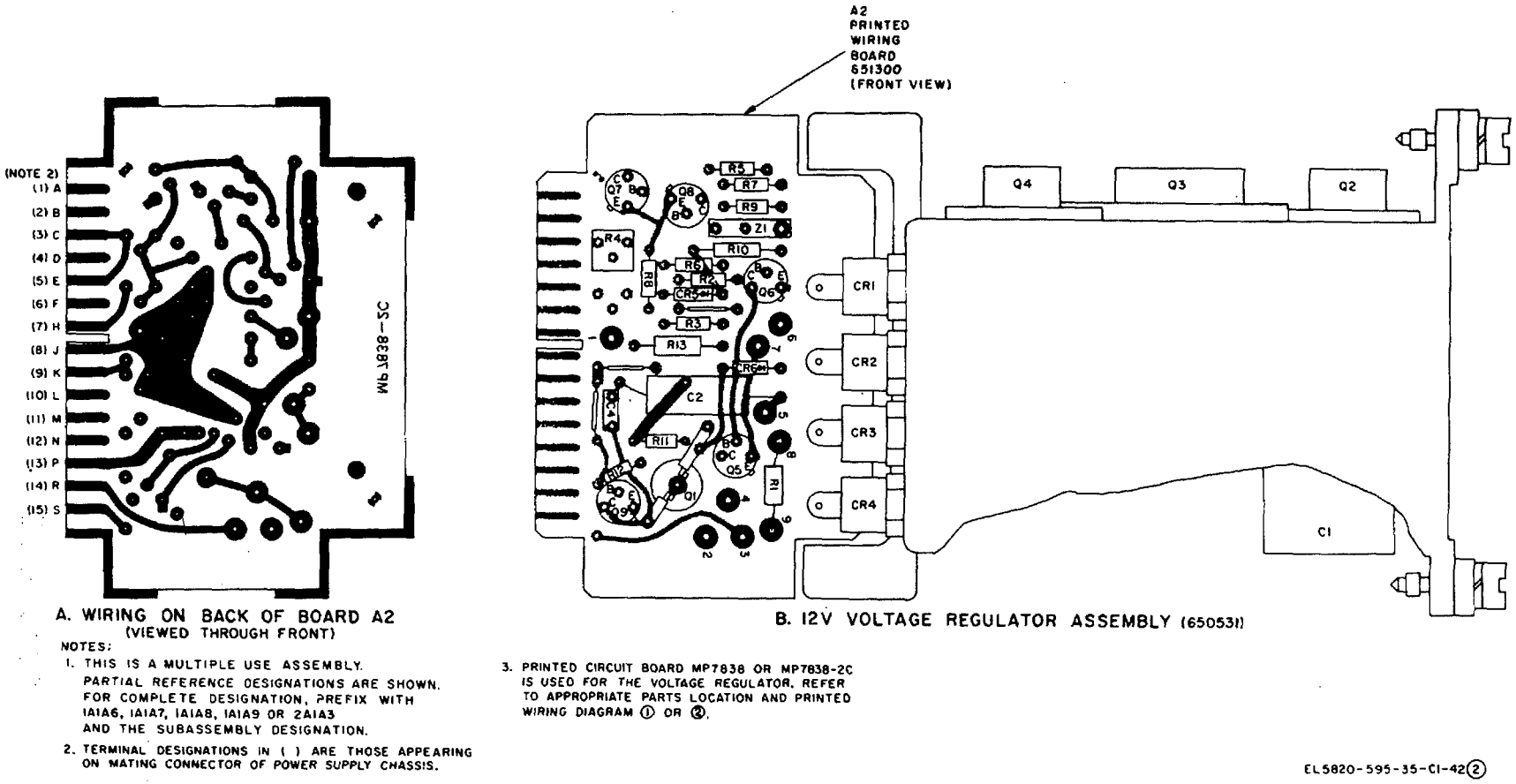
B. 12V VOLTAGE REGULATOR ASSEMBLY (650531).

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A6, 1A1A7, 1A1A8, 1A1A9, OR 2A3A3 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM (1) OR (2).

EL5820-595-35-CI-42 (1)

Figure 7-10 (1). 12v regulator 1A1A6 through 1A1A9 and 2A3A3, parts location and printed wiring diagram.



NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A6, 1A1A7, 1A1A8, 1A1A9 OR 2A1A3 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
3. PRINTED CIRCUIT BOARD MP7838 OR MP7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM ① OR ②.

Figure 7-10 (2). 12v regulator 1A1A6 through 1A1A9 and 2A3A3, parts location and printed wiring diagram.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED, EXCEPT BUS WIRE WHICH IS NO.22 SOLID.

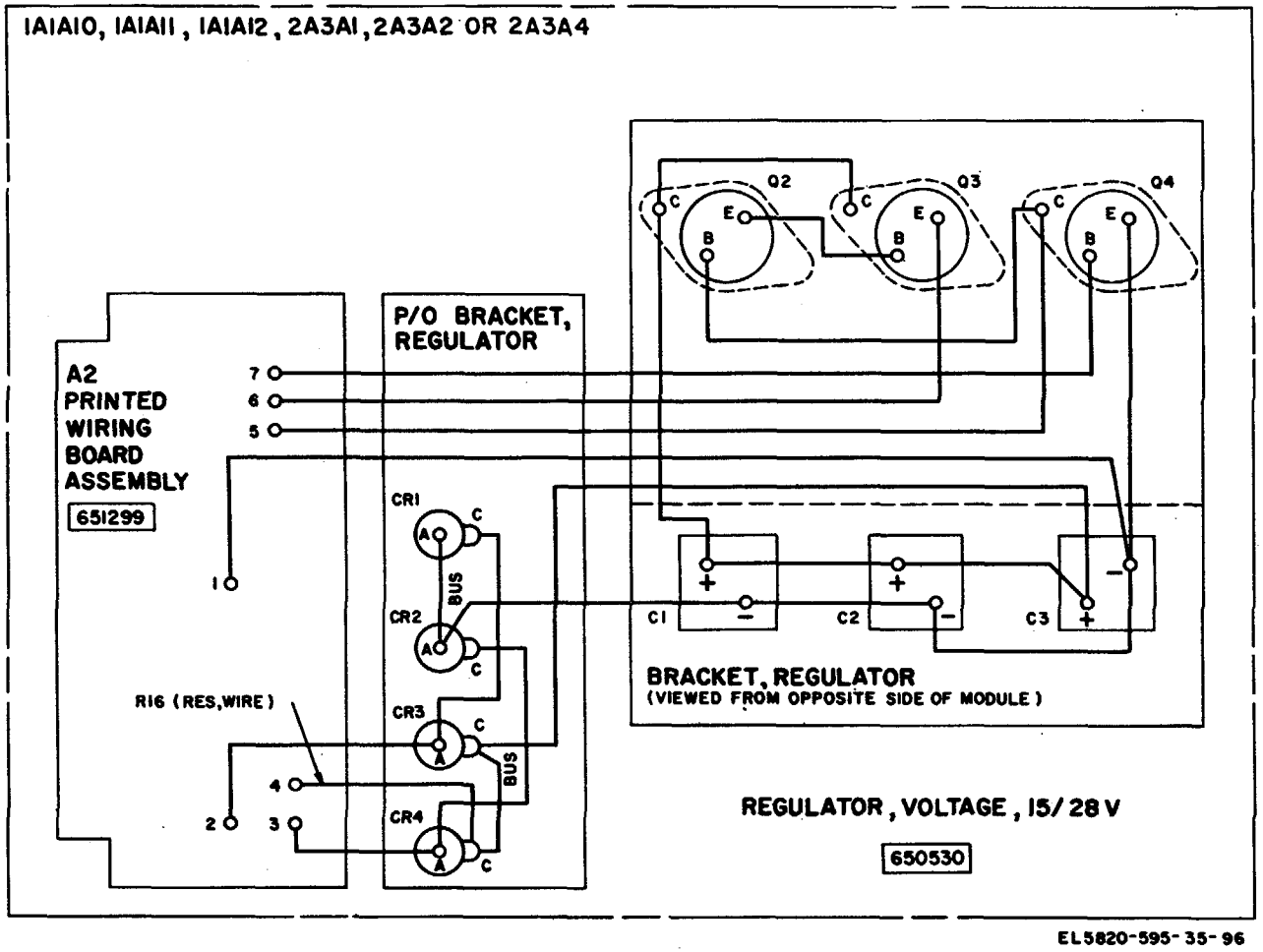
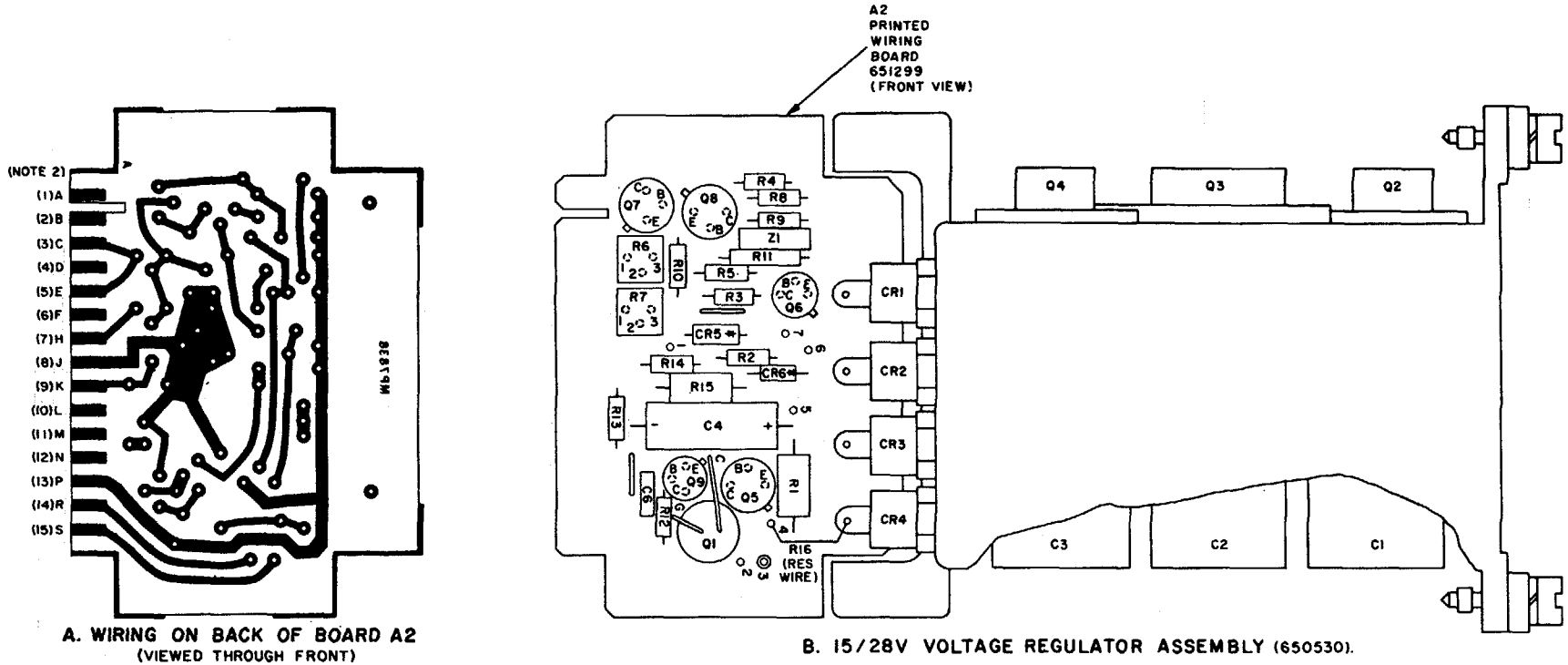


Figure 7-11. 15/28v regulator 1A1A10 through 1A1A12, 2A3A2, and 2A3A4, bracket wiring diagram.



A. WIRING ON BACK OF BOARD A2
(VIEWED THROUGH FRONT)

B. 15/28V VOLTAGE REGULATOR ASSEMBLY (650530).

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1A10, 1A1A11, 1A1A12, 2A3A1, 2A3A2 OR 2A3A4 AND THE SUBASSEMBLY DESIGNATION.
2. TERMINAL DESIGNATIONS IN ( ) ARE THOSE APPEARING ON MATING CONNECTOR OF POWER SUPPLY CHASSIS.
3. PRINTED CIRCUIT BOARD MP7838 OR 7838-2C IS USED FOR THE VOLTAGE REGULATOR. REFER TO APPROPRIATE PARTS LOCATION AND PRINTED WIRING DIAGRAM (1) OR (2).

EL5820-595-35-CI-44 (1)

Figure 7-12 (1). 15/28v regulator 1A1A10 through 1A1A12, 2A3A1, 2A3A2, and 2A3A1, parts location and printed wiring diagram.

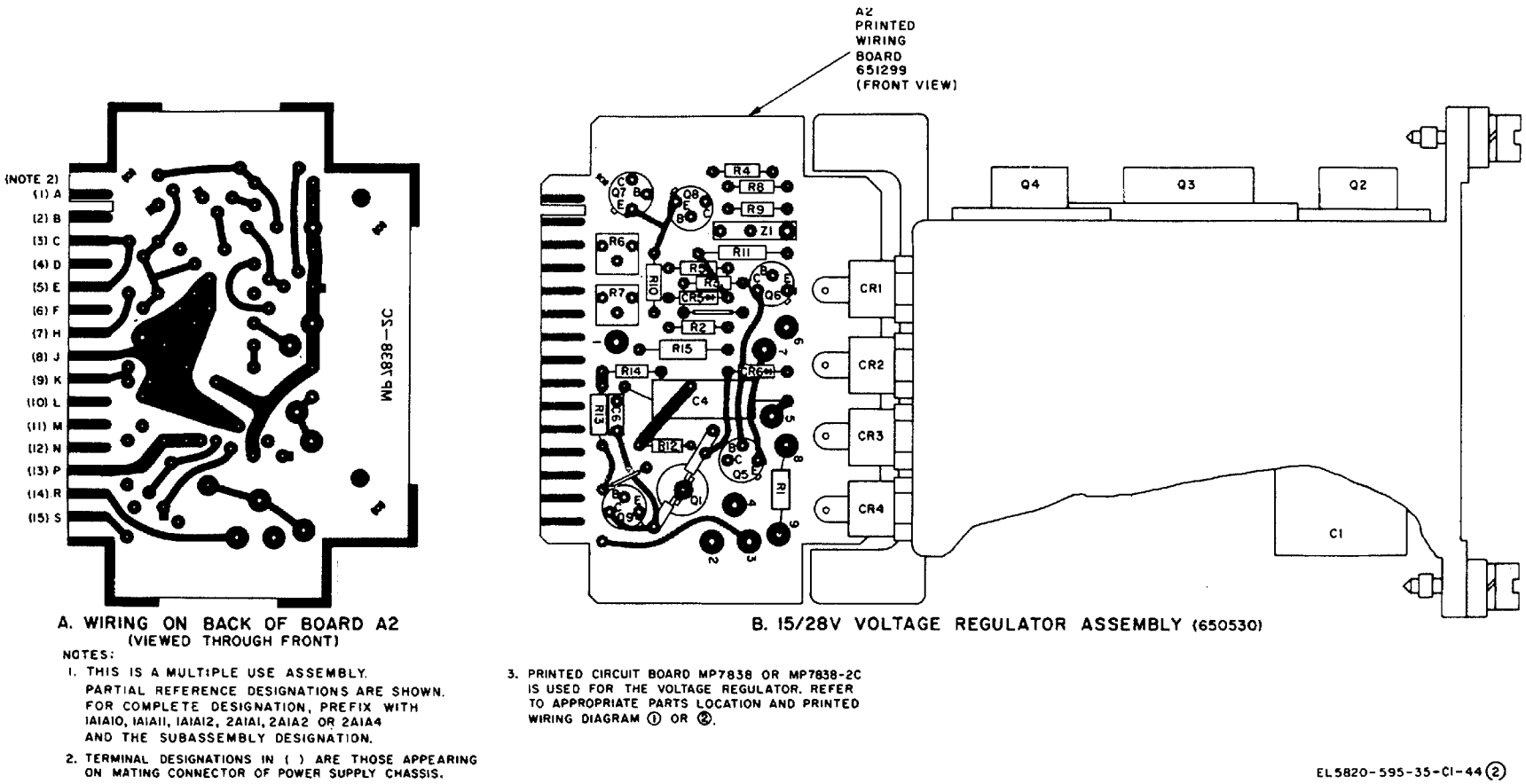


Figure 7-12 (2). 15/28v regulator 1A1A10 through 1A1A12, 2A3A1, 2A3A2, and 2A3A4, parts location and printed wiring diagram

NOTES:

1. THIS DIAGRAM IS USED FOR ATTENUATOR ASSEMBLIES 650514 (12 CHANNEL) AND 650536 (24 CHANNEL).
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
3. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED; EXCEPT CABLE W1.

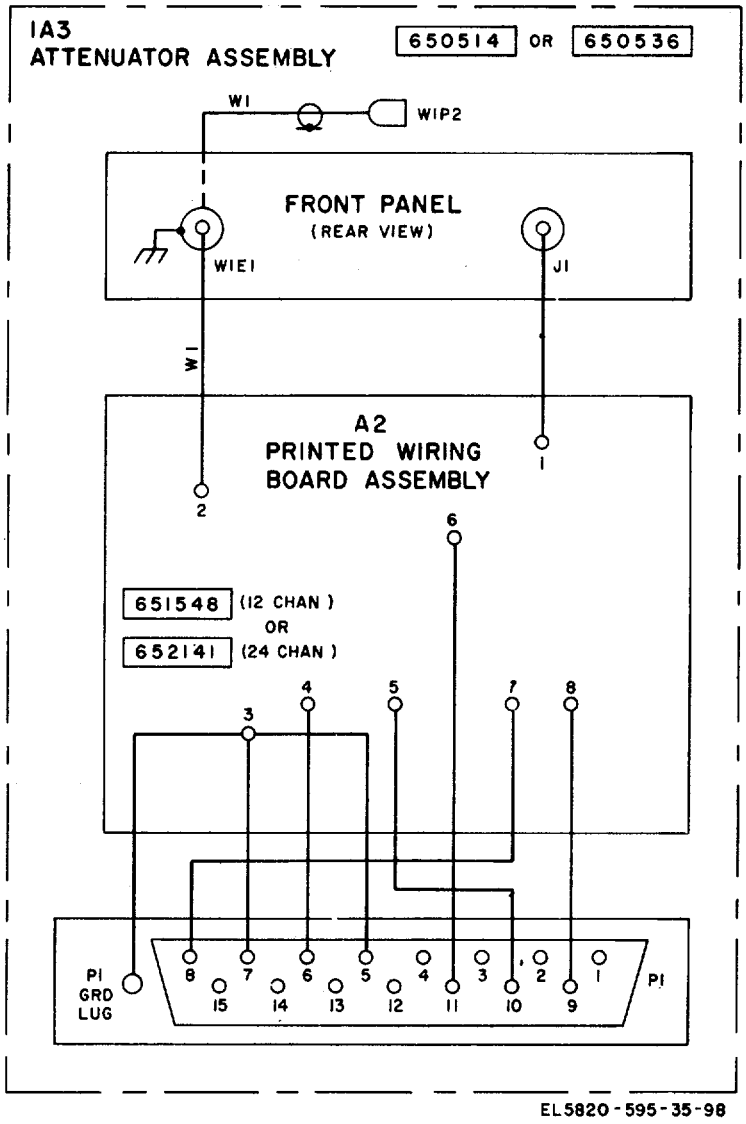
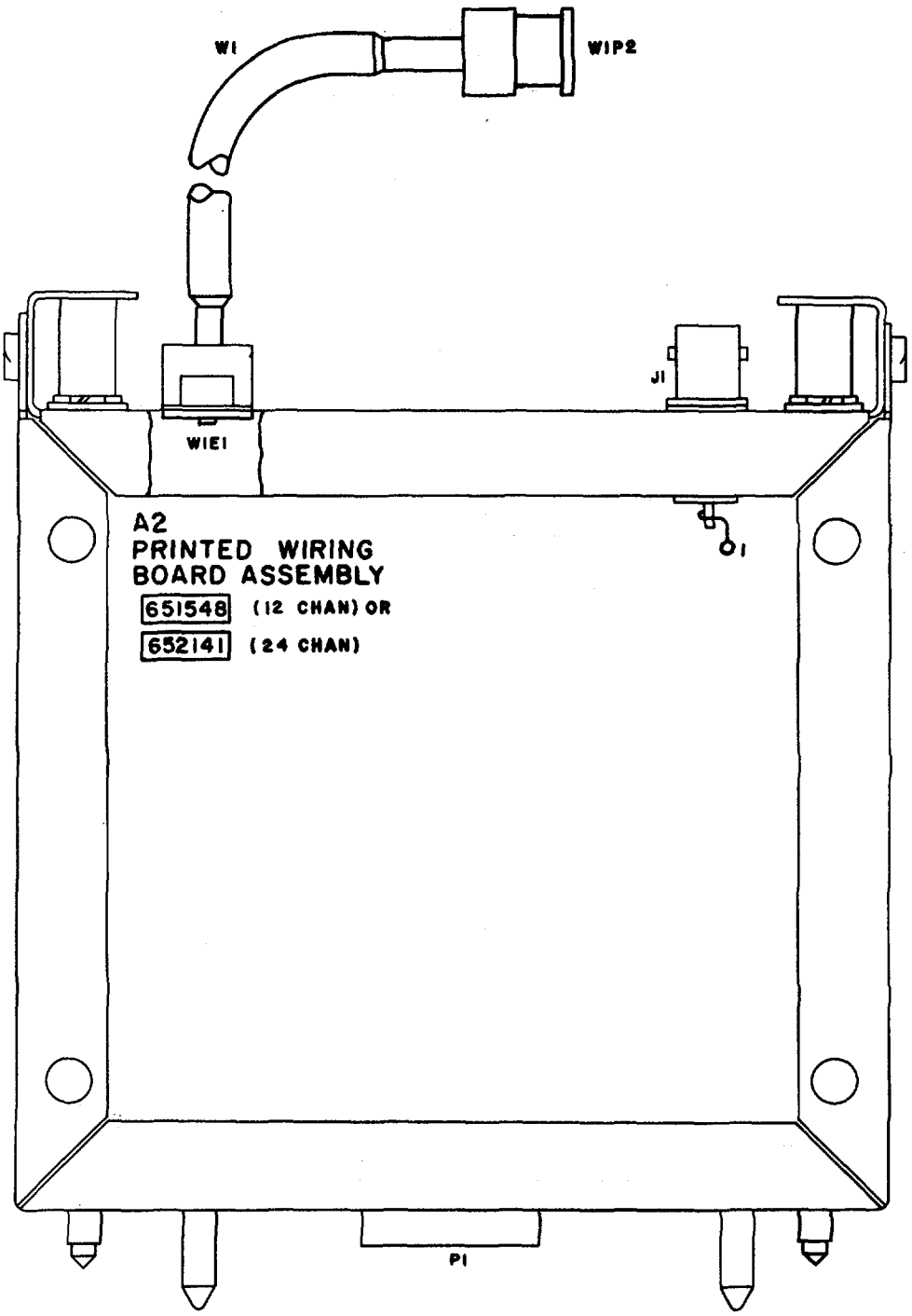


Figure 7-13. Pom attenuator (12 or 24 channel) 1A3 assembly, wiring diagram.

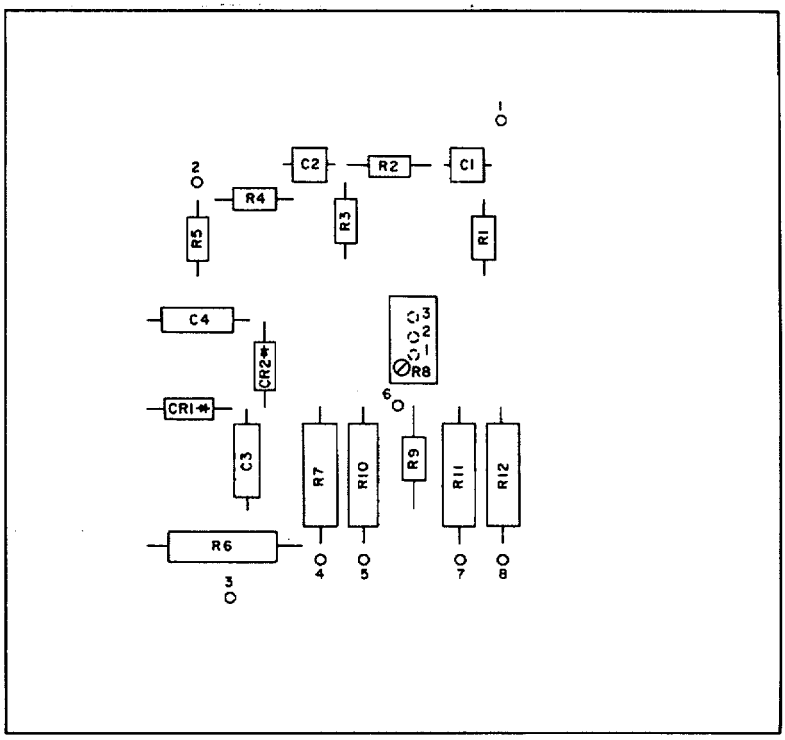


NOTES:

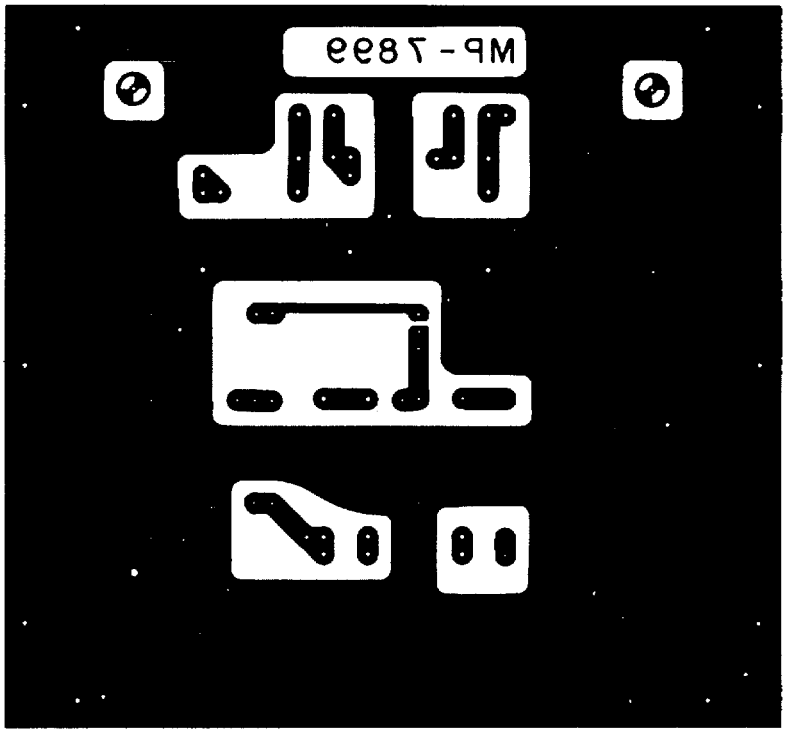
1. THIS DIAGRAM IS USED FOR ATTENUATOR ASSEMBLIES 650514 AND 650536. ATTENUATOR ASSEMBLY 650514 IS USED FOR 12 CHANNEL OPERATION. ATTENUATOR ASSEMBLY 650536 IS USED FOR 24 CHANNEL OPERATION.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A3

EL5820-595-35-172(1)

Figure 7-14 (1). Pom attenuator (12 or 24 channel) 1A3, parts location and printed wiring diagram (part 1 of 2).



A. PARTS ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

EL5820-595-35-172 (2)

Figure 7-14 (2). Pom attenuator (12 or 24 channel) 1A3, parts location and printed wiring diagram (part 2 of 2).

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

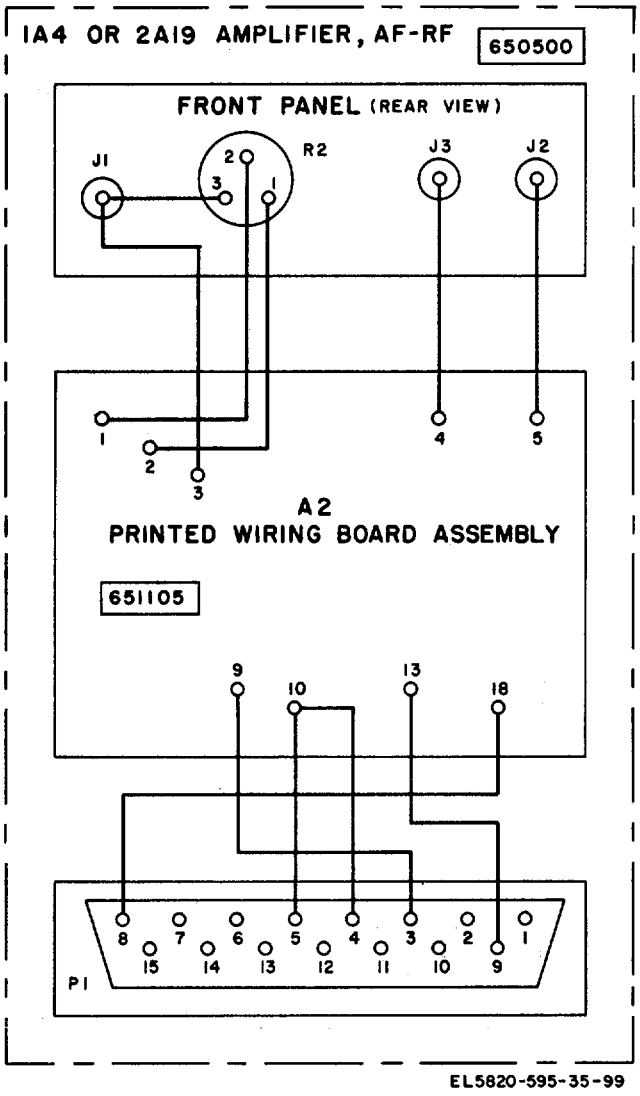


Figure 7-15. AF-RF amplifier 1A4/2A19 assembly, wiring diagram.

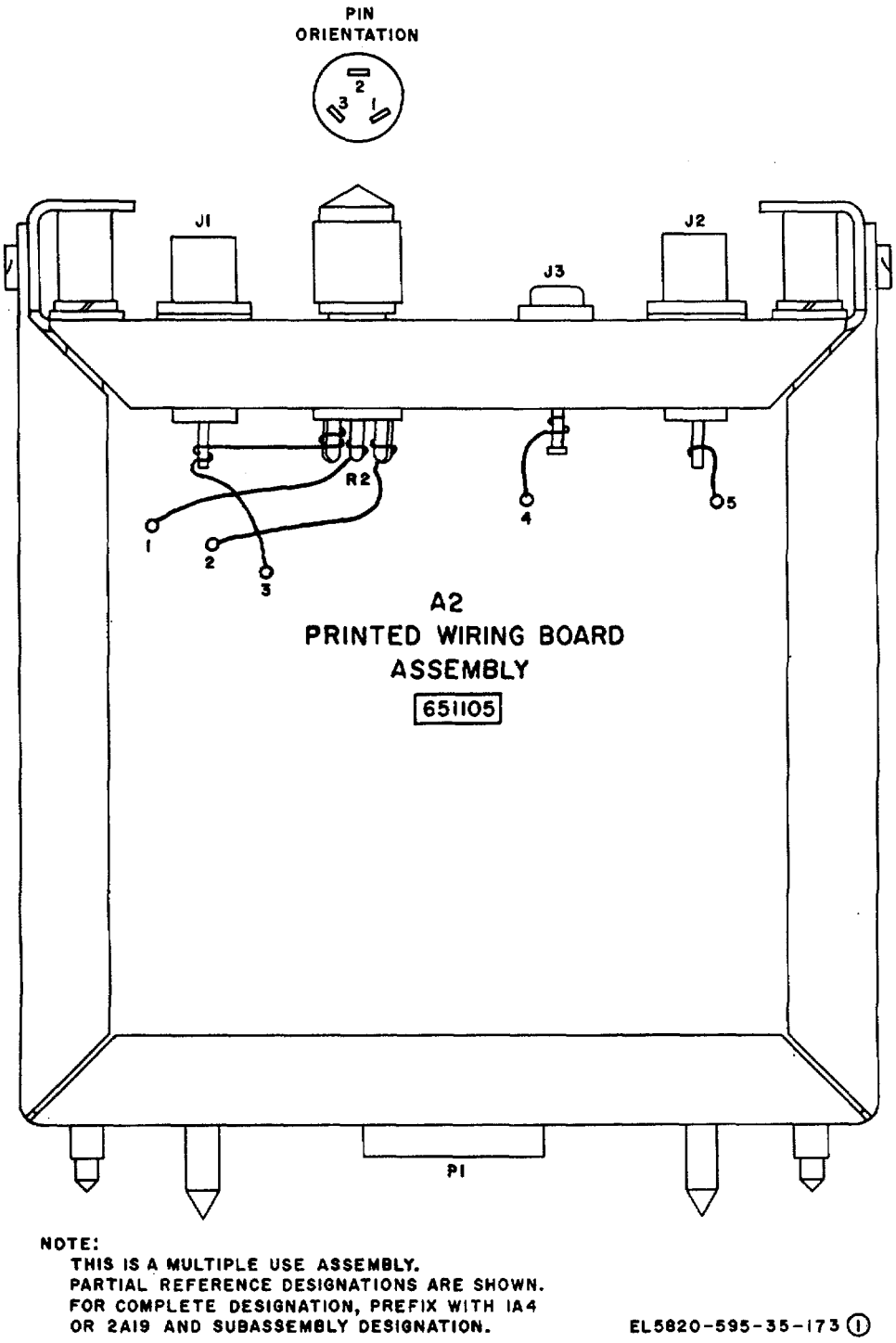
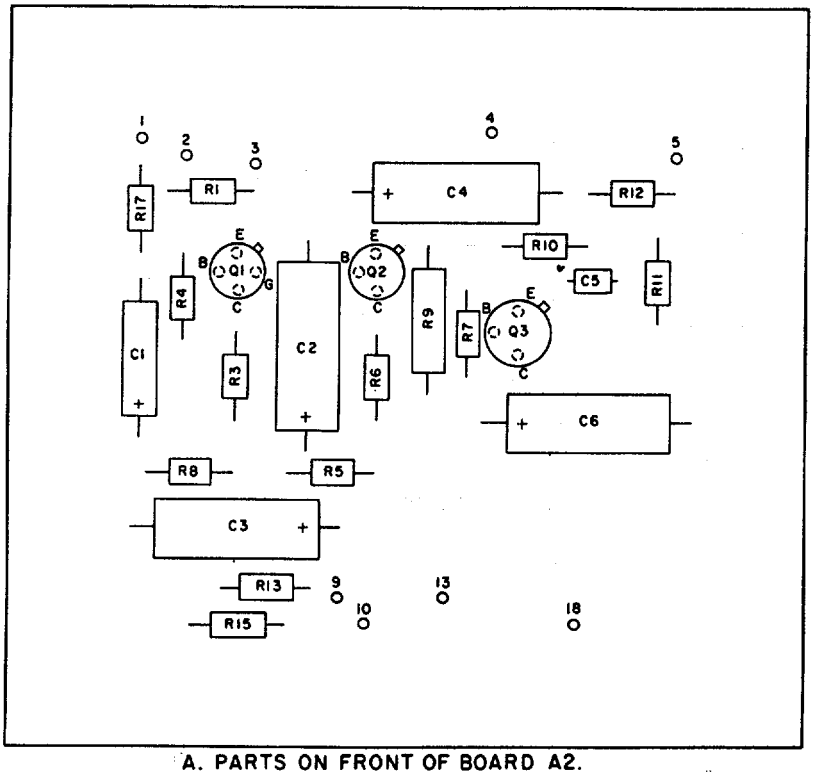
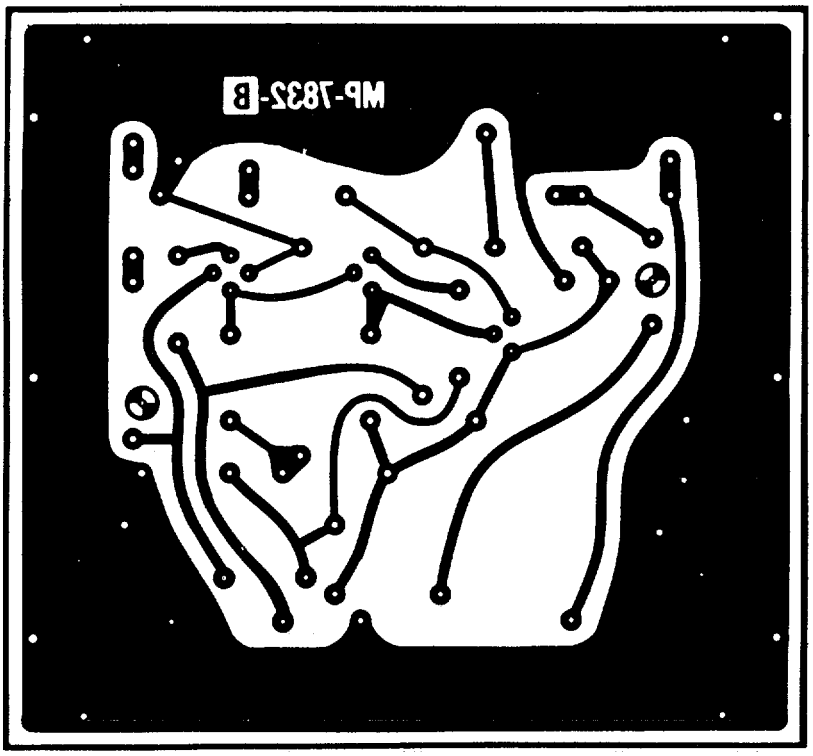


Figure 7-16 (1). AF-RF amplifier 1A4/2A19, parts location and printed wiring diagram (part 1 of 2).



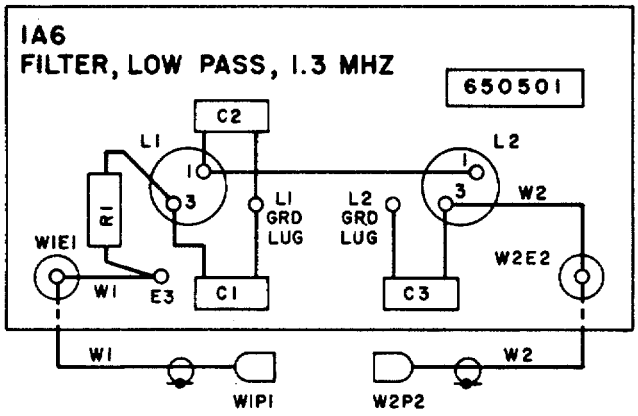
A. PARTS ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

EL5820-595-35-173 (2)

Figure 7-16 (2). AF-RF amplifier 1A4/2A19, parts location and printed wiring diagram (part 2 of 2).



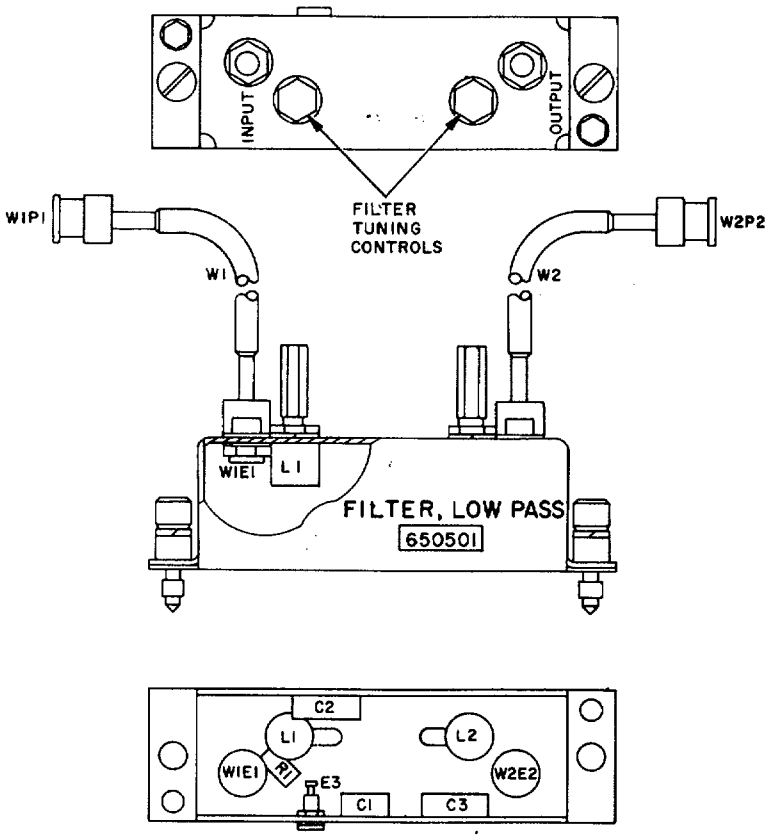
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A6.

2. WIRING IS NO. 22 AWG STRANDED WIRE, TEFLON INSULATED, EXCEPT CABLES W1 & W2.

EL5820-595-35-C1-45

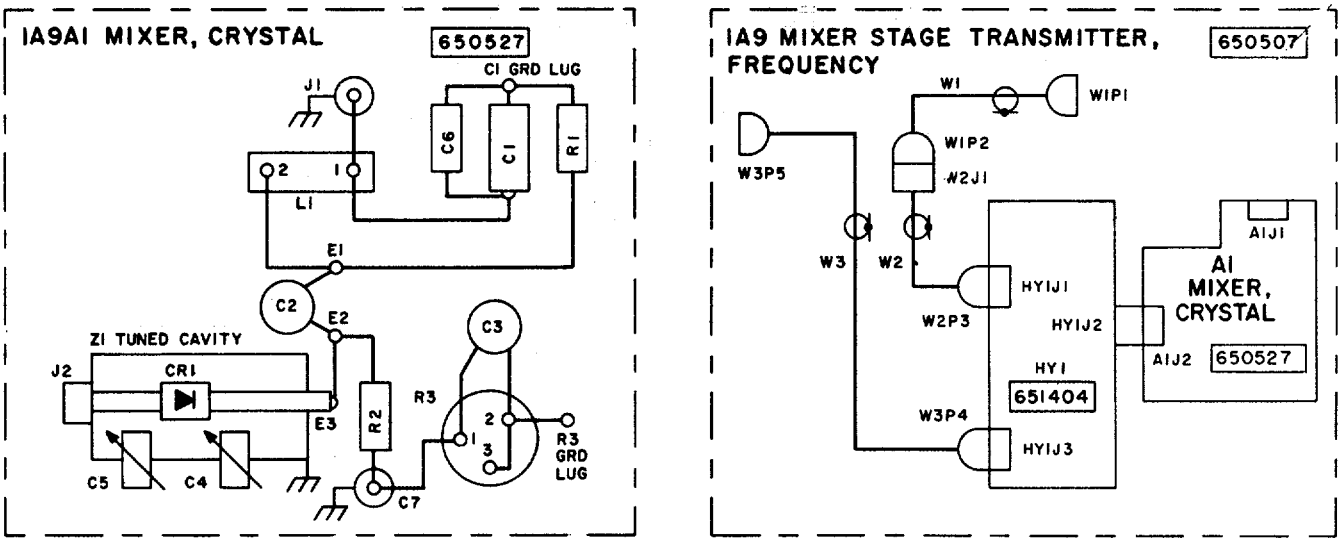
Figure 7-17. 1.3 MHz low pass filter 1A6 assembly, wiring diagram.



NOTE :
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A6.

EL5820-595-35-175

Figure 7-18. 1.3 MHz low pass filter 1A6, parts location diagram.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 SOLID, TINNED COPPER.

EL5820-595-35-104

Figure 7-19. Frequency mixer 1A9 assembly, wiring diagram.

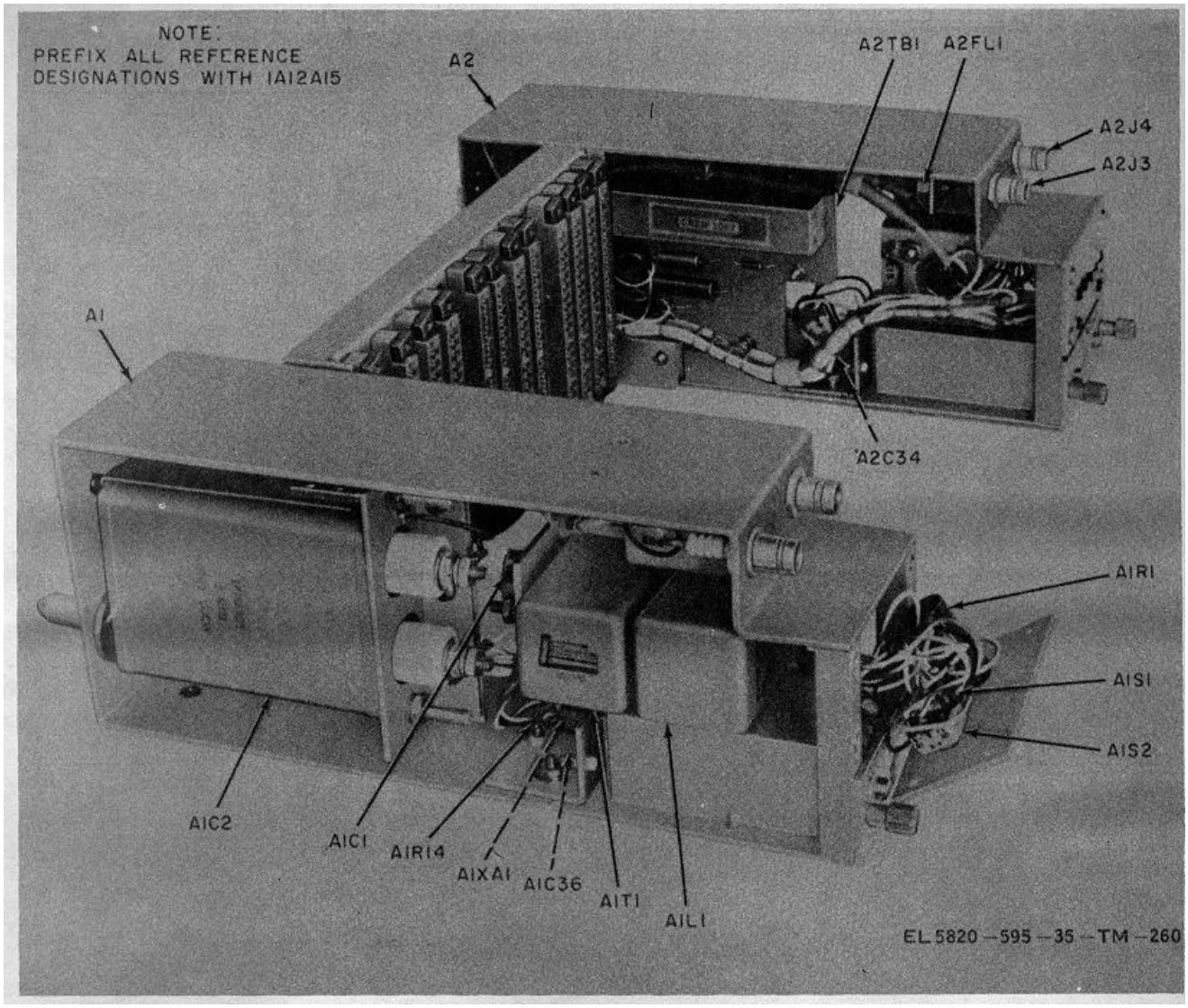


Figure 7-20. Digital data modem chassis 1A12A15, left oblique view, parts location.

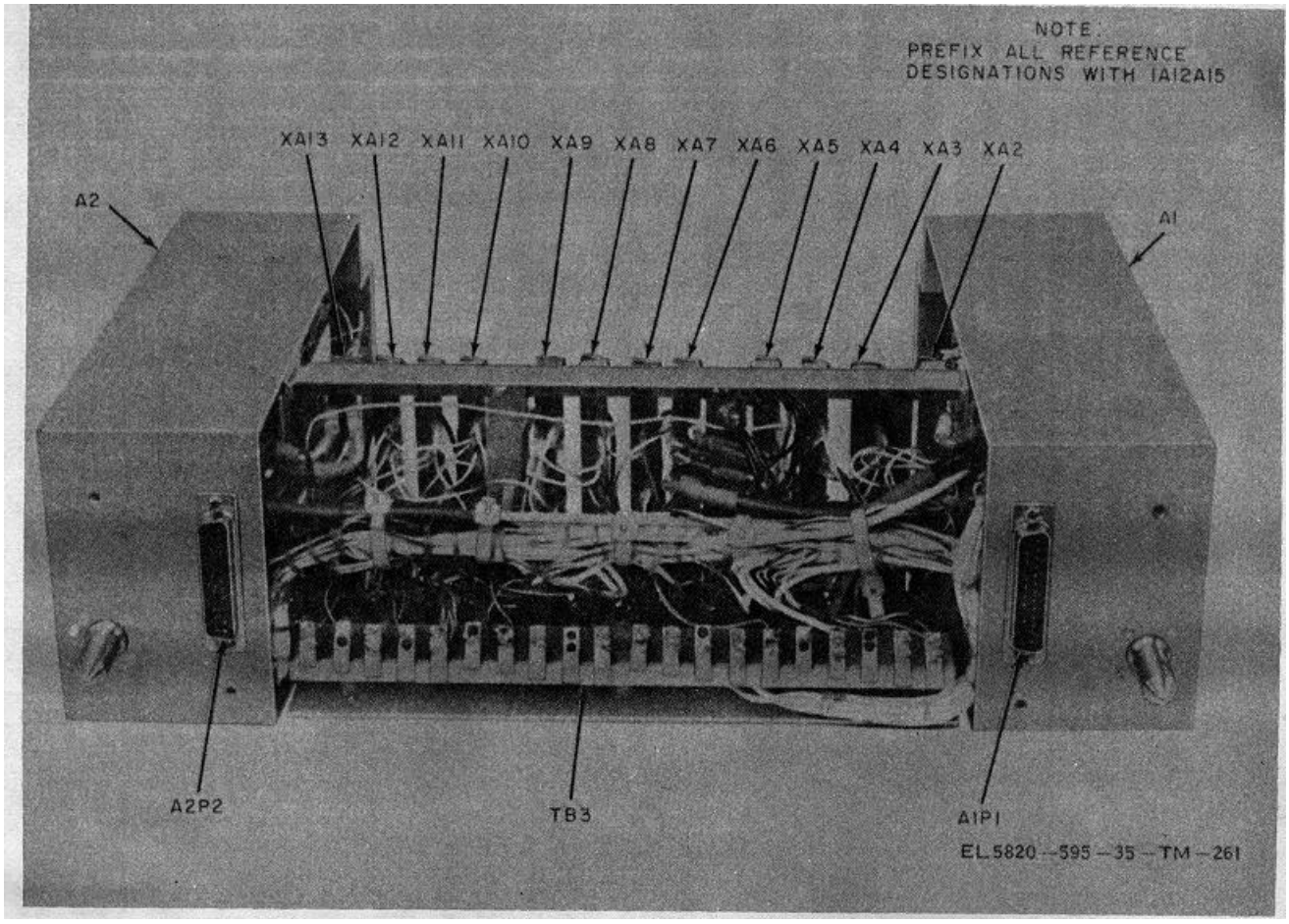


Figure 7-21. Digital data modem chassis 1A12A15, rear view, parts location.

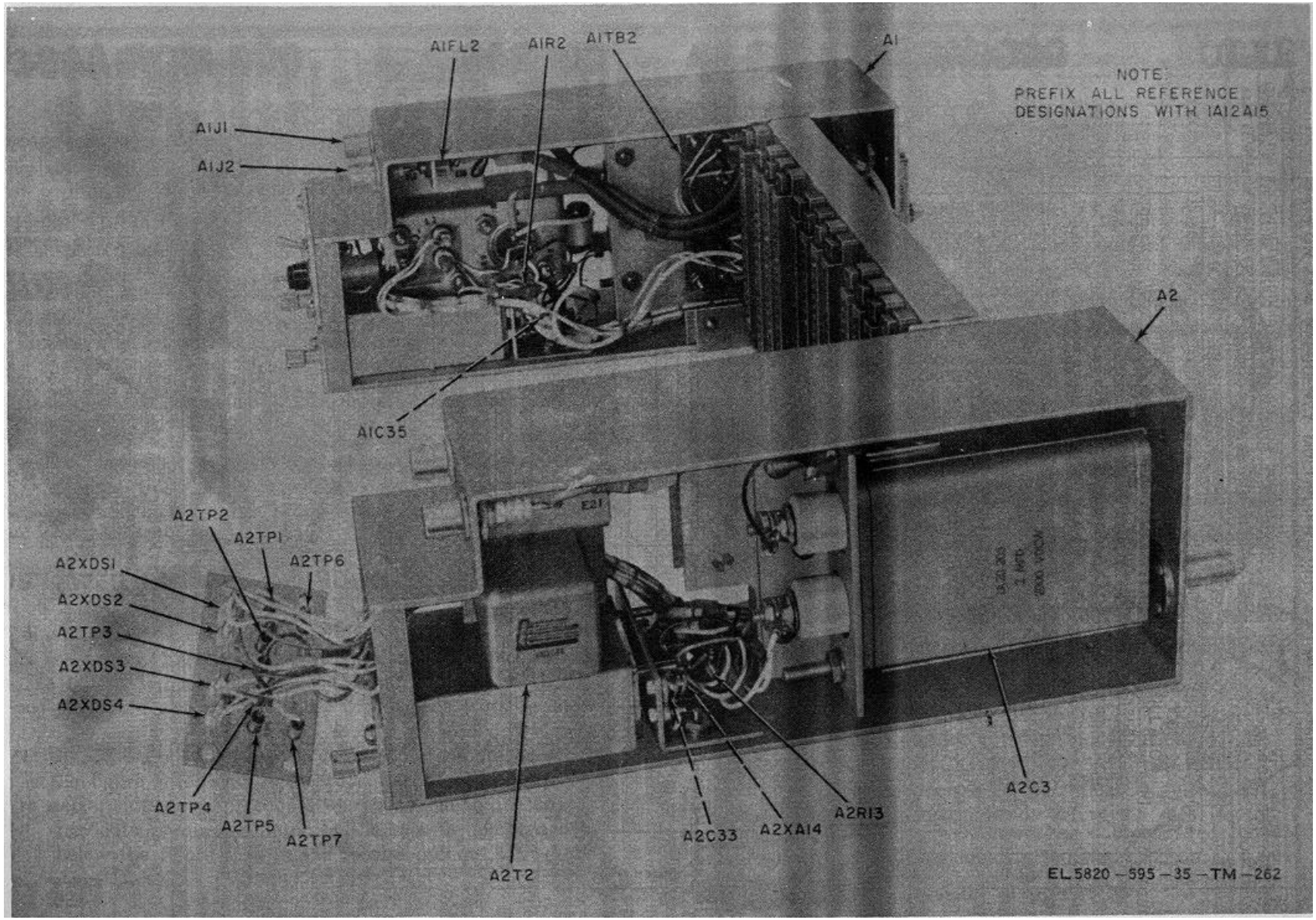
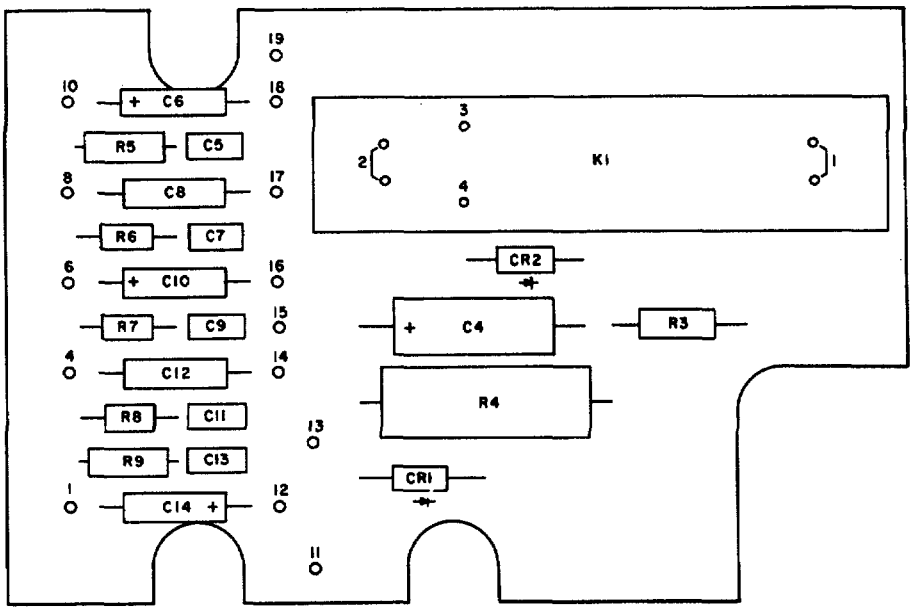
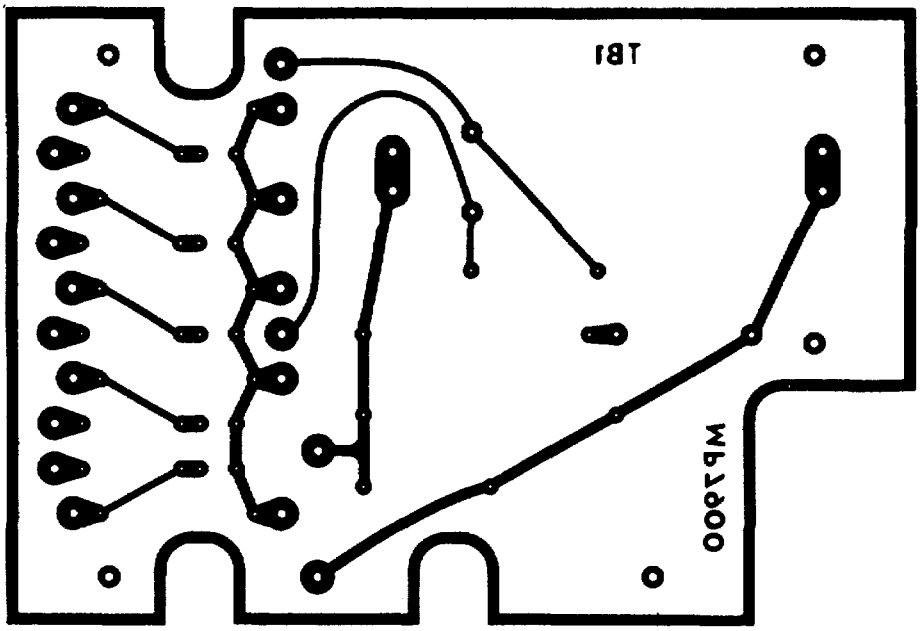


Figure 7-22. Digital data modem chassis 1A12A15, right oblique view, parts location.



A. PARTS ON FRONT OF BOARD TB1 (651726).



B. WIRING ON BACK OF BOARD TB1 (VIEWED THROUGH FRONT).

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A15A2TB1.

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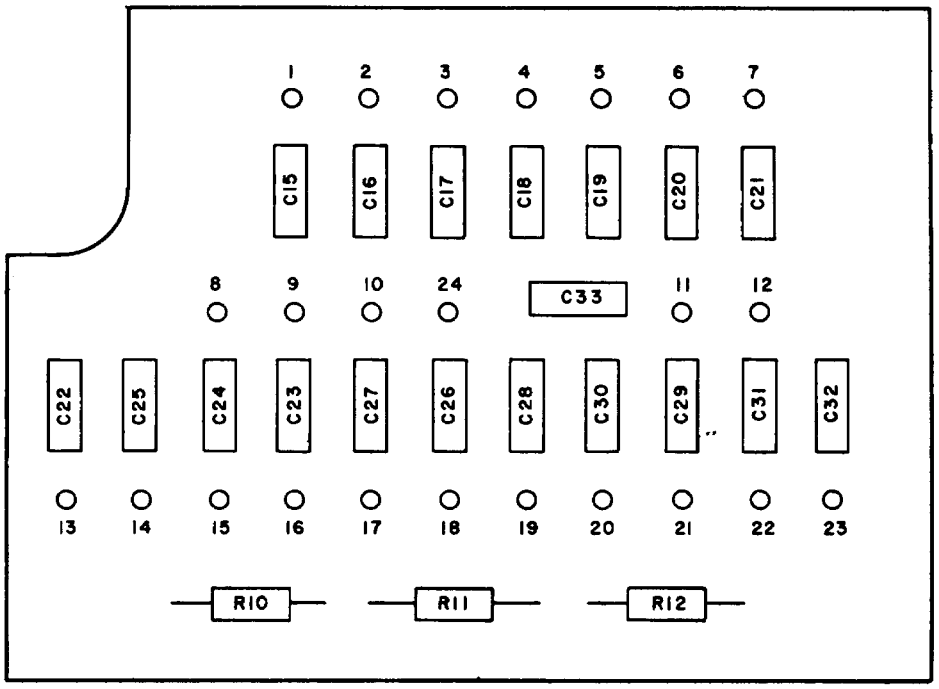
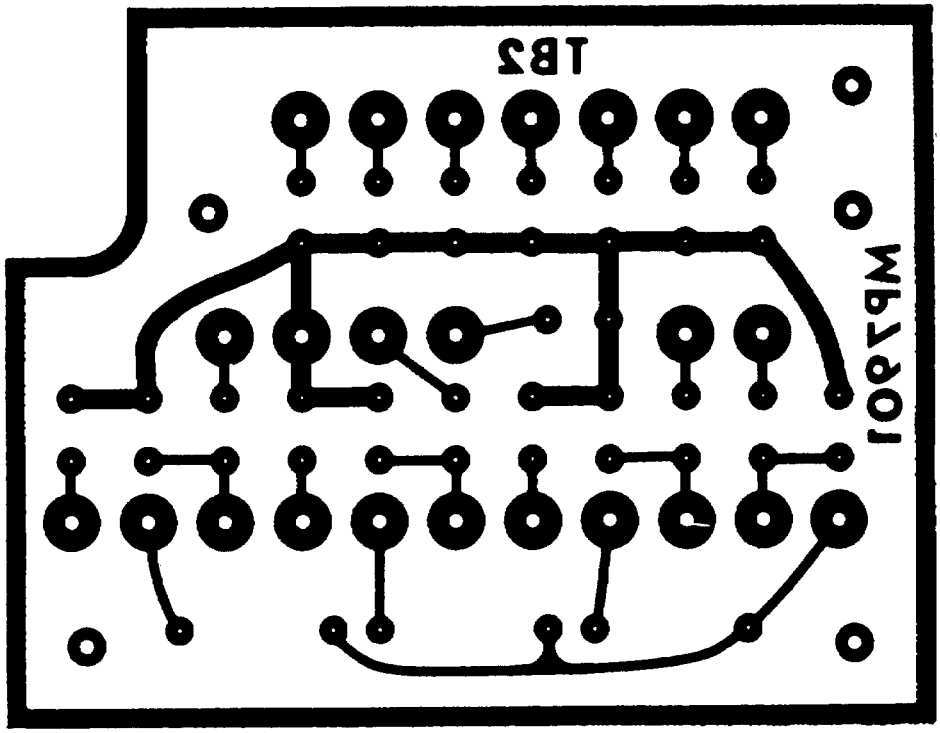
Figure 7-23. Printed wiring board assembly 1A12A15A2TB1, parts location and printed wiring diagram.



A. PARTS ON FRONT OF BOARD TB2 (651728).



B. WIRING ON BACK OF BOARD TB2 (VIEWED THROUGH FRONT).

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A15A1TB2.

EL5820-595-35-222

Figure 7-24. Printed wiring board assembly 1A12A15A1TB2, parts location and printed wiring diagram.

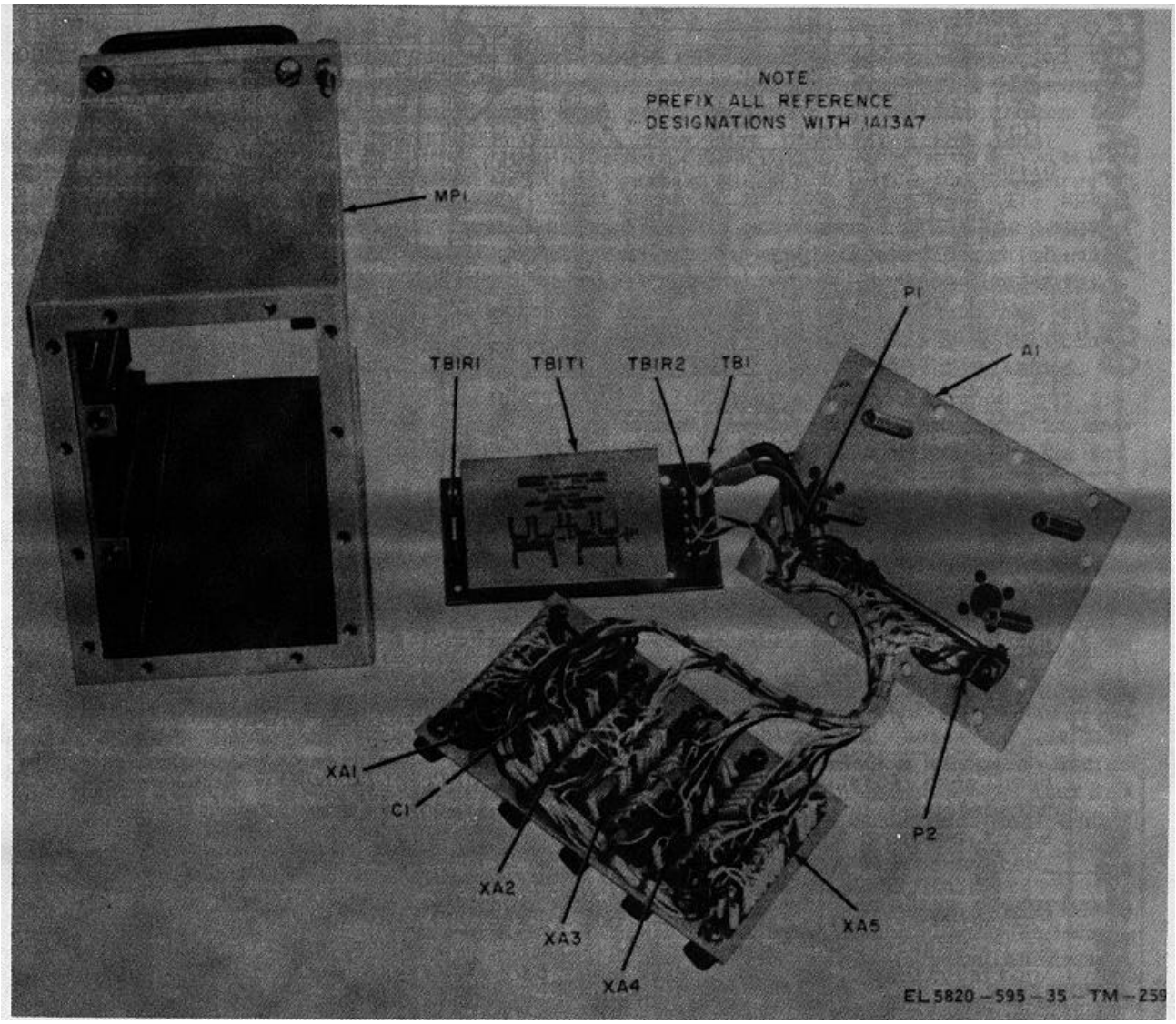


Figure 7-25. Orderwire chassis 1A13A7, partially disassembled, parts location.

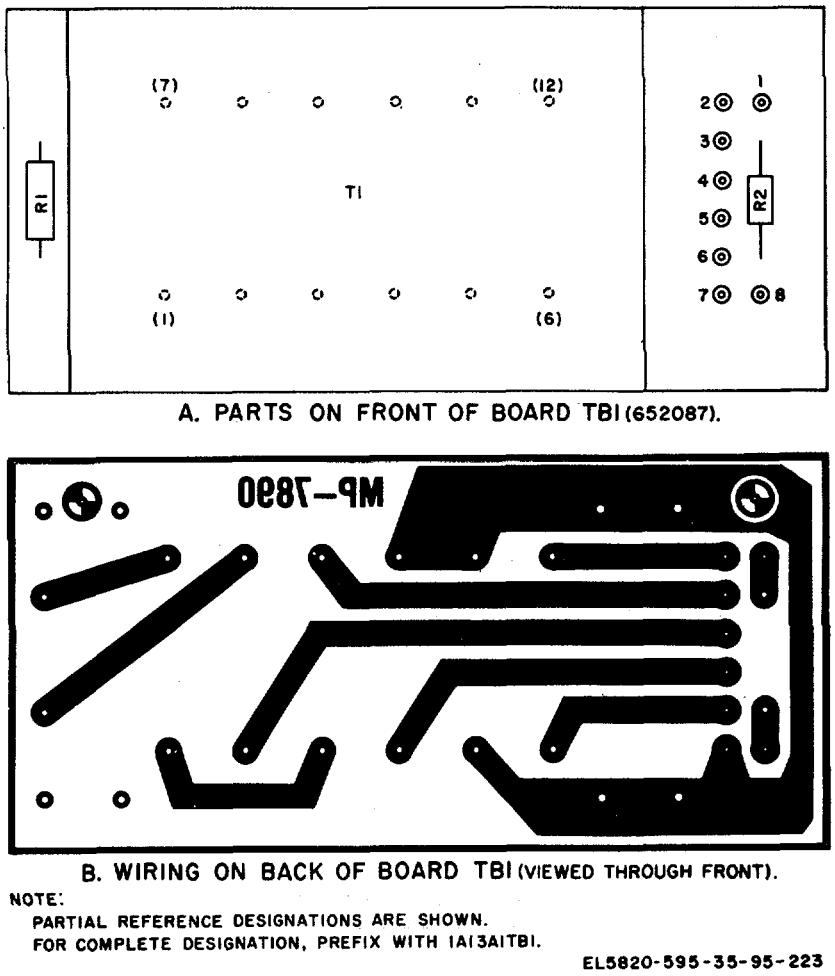


Figure 7-26. Printed wiring board assembly 1A13A7TB1, parts location and printed wiring diagram.

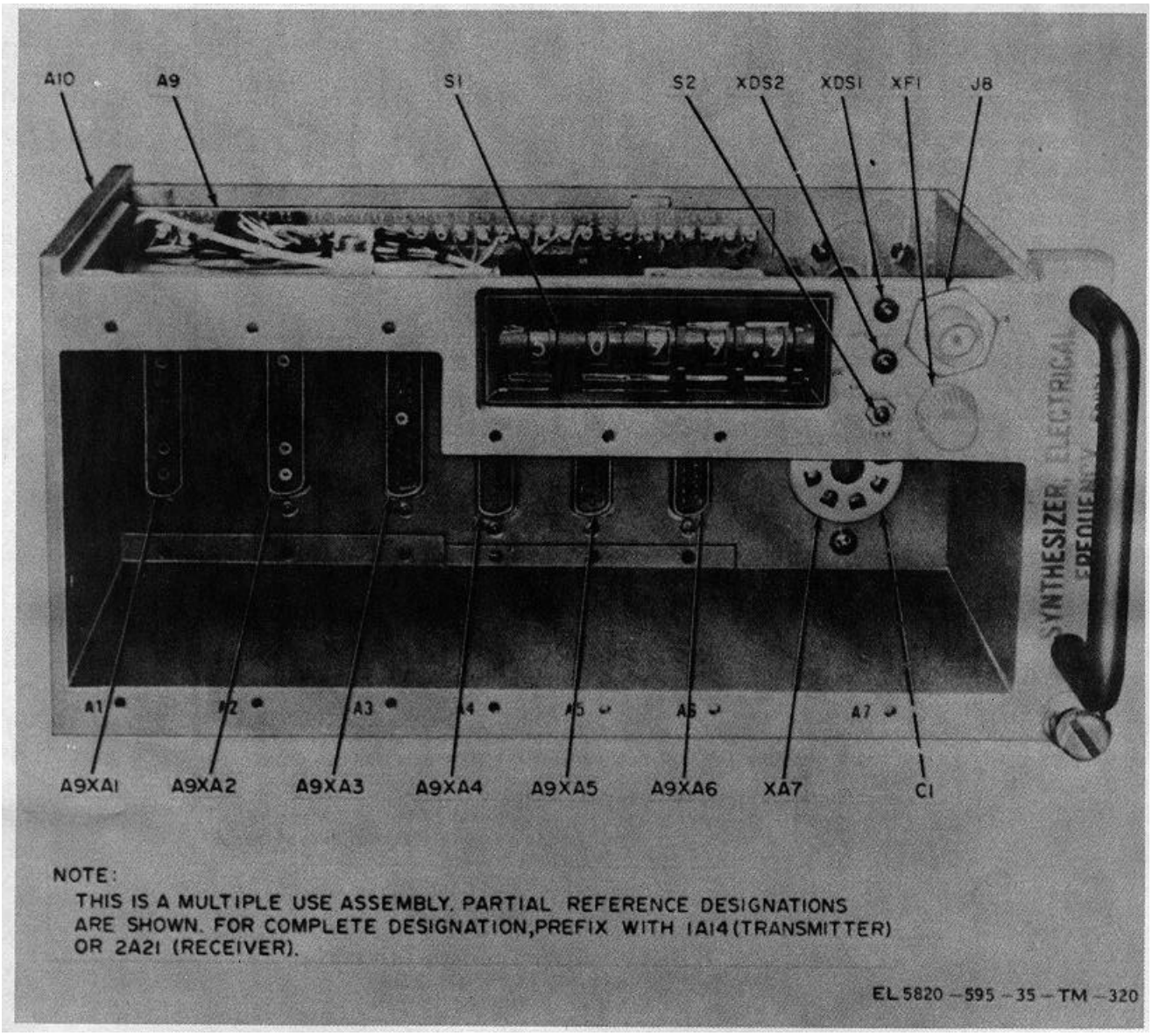


Figure 7-27. Frequency synthesizer 1A14/2A21, partially disassembled, front view, parts location.

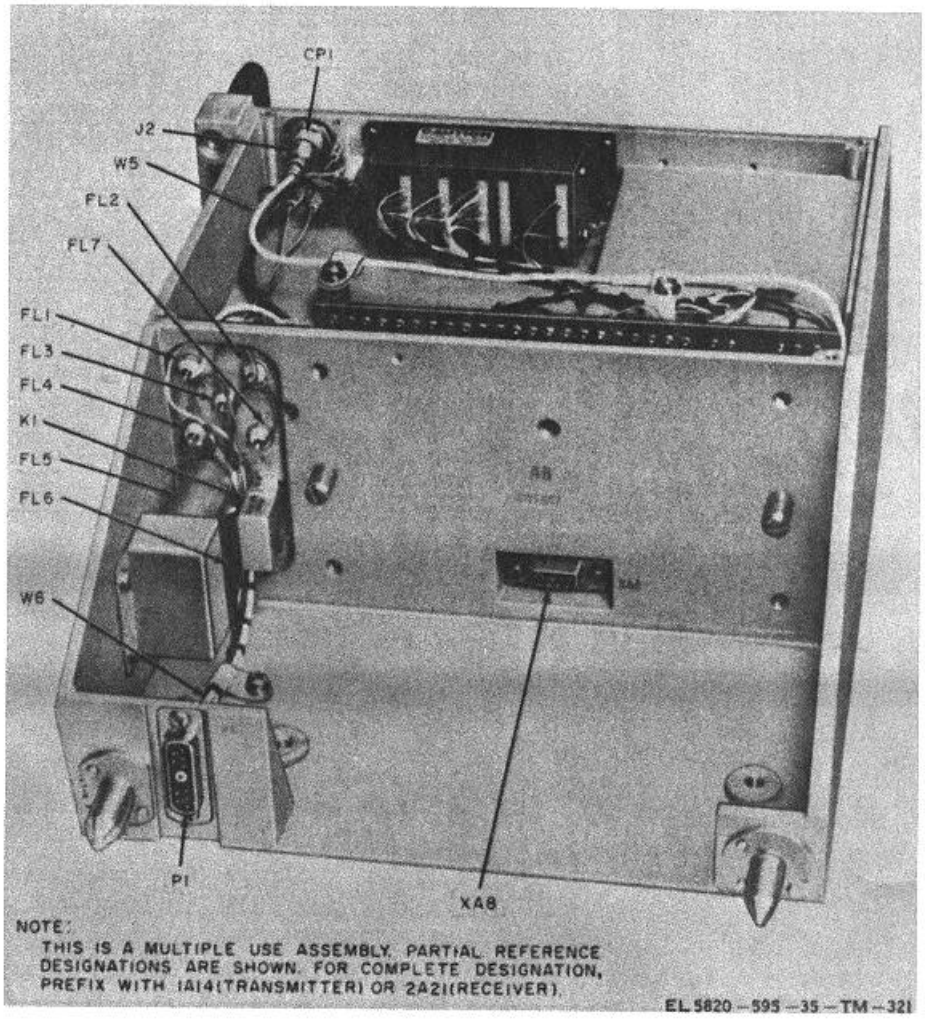


Figure 7-28. Frequency synthesizer 1A14/2A21, partially disassembled, rear view, parts location.

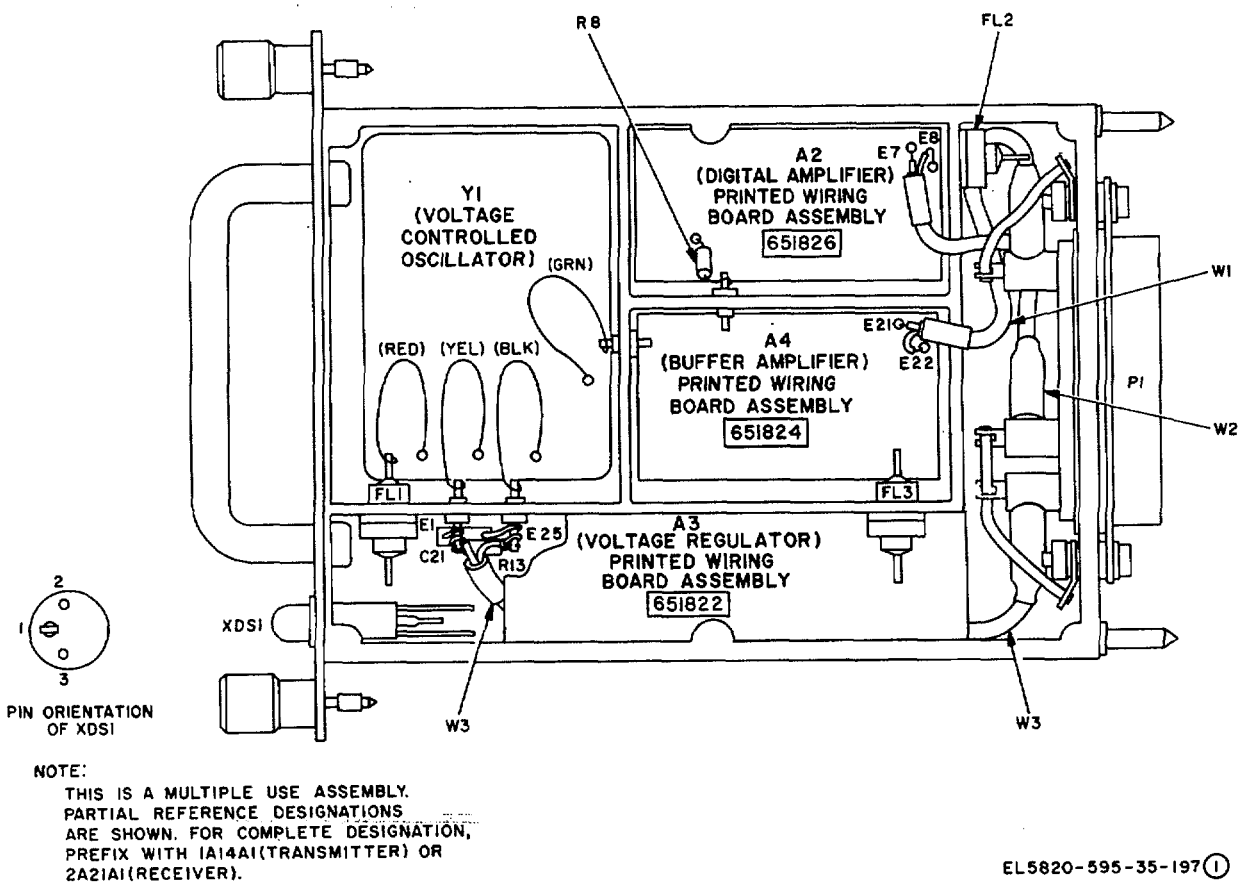


Figure 7-29(1). RF oscillator 1A14A1/2A21A1, parts location and printed wiring diagram (part 1 of 4).

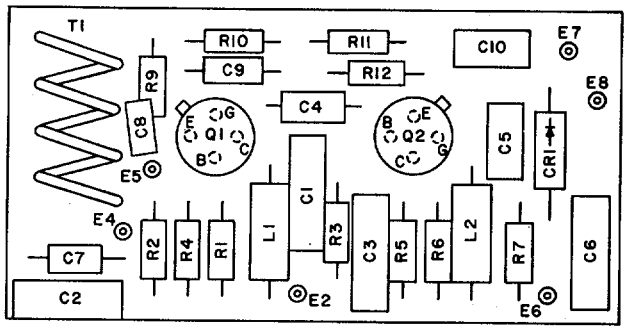
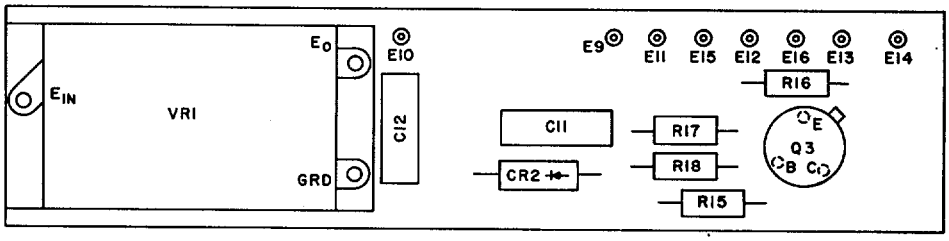


Figure 7-29(2). RF oscillator 1A14A1/2A21A1, parts location and printed wiring diagram (part 2 of 4).



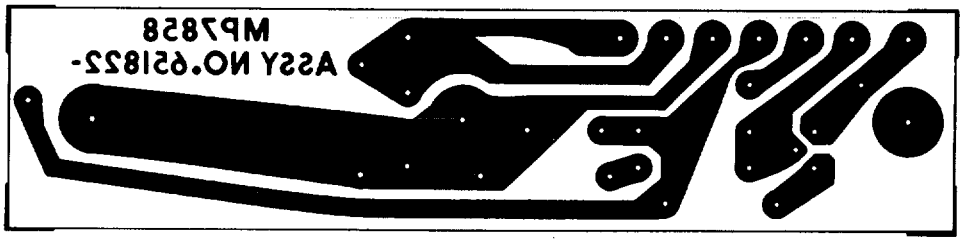


Figure 7-29(3). RF oscillator 1A14A1/2A21A1, parts location and printed wiring diagram (part 3 of 4).

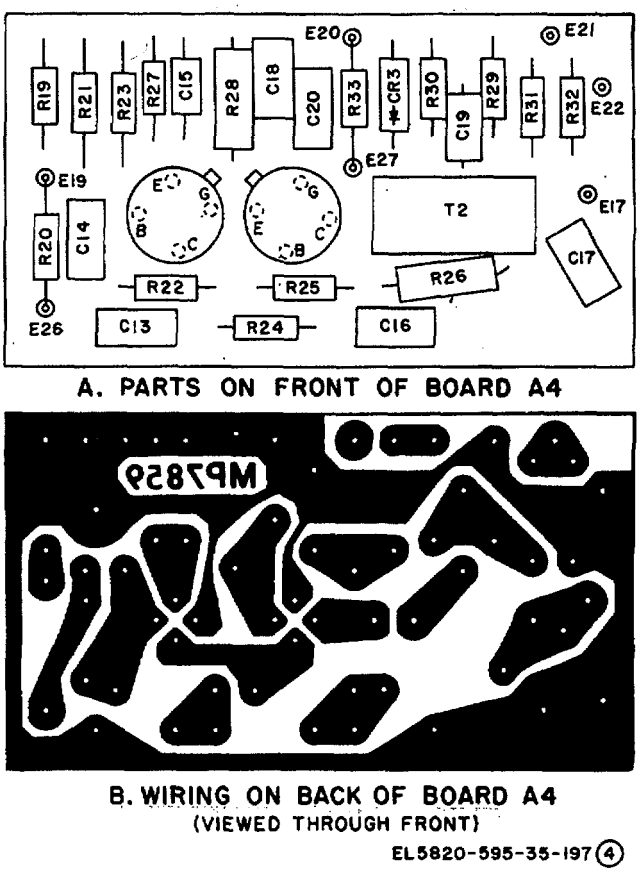
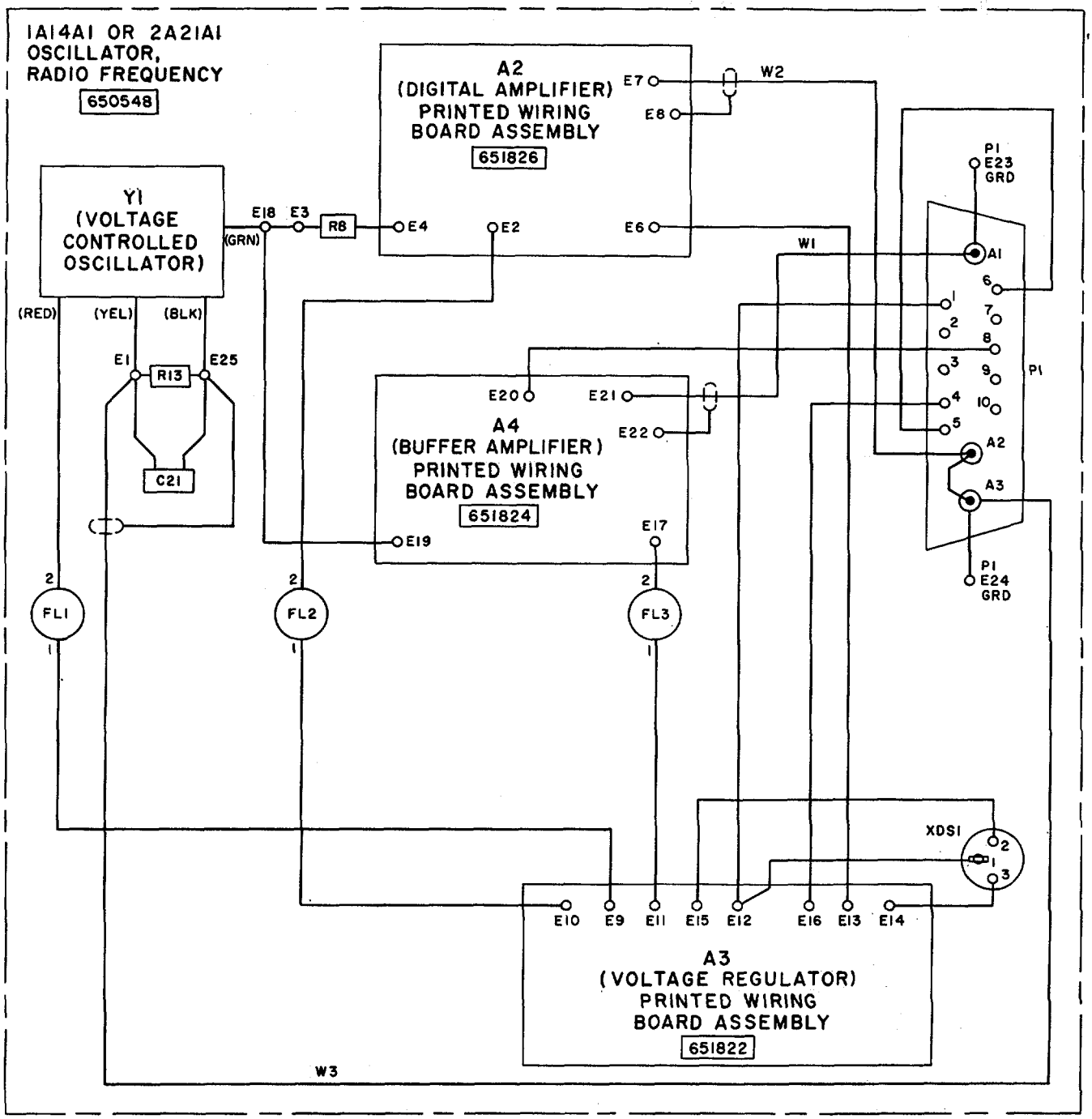


Figure 7-29(4). RF oscillator 1A14A1/2A21A1, parts location and printed wiring diagram (part 4 of 4).



NOTE:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

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Figure 7-30. RF oscillator 1A14A1/2A21A1 assembly, wiring diagram.

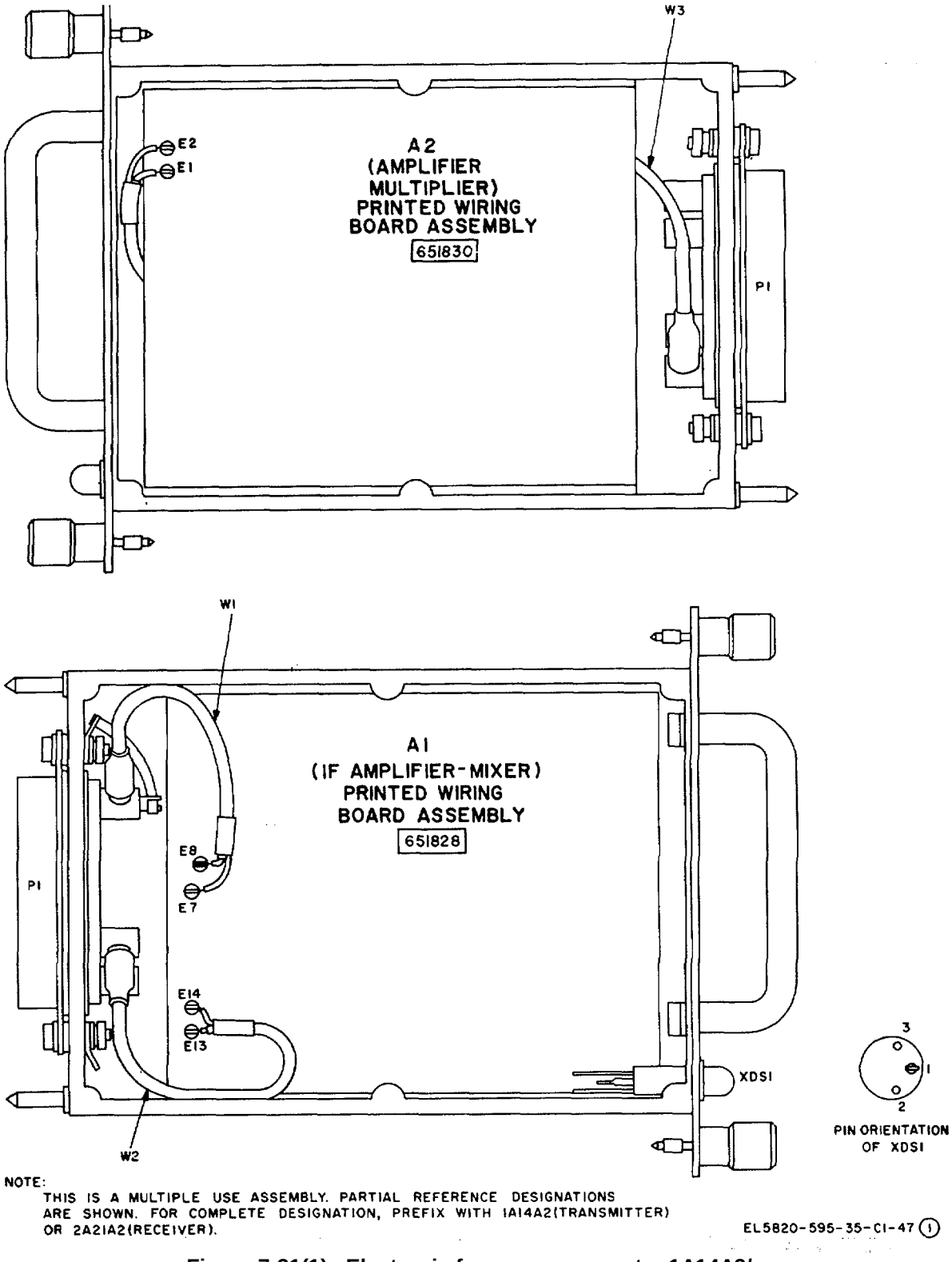
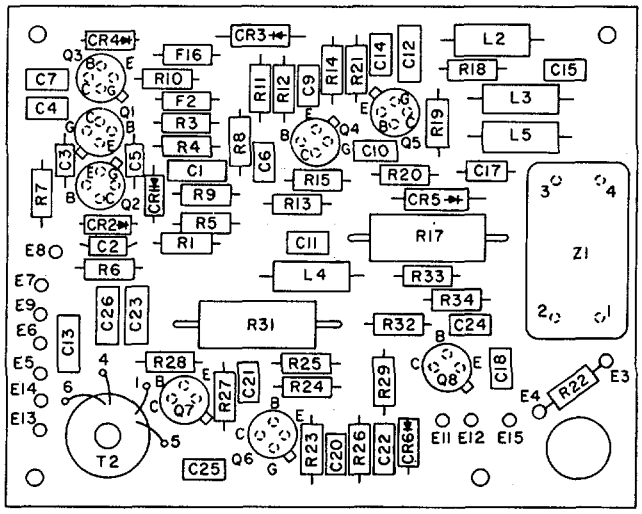
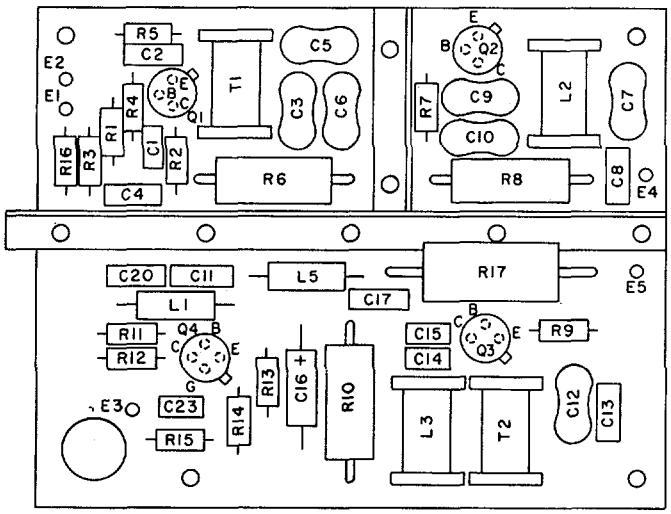


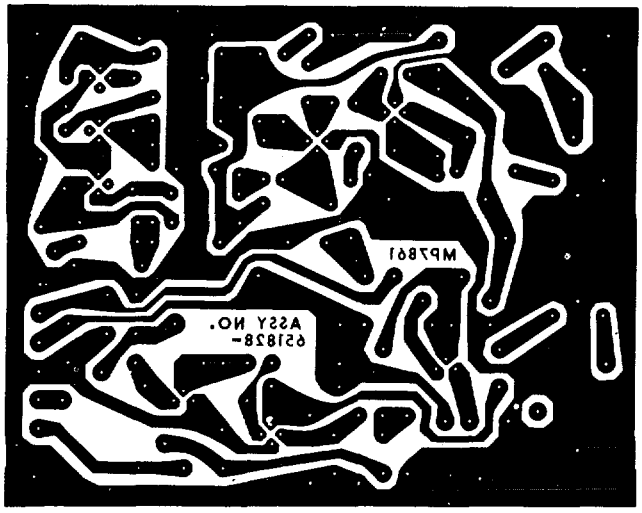
Figure 7-31(1). Electronic frequency converter 1A14A2/ 2A21A2, parts location and printed wiring diagram (part 1 of 2).



A. PARTS ON FRONT OF BOARD A1



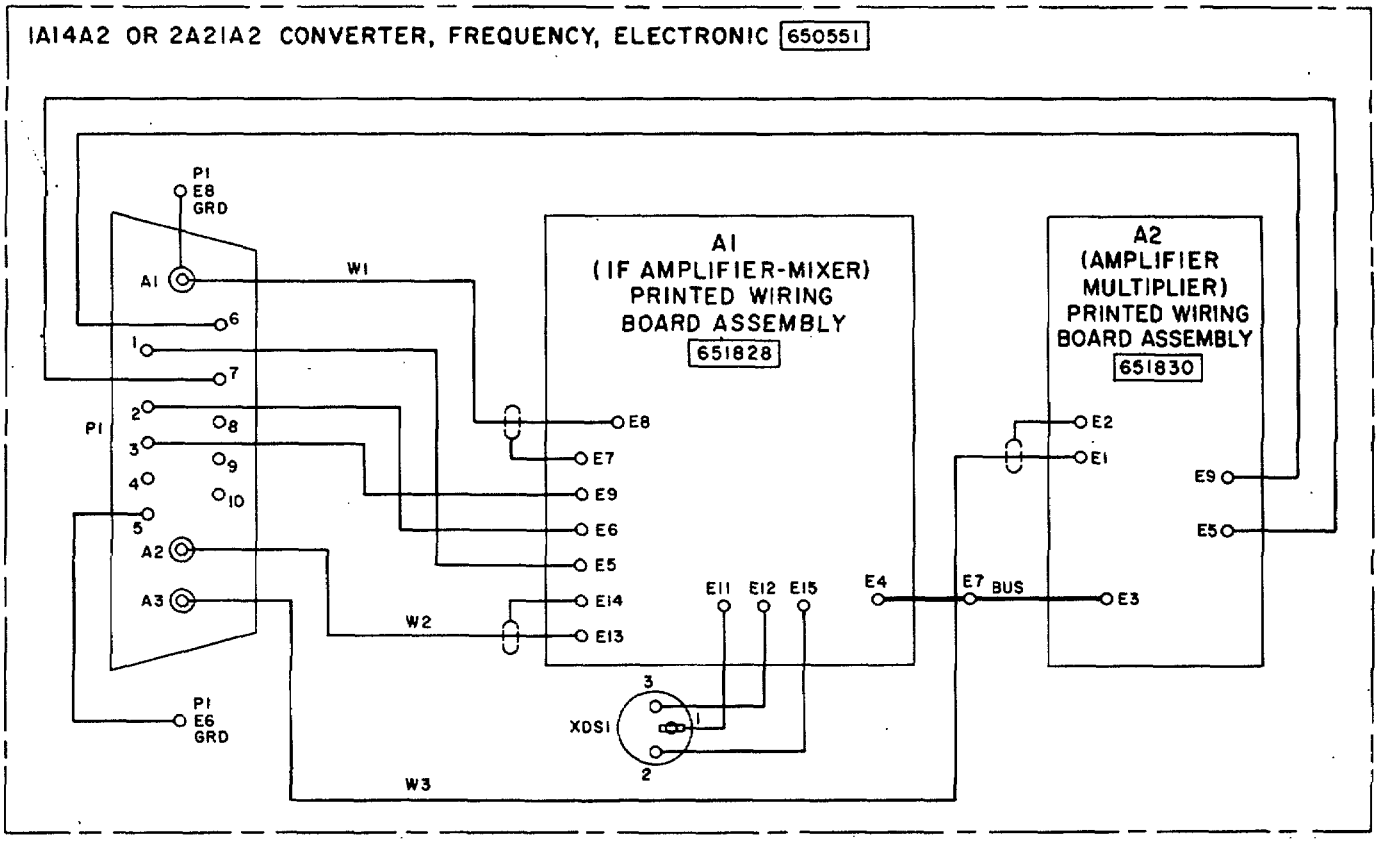
B. PARTS ON FRONT OF BOARD A2



C. WIRING ON BACK OF BOARD A1
(VIEWED THROUGH FRONT)

D. WIRING ON BACK OF BOARD A2
(VIEWED THROUGH FRONT)

EL5820-595-35-CI-47(2)



NOTE:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

EL5820-595-35-CI-48

Figure 7-32. Electronic frequency converter 1A14A2/ 2A21A2 assembly, wiring diagram.

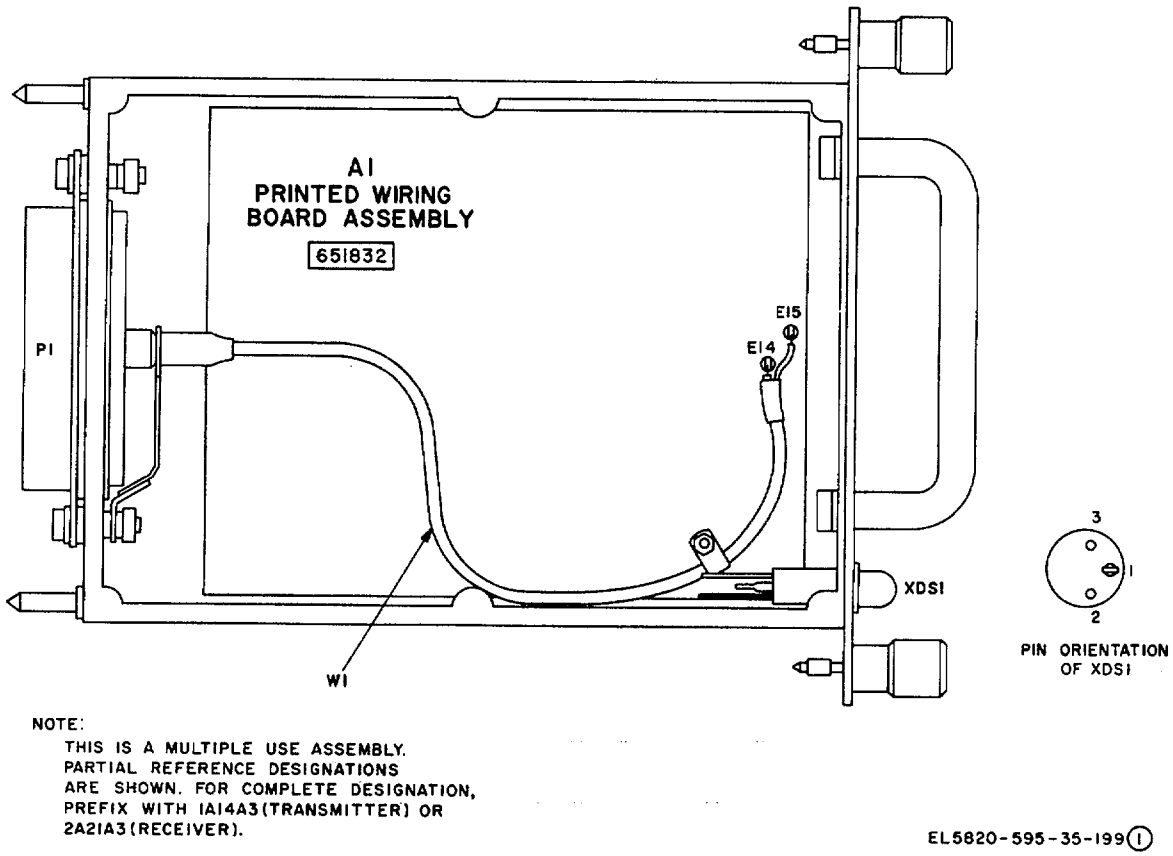
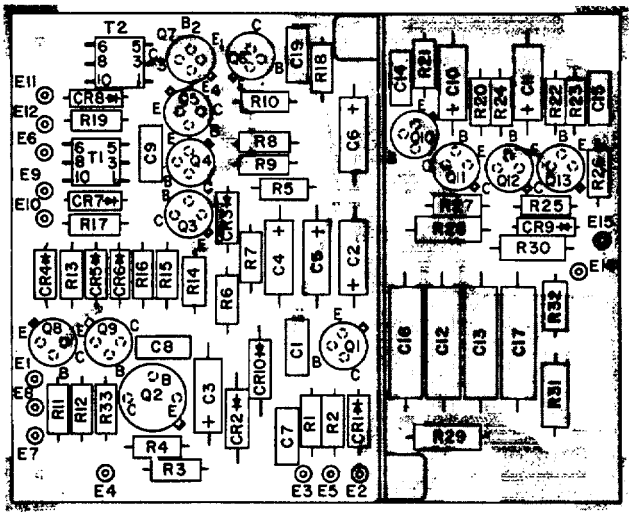


Figure 7-33(1). AF phase error detector 1A14A3/2A21A3, parts location and printed wiring diagram (part 1 of 2).



A. PARTS AND WIRING ON FRONT OF BOARD AI

B. WIRING ON BACK OF BOARD AI
(VIEWED THROUGH FRONT)

EL5820-595-35-199 (2)

Figure 7-33(2). AF phase error detector 1A14A3/2A21A3, parts location and printed wiring diagram (part 2 of 2).

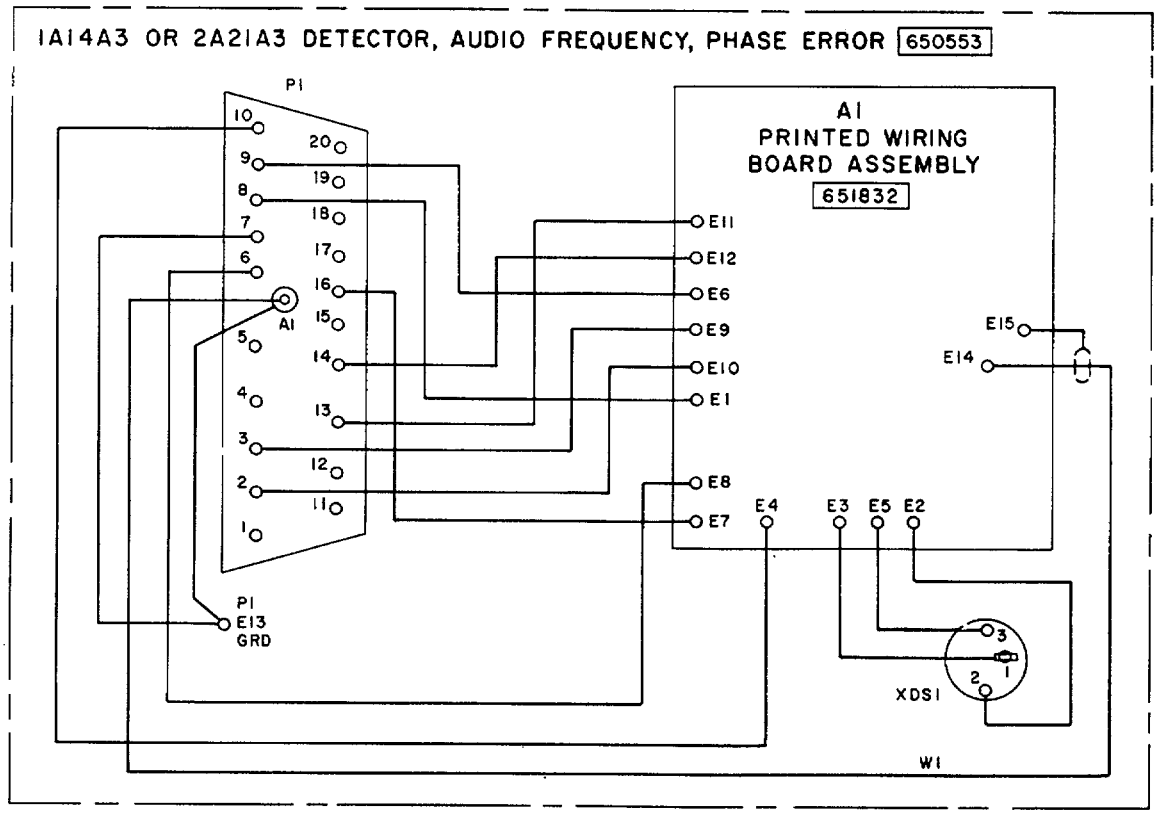


Figure 7-34. AF phase error detector 1A14A3/2A21A3 assembly, wiring diagram.

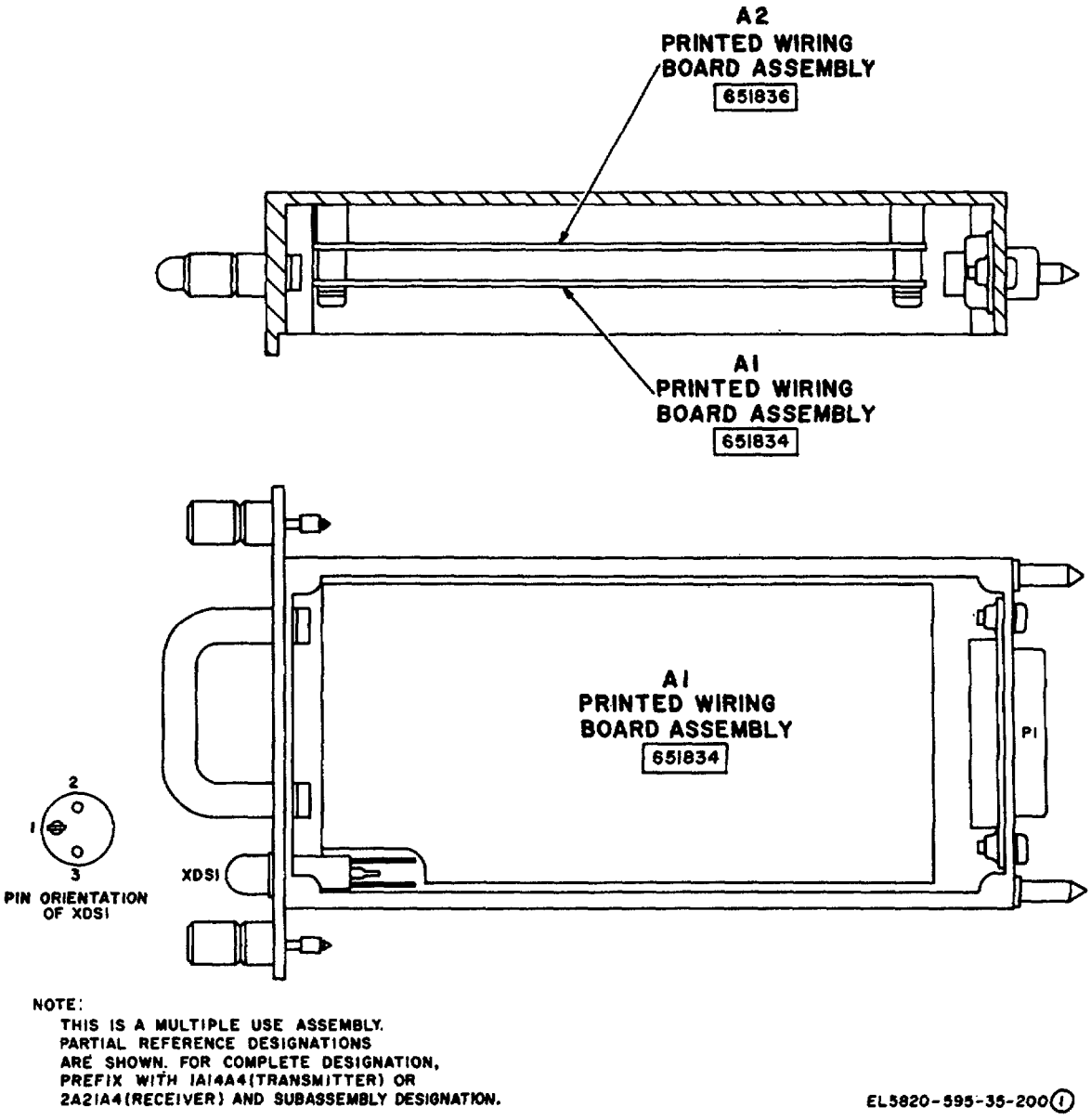
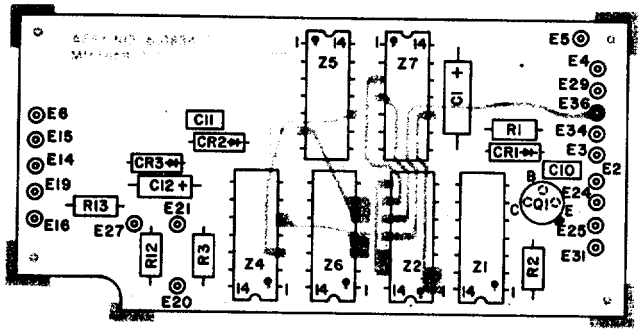
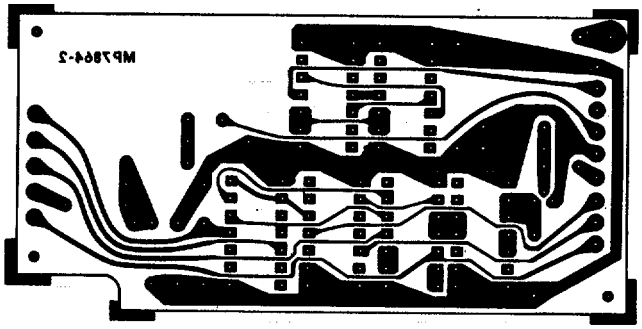


Figure 7-35(1). Variable frequency divider No. 1, 1A14A4/ 2A21A4, parts location and printed wiring diagram (part 1 of 3).



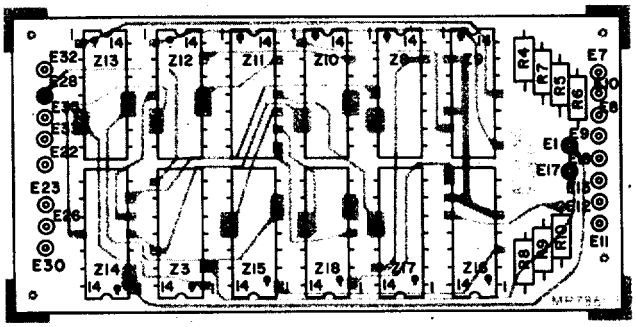
A. PARTS AND WIRING ON FRONT OF BOARD A1



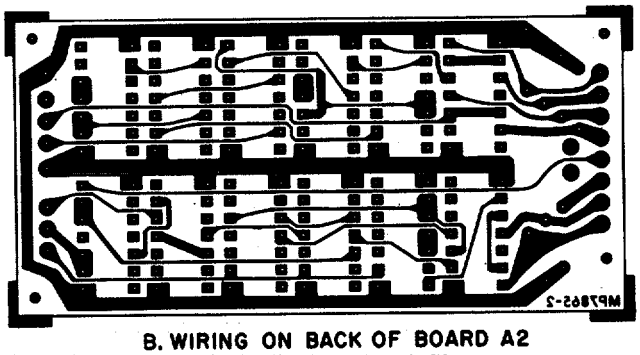
B. WIRING ON BACK OF BOARD A1
(VIEWED THROUGH FRONT)

EL5820-595-35-200 (2)

Figure 7-35(2). Variable frequency divider No. 1, 1A14A4/ 2A21A4, parts location and printed wiring diagram (part 2 of 3).



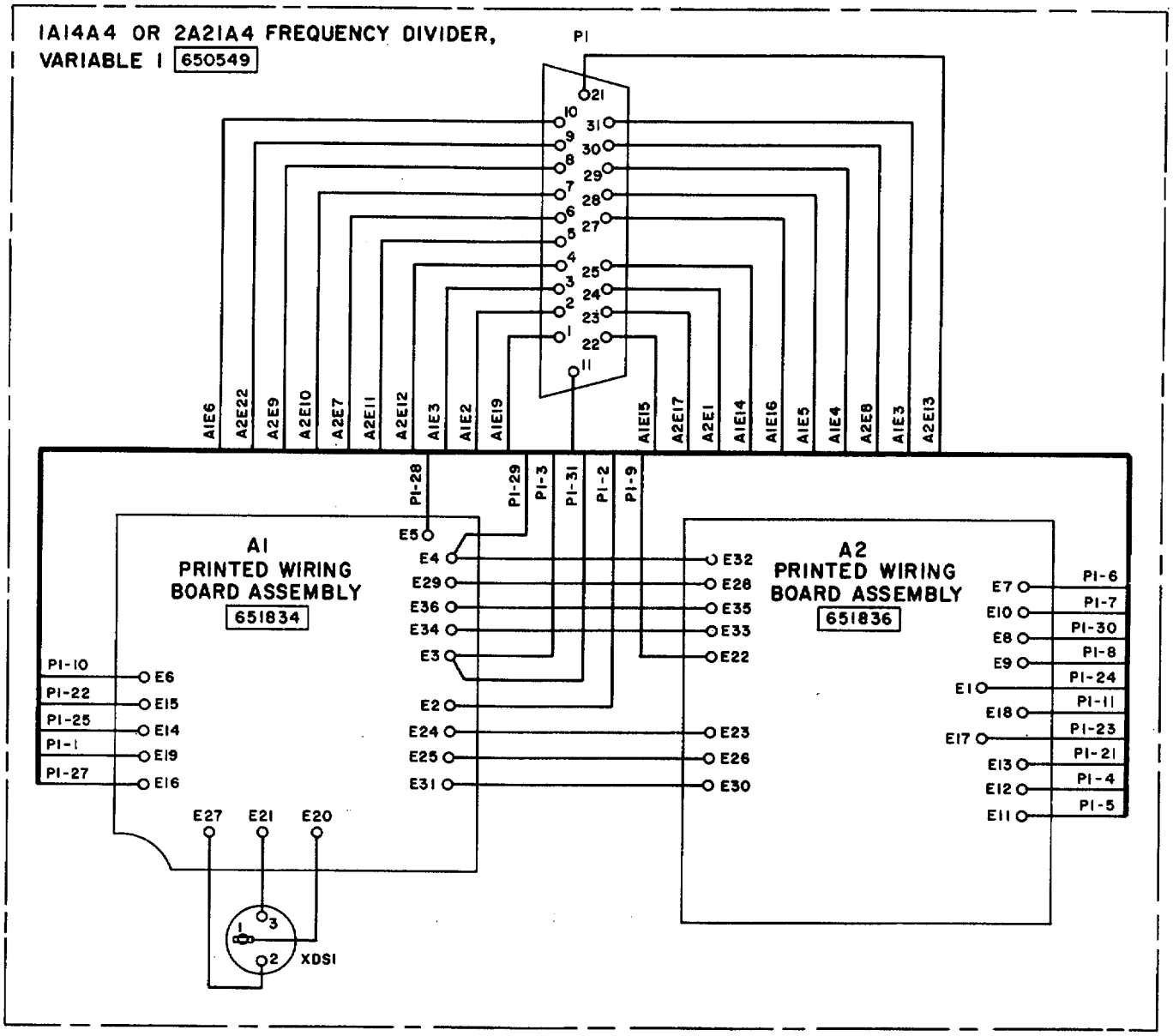
A. PARTS AND WIRING ON FRONT OF BOARD A2



B. WIRING ON BACK OF BOARD A2
(VIEWED THROUGH FRONT)

EL5820-595-35-200 ③

Figure 7-35(3). Variable frequency divider No. 1, 1A14A4/ 2A21A4, parts location and printed wiring diagram (part 3 of 3).

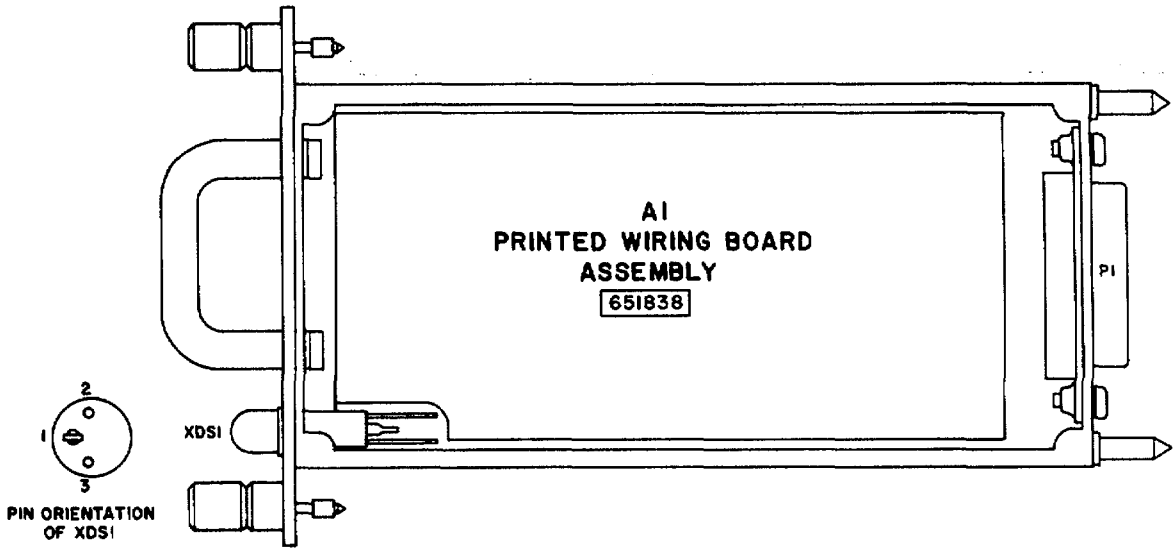


NOTE:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

EL5820-595-35-165

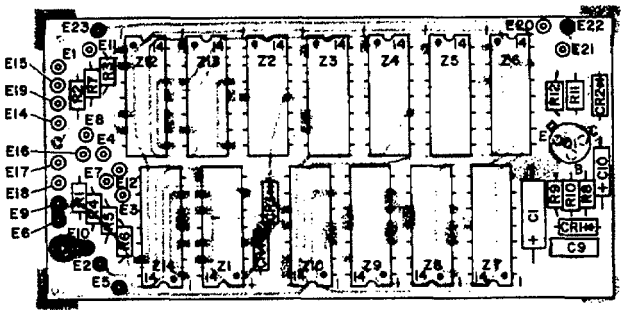
Figure 7-36. Variable frequency divider No. 1, 1A14A4/ 2A21A4 assembly, wiring diagram.



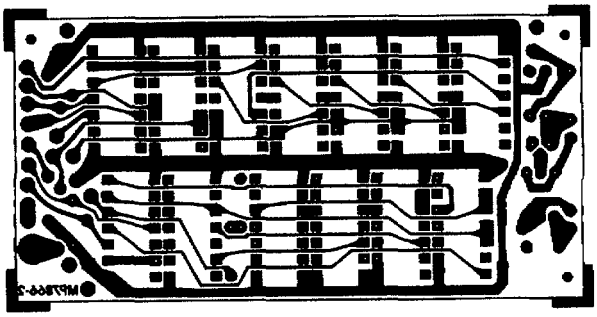
NOTE:
THIS IS A MULTIPLE USE ASSEMBLY.
PARTIAL REFERENCE DESIGNATIONS
ARE SHOWN. FOR COMPLETE DESIGNATION,
PREFIX WITH 1A14A5(TRANSMITTER) OR
2A21A5(RECEIVER).

EL5820-595-35-201 (1)

Figure 7-37(1). Variable frequency divider No. 2, 1A14A5/ 2A21A5, parts location and printed wiring diagram (part 1 of 2).



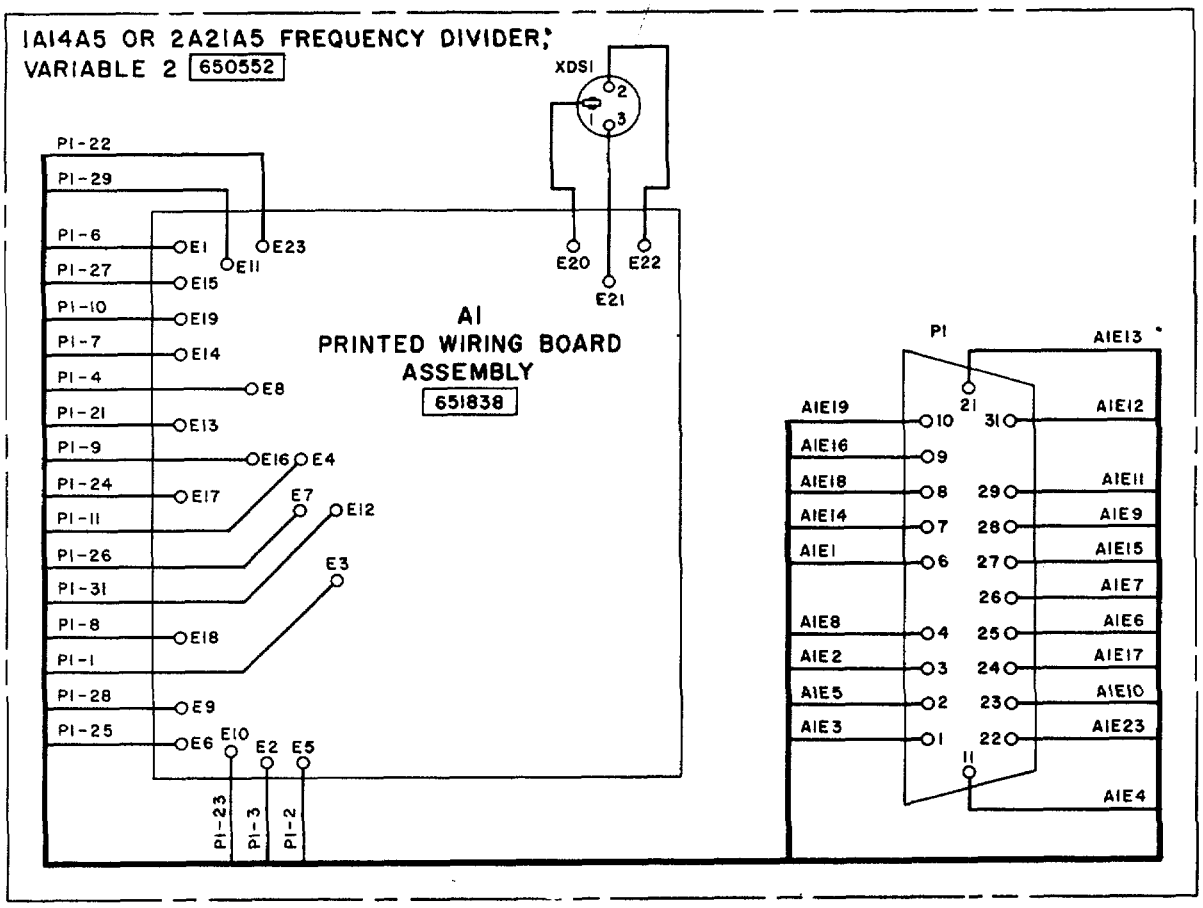
A. PARTS AND WIRING ON FRONT OF BOARD A1



B. WIRING ON BACK OF BOARD A1
(VIEWED THROUGH FRONT)

EL5820-595-35-201 (2)

Figure 7-37(2). Variable frequency divider No. 2, 1A14A5/ 2A21A5, parts location and printed wiring diagram (part 2 of 2).



NOTES:
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER, AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

EL5820-595-35-CI-50

Figure 7-38. Variable frequency divider No. 2, 1A14A5/ 2A21A5 assembly, wiring diagram.

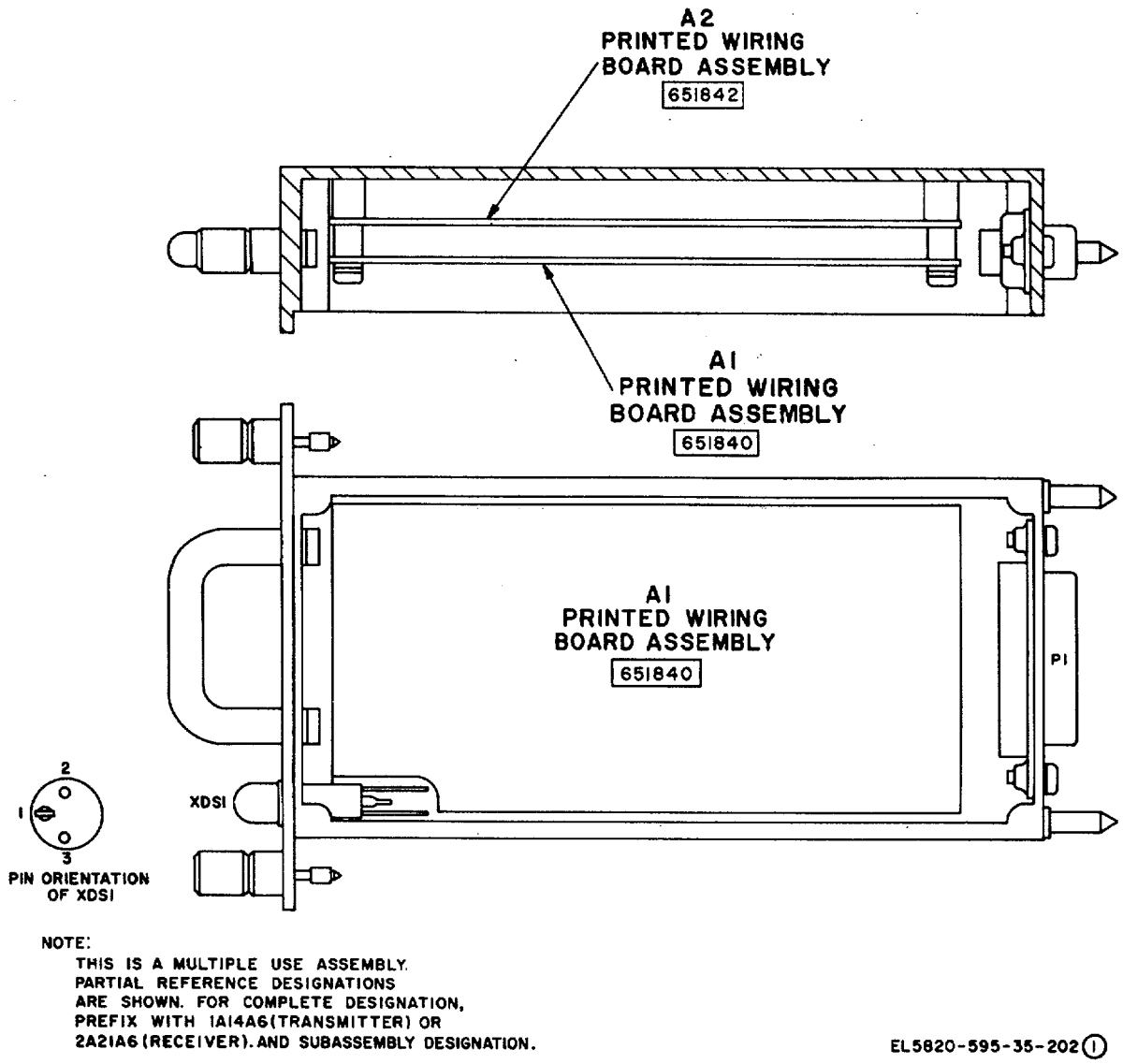


Figure 7-39(1). Fixed frequency divider 1A14A6/2A21A6, parts location and printed wiring diagram (part 1 of 3).

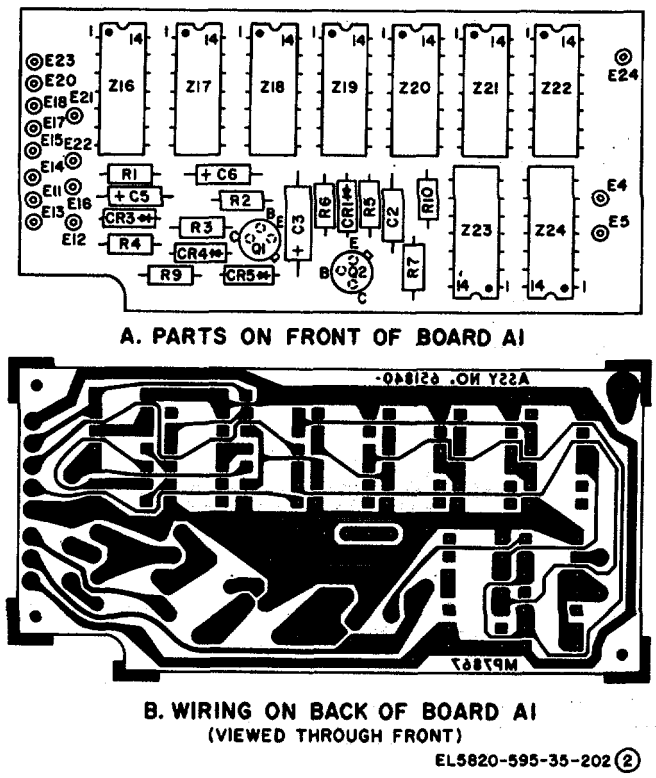
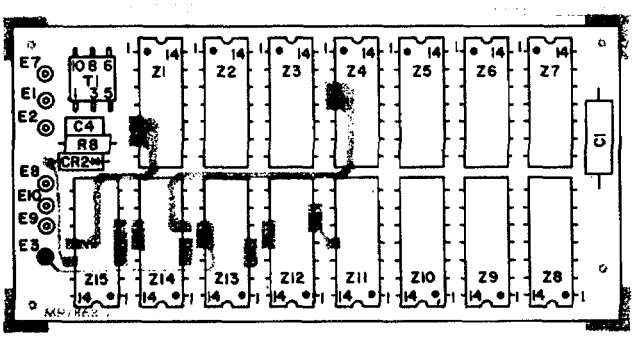
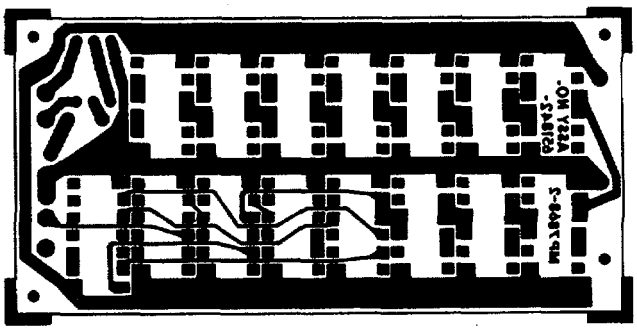


Figure 7-39(2). Fixed frequency divider 1A14A6/2A21A6, parts location and printed wiring diagram (part 2 of 3).



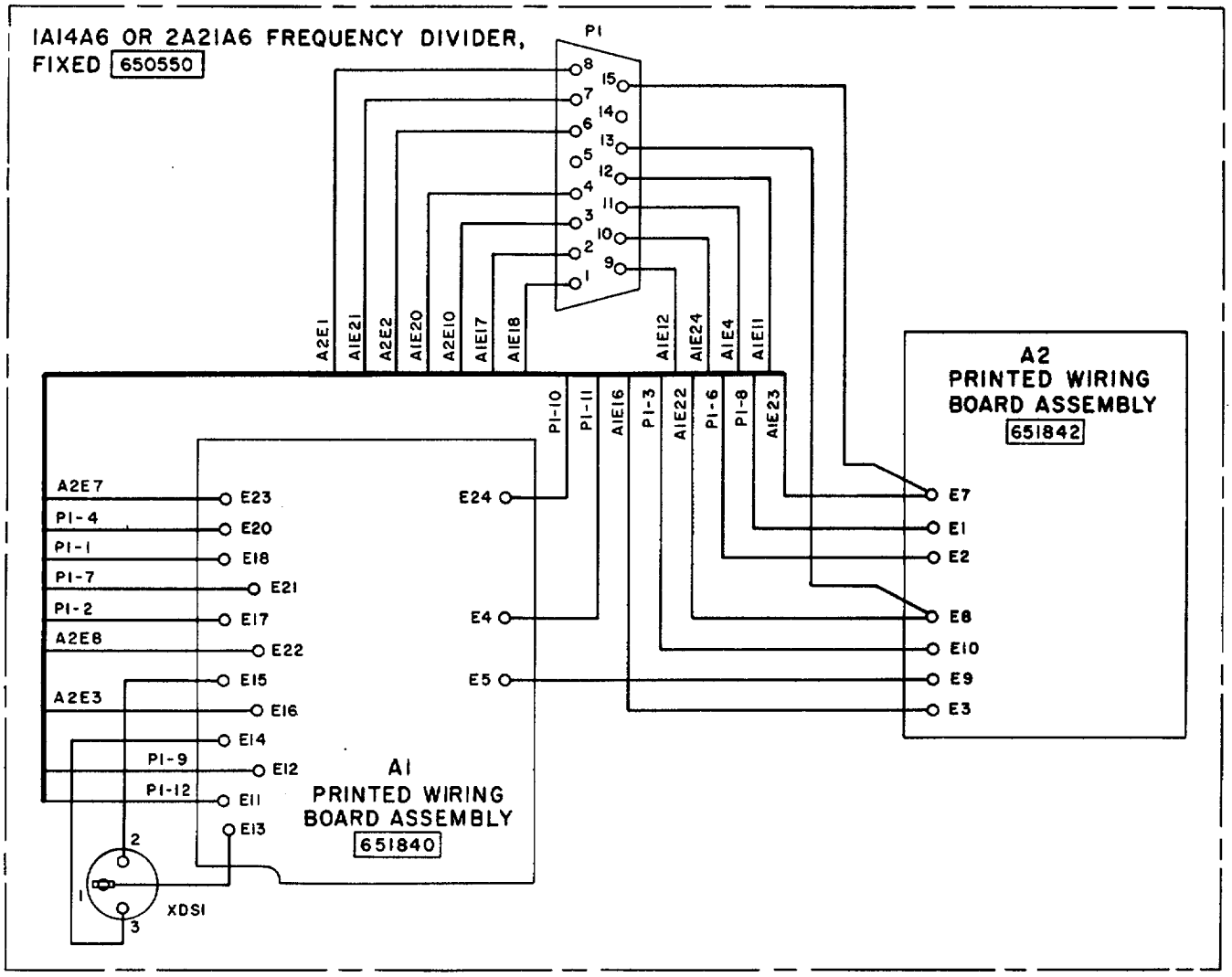
A. PARTS AND WIRING ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A2
(VIEWED THROUGH FRONT)

EL5820-595-35-202 ⑤

Figure 7-39(3). Fixed frequency divider 1A14A6/2A21A6, parts location and printed wiring diagram (part 3 of 3).



NOTE:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 26 AWG.

EL5820-595-35-CI-51

Figure 7-40. Fixed frequency divider 1A14A6/A1A21A6 assembly, wiring diagram.

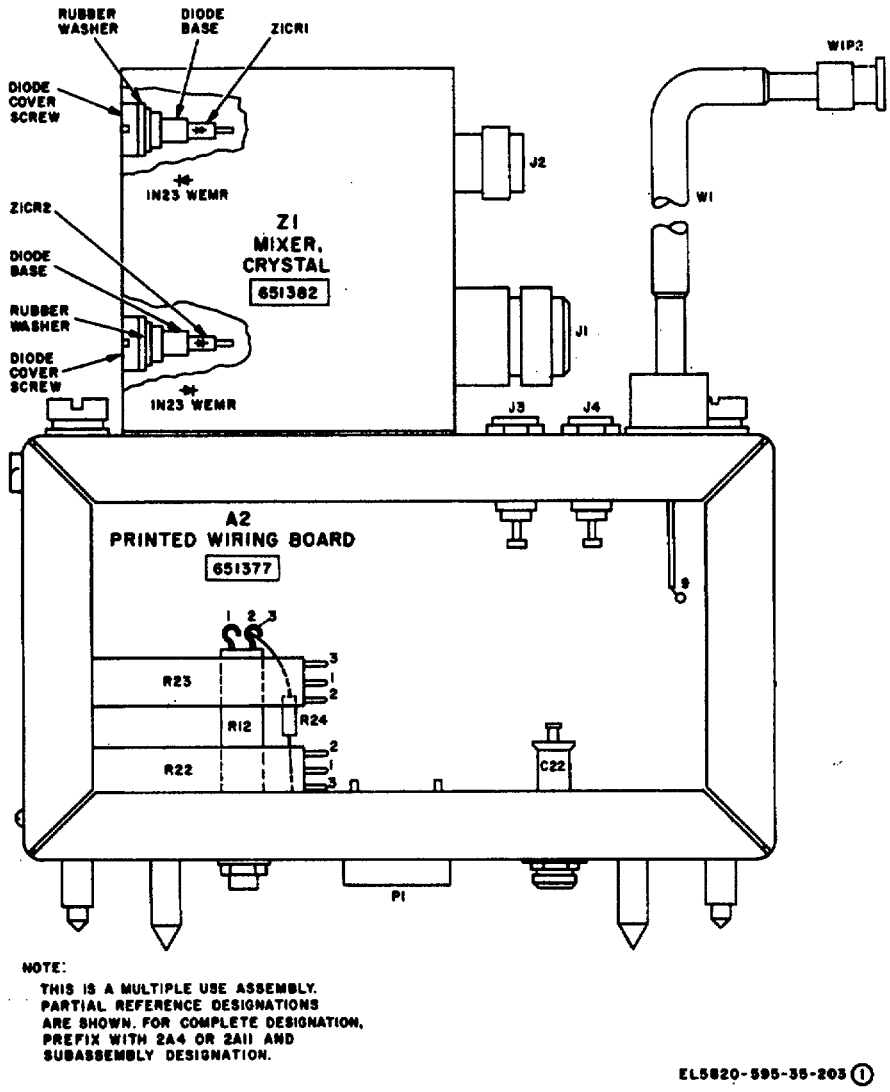
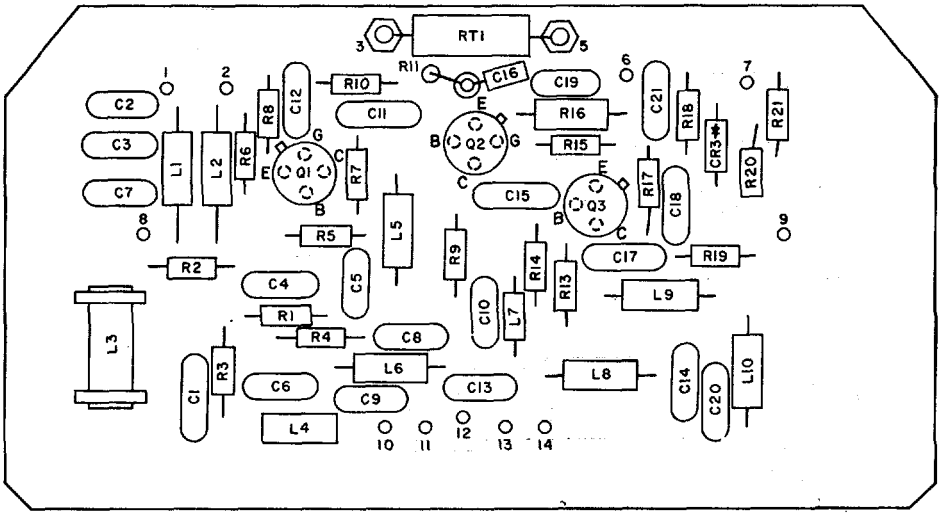
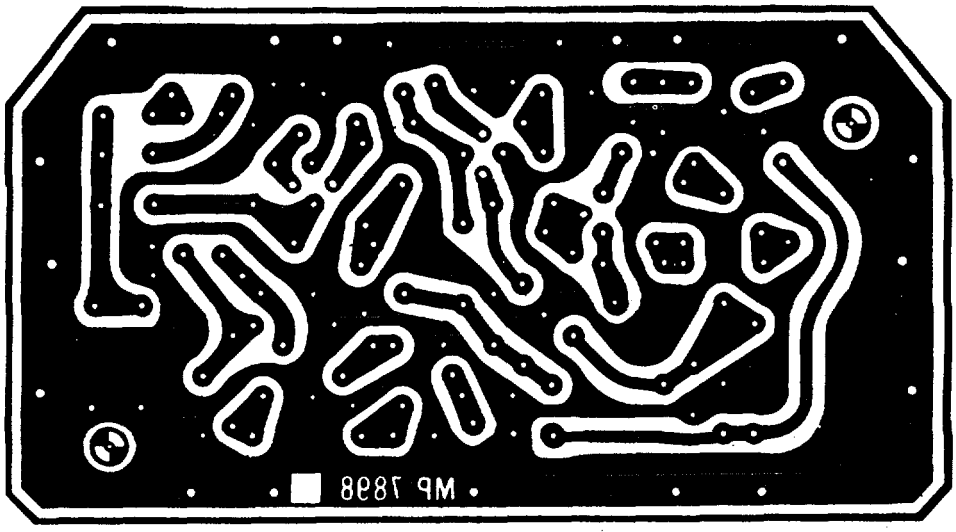


Figure 7-41(1). Mixer preamplifier SA41/A11, parts location and printed wiring diagram (part 1 of 2).



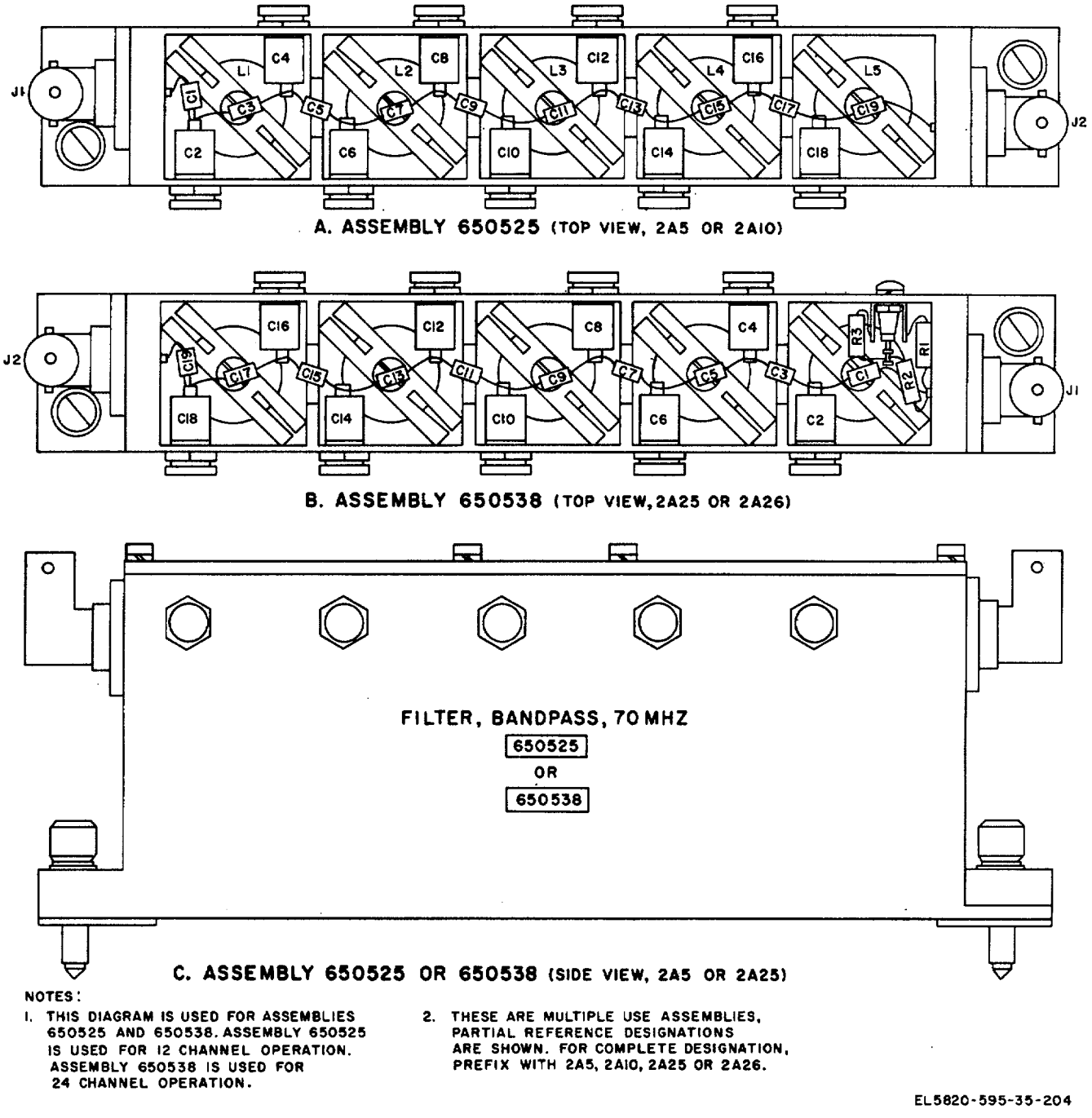
A. PARTS ON FRONT OF BOARD A2.



B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

EL5820-595-35-203 (2)

Figure 7-41(2). Mixer preamplifier 2A4/2All, parts location and printed wiring diagram (part 2 of 2).



NOTES:

1. THIS DIAGRAM IS USED FOR ASSEMBLIES 650525 AND 650538. ASSEMBLY 650525 IS USED FOR 12 CHANNEL OPERATION. ASSEMBLY 650538 IS USED FOR 24 CHANNEL OPERATION.
2. THESE ARE MULTIPLE USE ASSEMBLIES, PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 2A5, 2A10, 2A25 OR 2A26.

EL5820-595-35-204

Figure 7-42. 750 kHz if filter 2A5/2A10, parts location diagram.

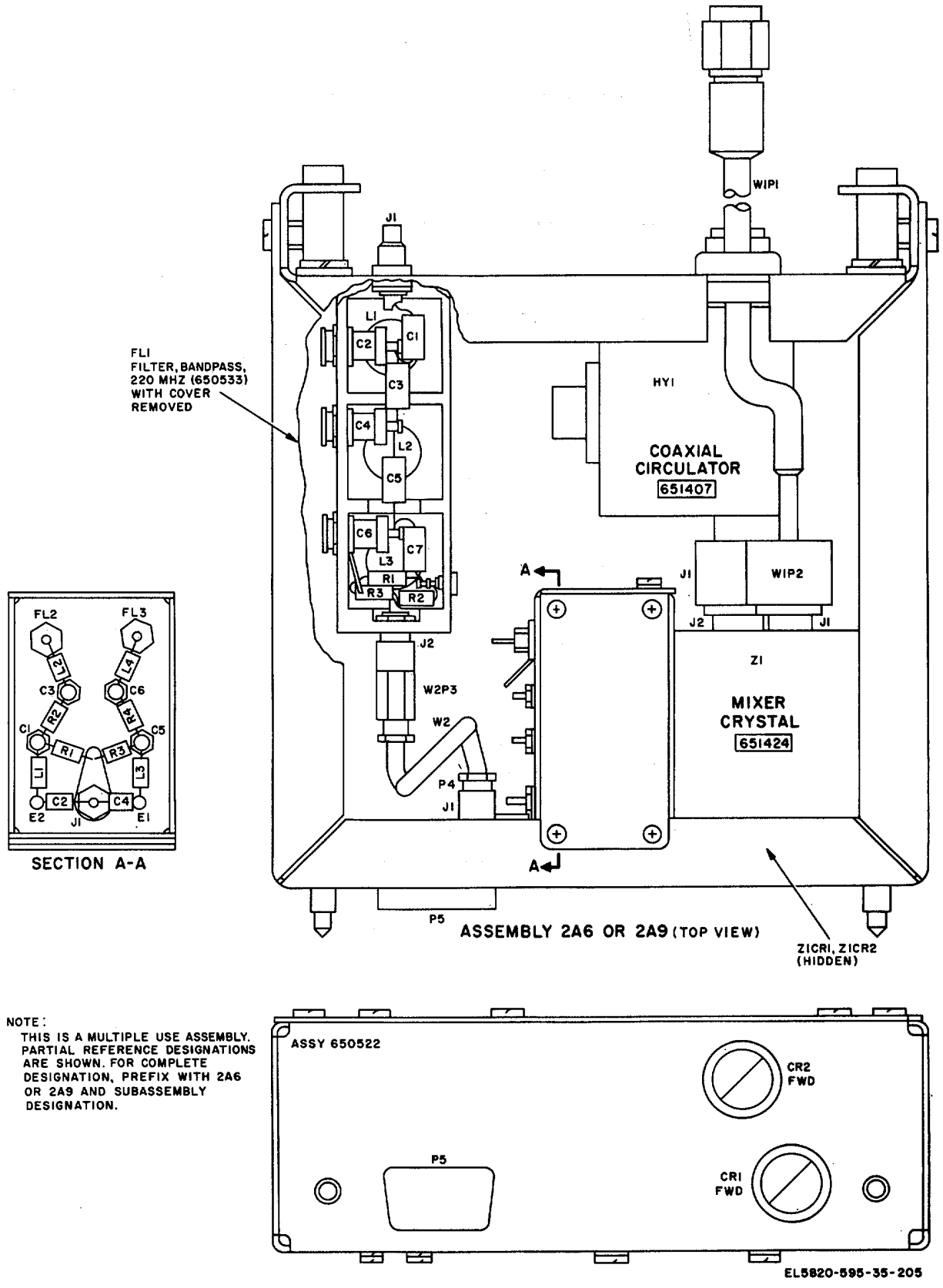
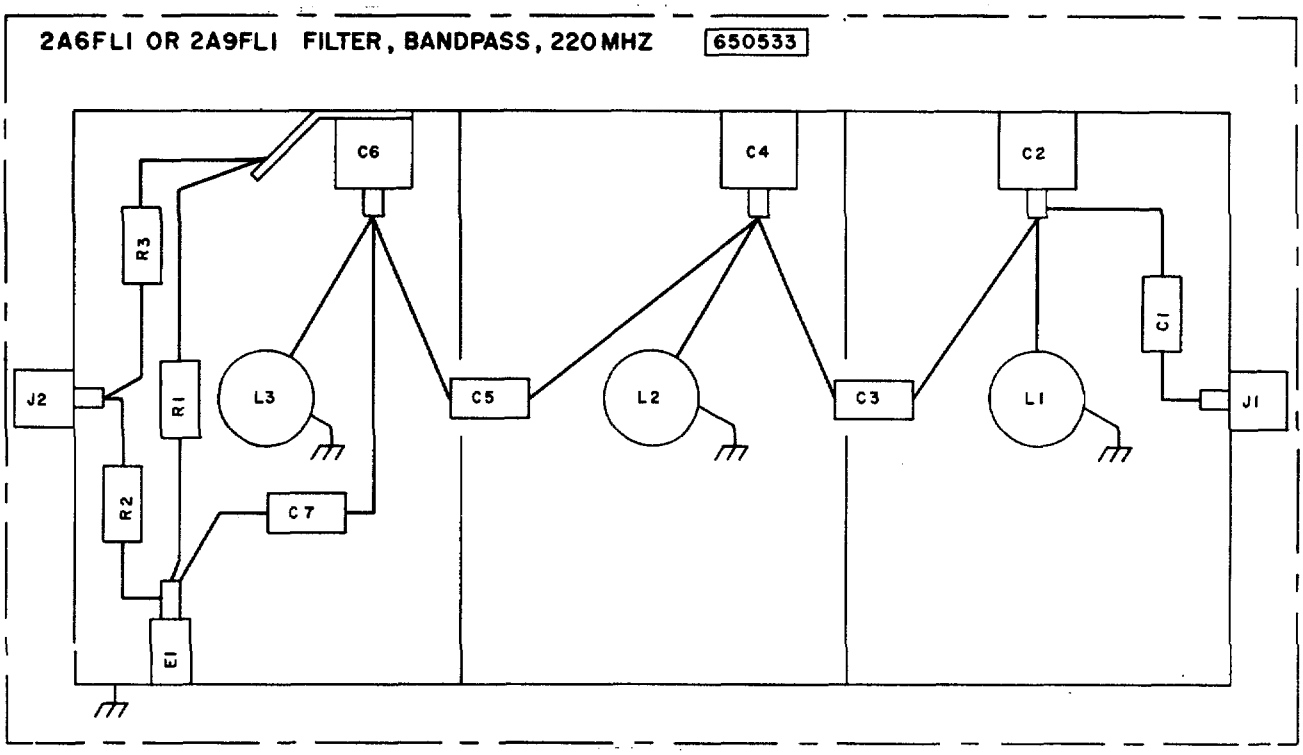


Figure 7-43. Frequency mixer 2A6/2A9, parts location diagram.



NOTE:

THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.

EL5820-595-35-115

Figure 7-44. 220 MHz bandpass filter 2A6FL1/2A9FL1, wiring diagram.

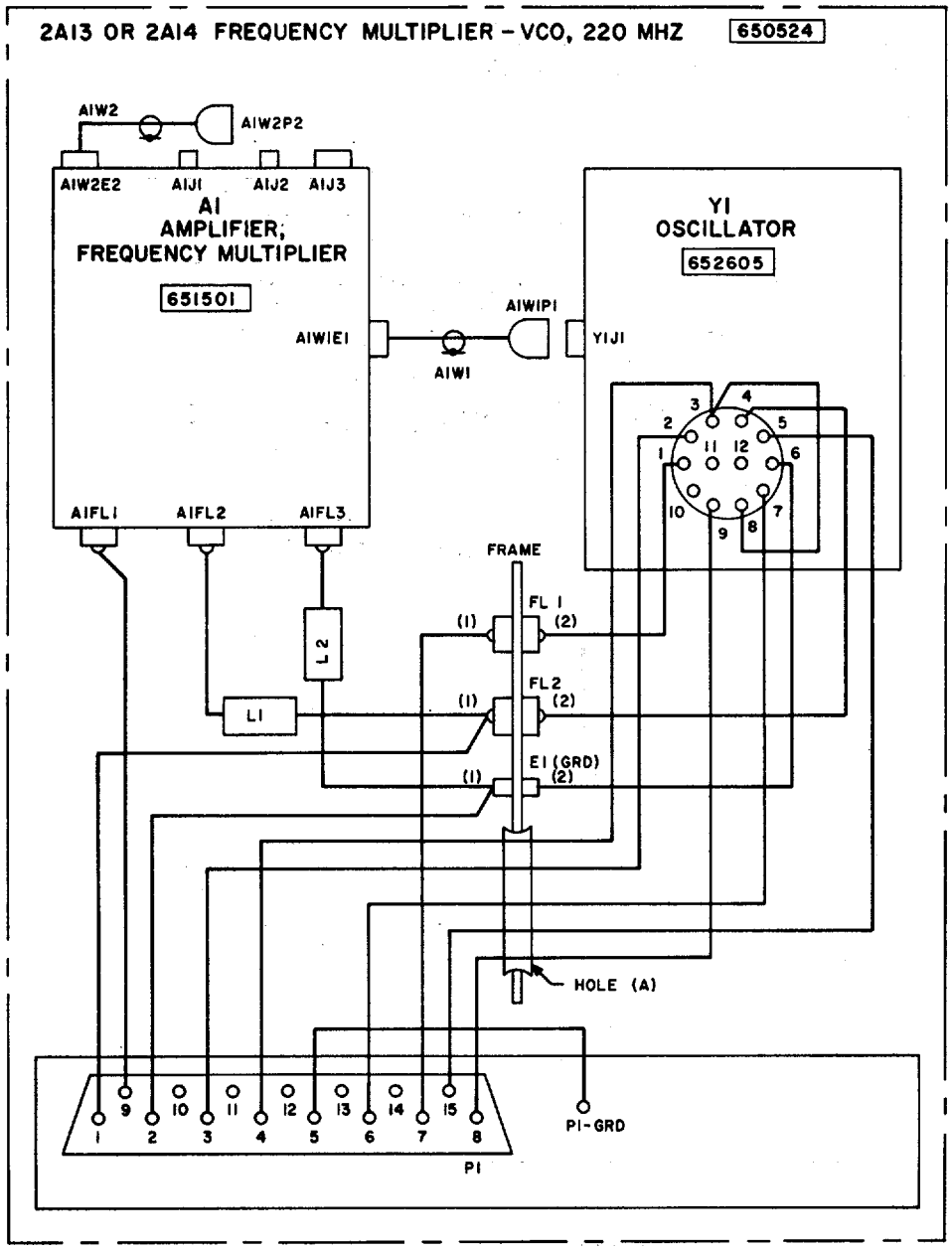
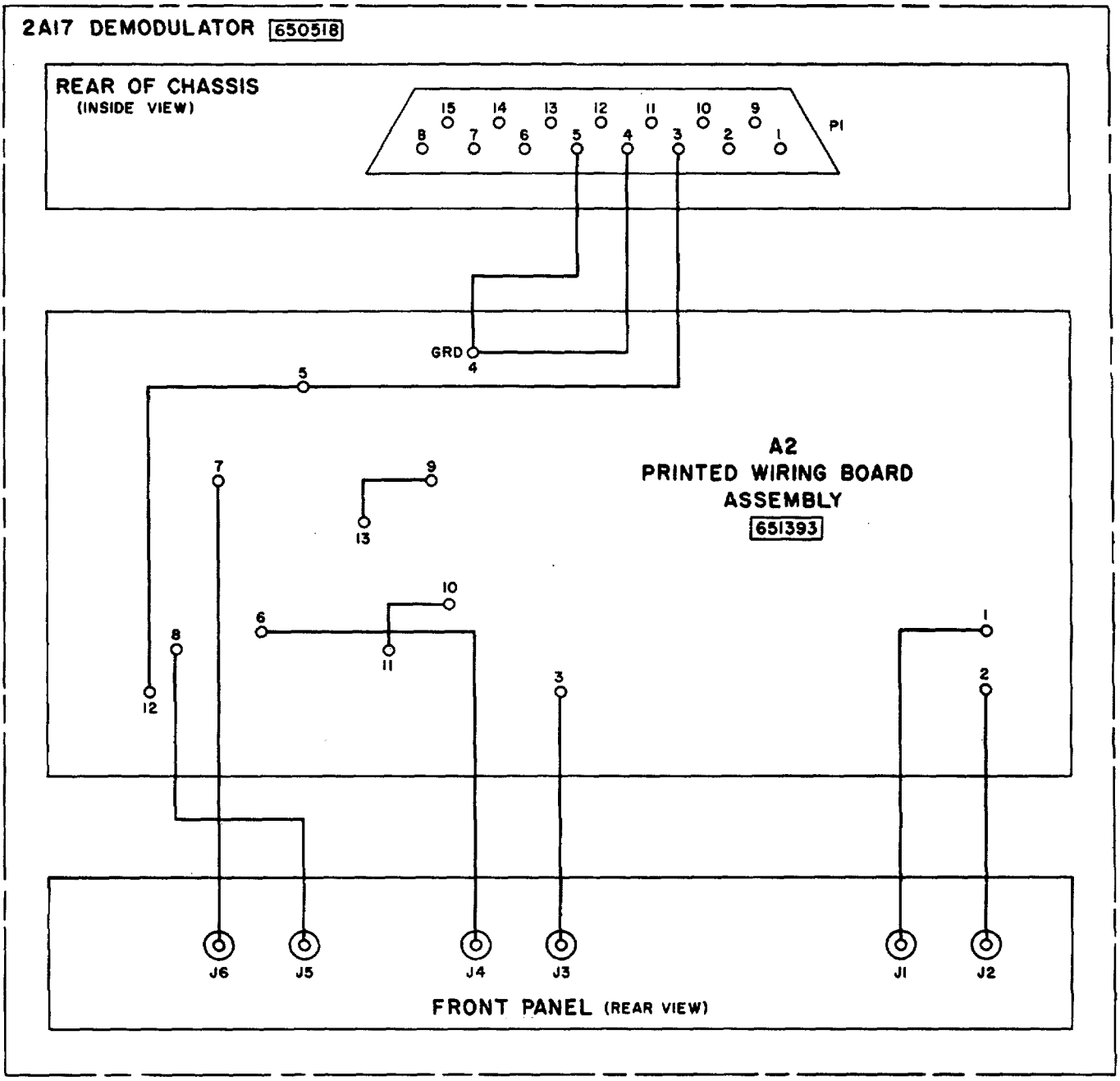


Figure 7-45. 20 MHz veo 2A11/2A14 assembly, wiring diagram.

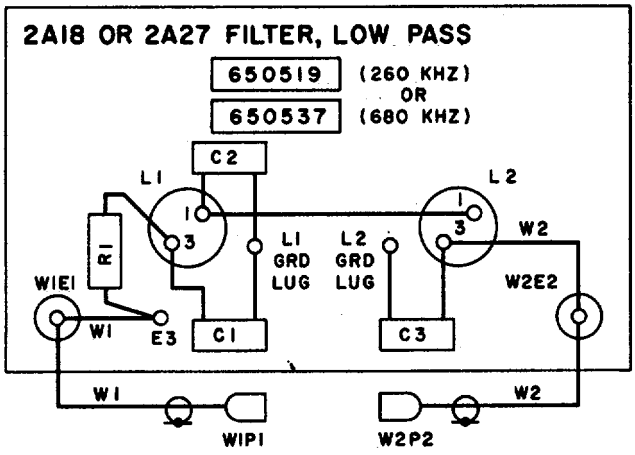


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL5820-595-35-121

Figure 7-46. Demodulator 2A17 assembly, wiring diagram

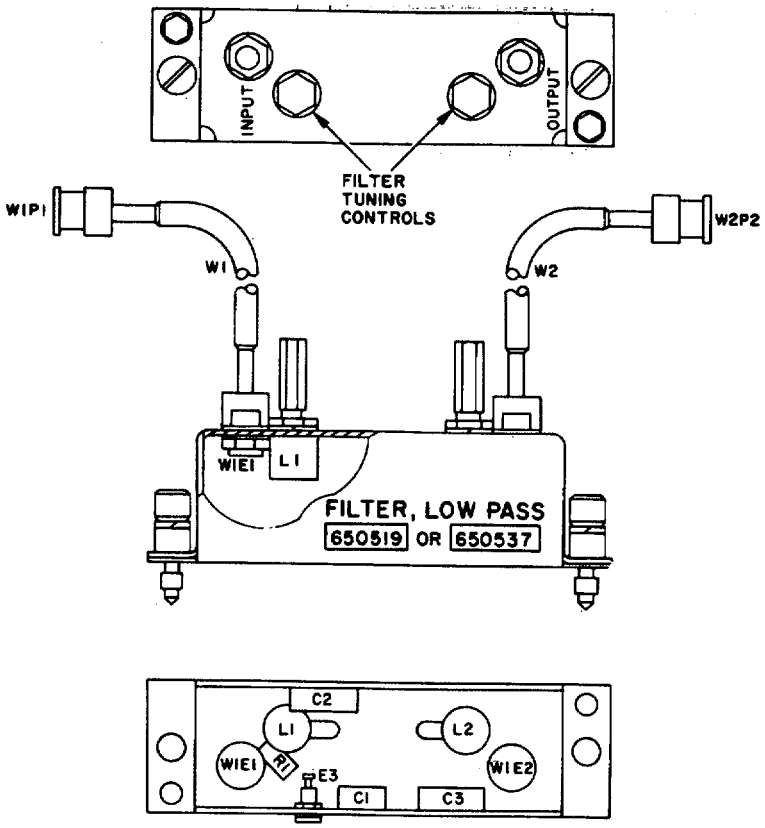


NOTES:

1. THIS DIAGRAM IS USED FOR BOTH FILTER ASSEMBLIES: 650519, 2A18 (B=260 KHZ)(FOR 12 CHANNEL OPERATION)AND 650537, 2A27 (B=680 KHZ)(FOR 24 CHANNEL OPERATION).
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
3. WIRING IS NO. 22 AWG STRANDED WIRE, TEFLON INSULATED, EXCEPT CABLES W1 & W2.

EL5820-595-35-122

Figure 7-47. 260 kHz low pass filter zA18/2A27, wiring diagram.

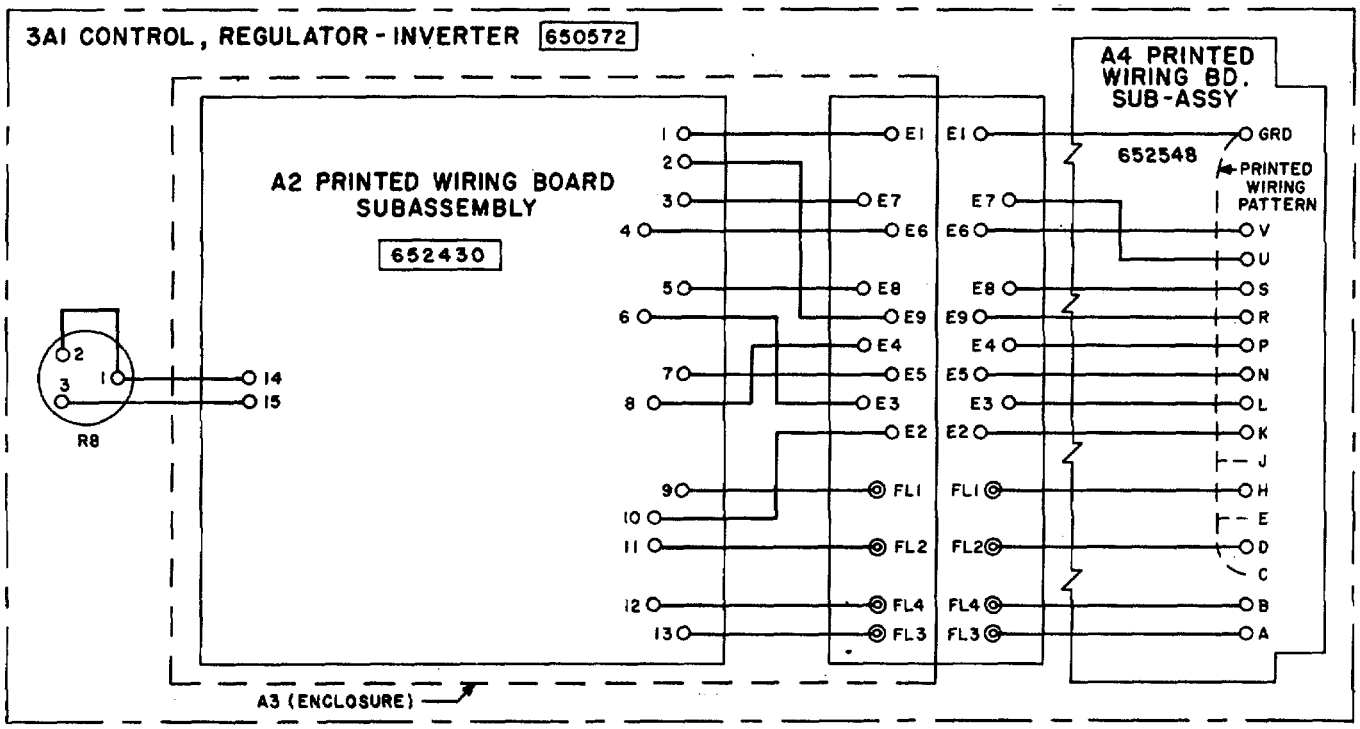


NOTES:

1. THIS DIAGRAM IS USED FOR FILTER ASSEMBLIES 650519 AND 650537.
   FILTER ASSEMBLY 650519 IS USED FOR 12 CHANNEL OPERATION.
   FILTER ASSEMBLY 650537 IS USED FOR 24 CHANNEL OPERATION.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
   FOR COMPLETE DESIGNATION, PREFIX WITH 2A18 OR 2A27.

EL5820-595-35-212

Figure 7-48. 260 kHz low pass filter 2A18/2A27, parts location diagram.

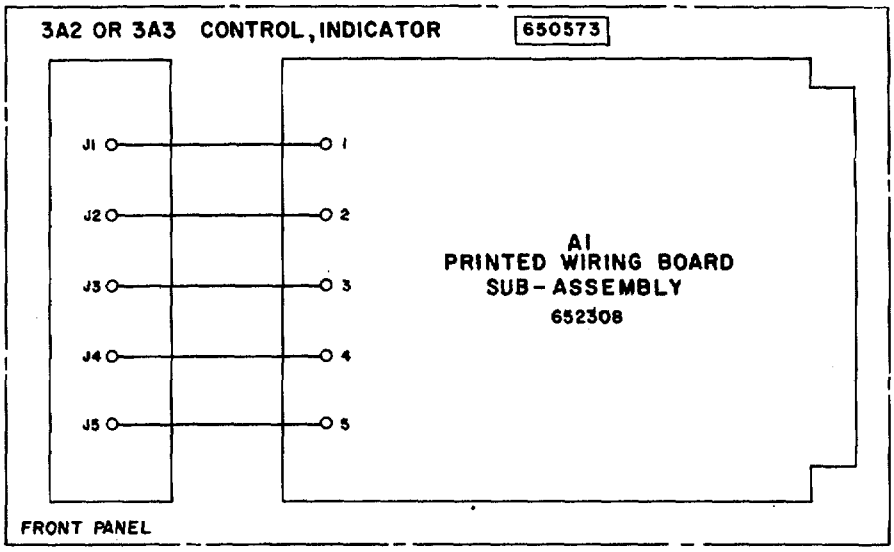


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL5820-595-35-12

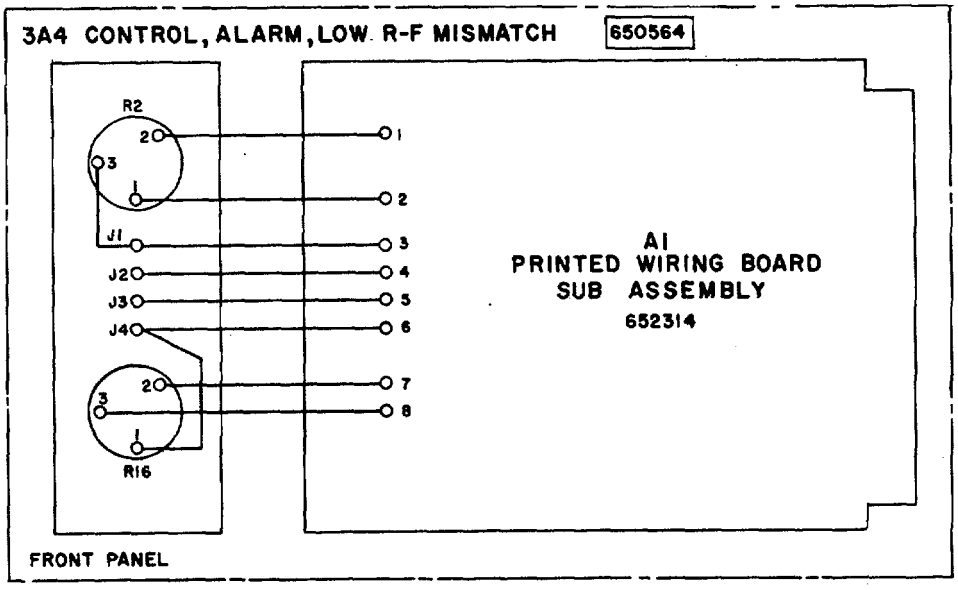
Figure 7-49. Inverter regulator control 3A1 assembly, wiring diagram.



NOTES:
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRING IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL5820-595-35-125

Figure 7-50. Indicator control 3A4 assembly, wiring diagram.



NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

EL5820-595-35-126

Figure 7-51. Low RF-mismatch, alarm and control 3A4 assembly, wiring diagram.

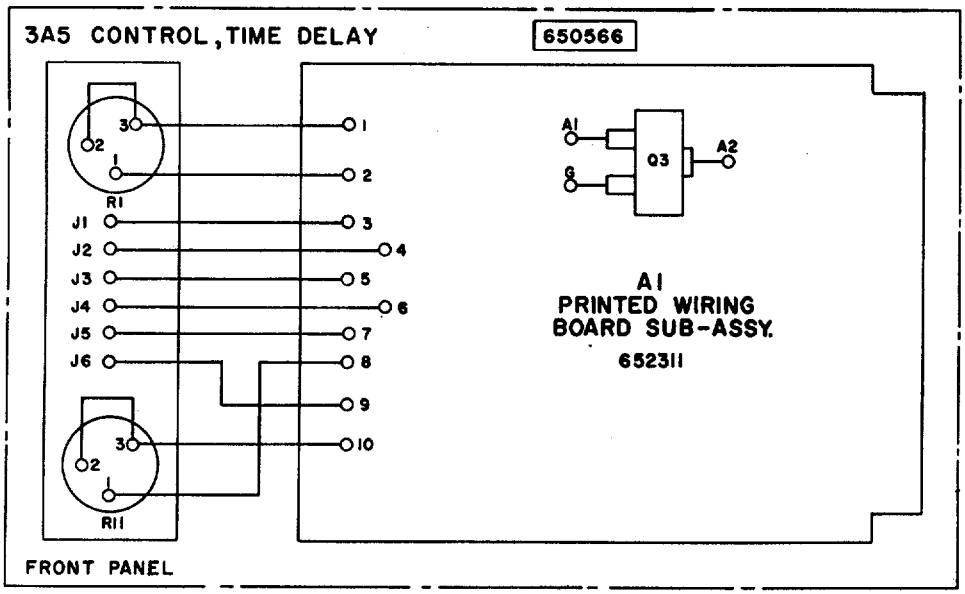


Figure 7-52. Time delay control 3A5 assembly, wiring diagram.

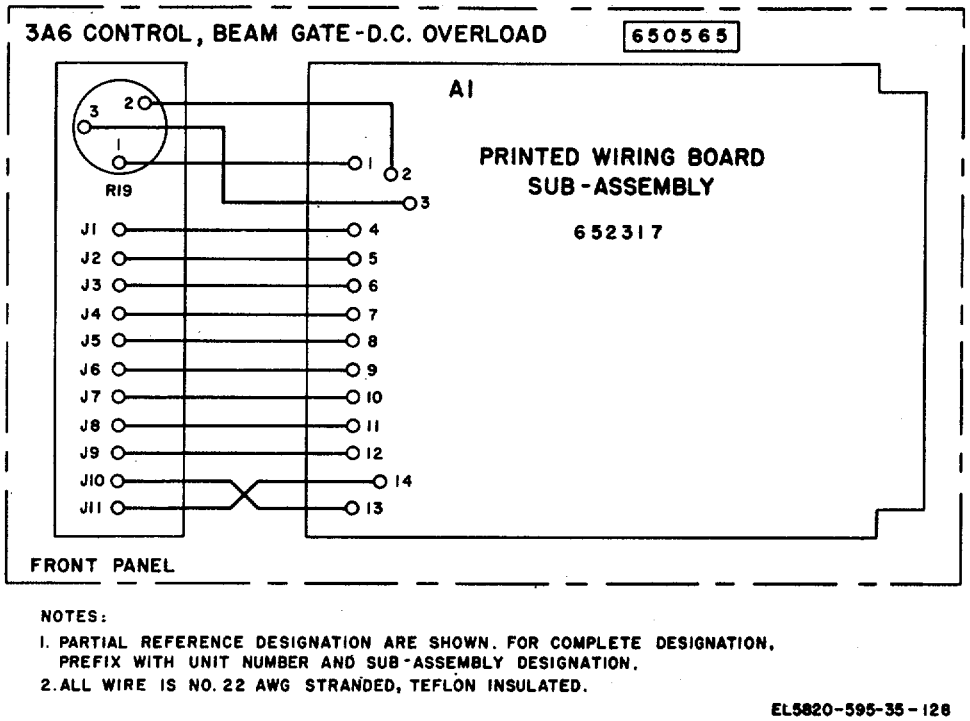


Figure 7-53. Beam gate-dc overload control 3A6 assembly, wiring diagram.

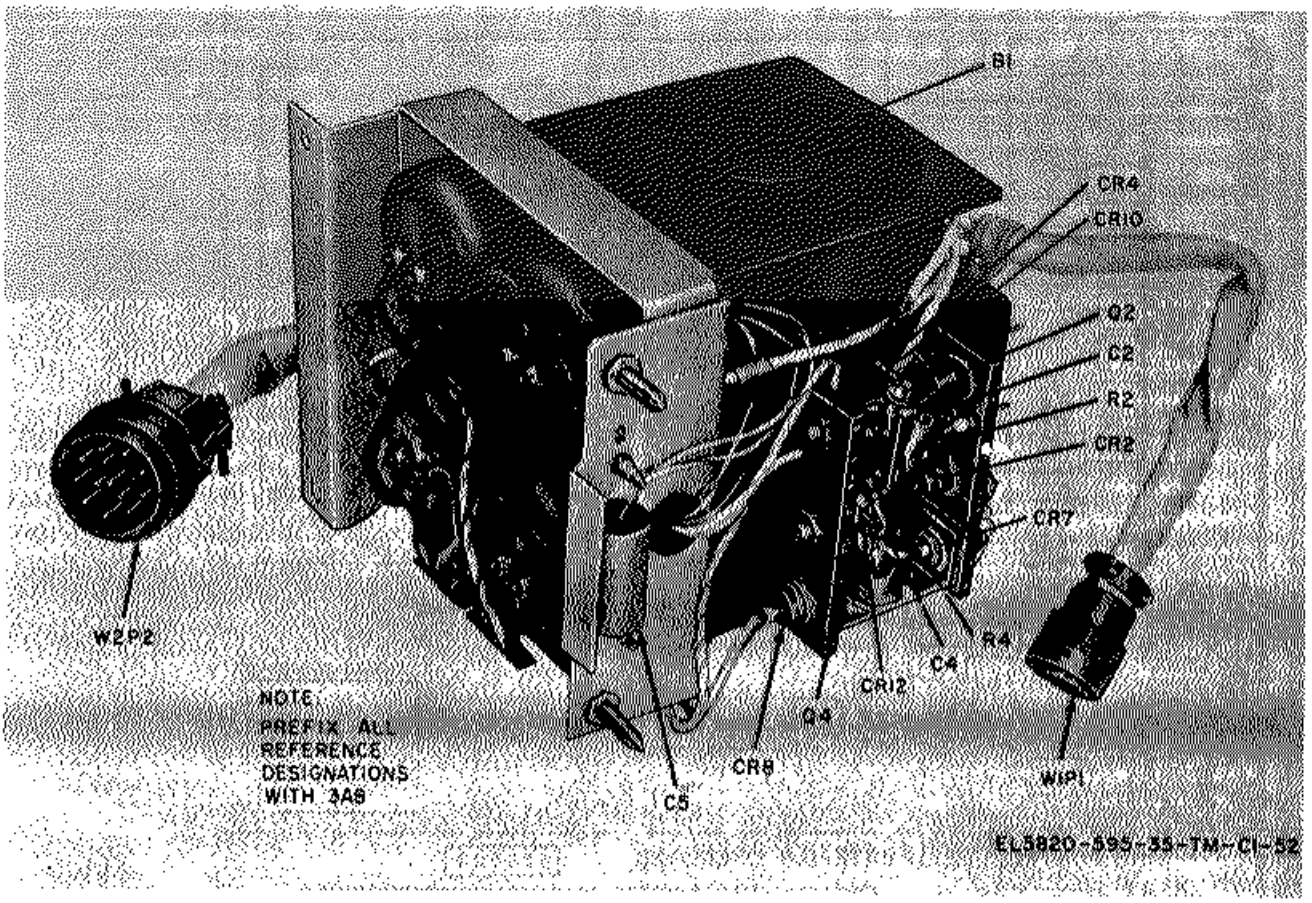


Figure 7-54. Inverter 3A8, rear oblique view, parts location diagram.

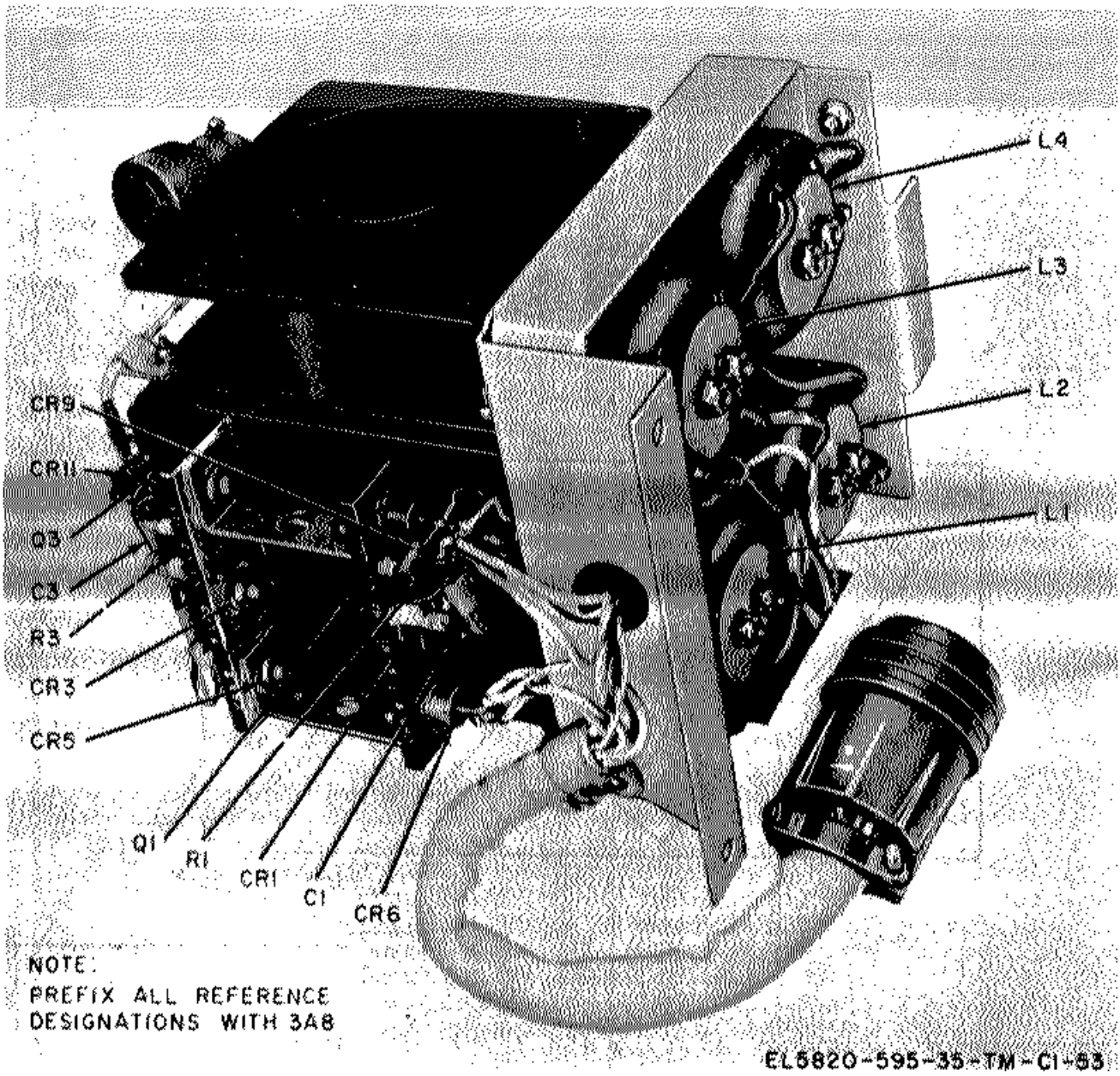


Figure 7-55. Inverter 3A8, front oblique view, parts location diagram.

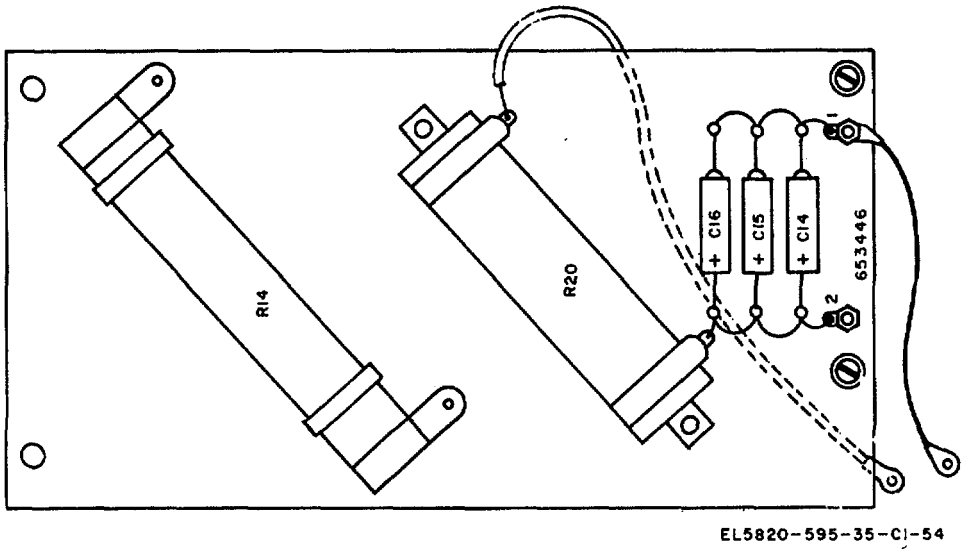
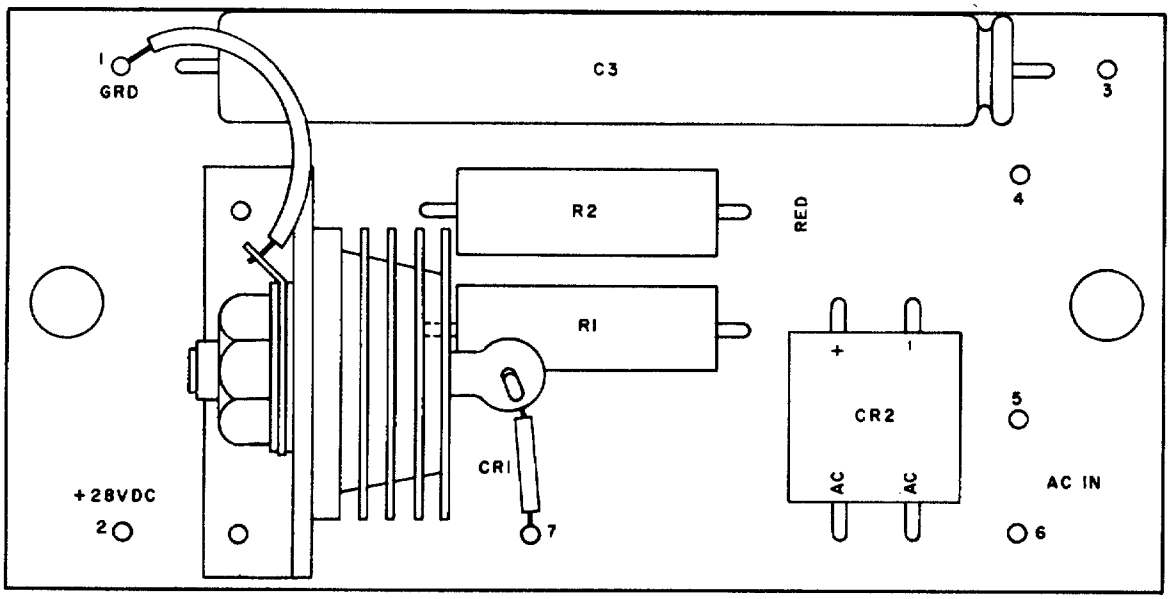
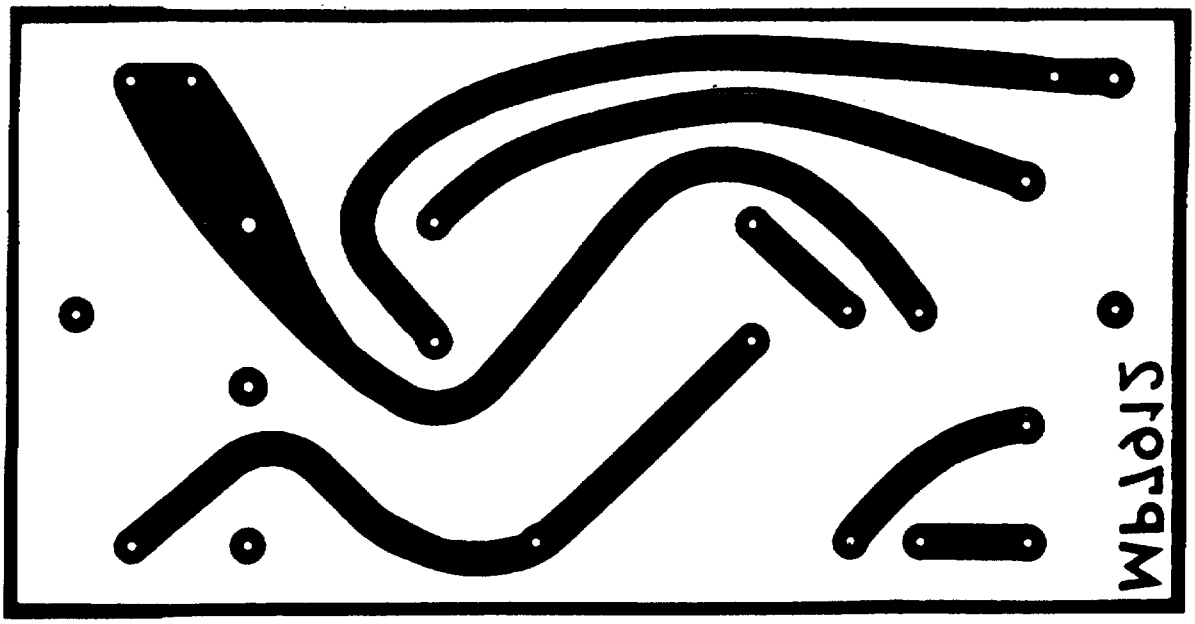


Figure 7-56. Component board assembly 3A9A33A1, parts location and printed wiring diagram.



A. PARTS ON FRONT OF BOARD 3A9A21 (652382).



B. WIRING ON BACK OF BOARD 3A9A21 (VIEWED THROUGH FRONT).

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 3A9A21.

EL5820-595-35-225

Figure 7-57. Rectifier assembly SA9A21, parts location and printed wiring diagram.

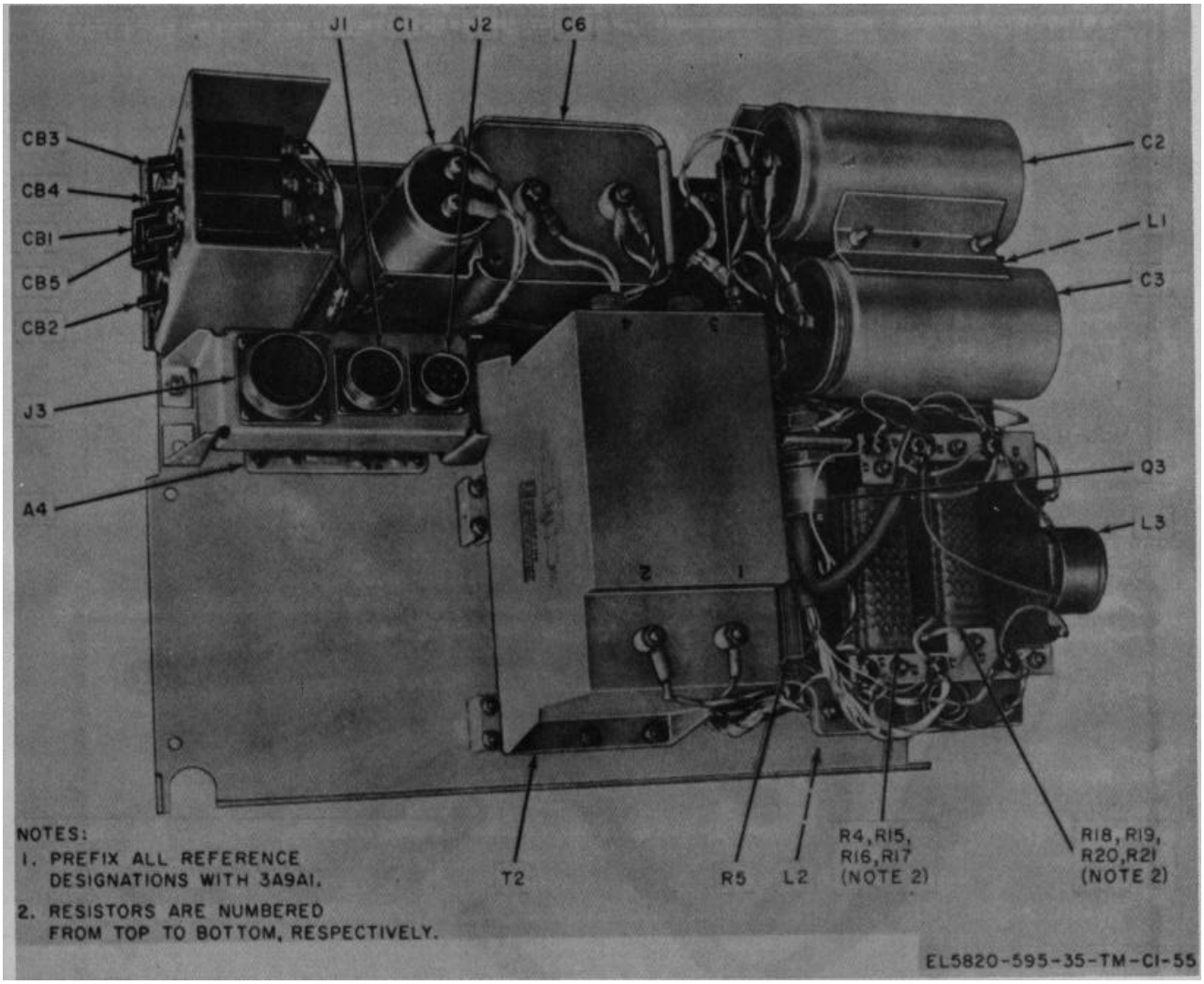


Figure 7-58. Hv power supply 3A9A1, top view, parts location.

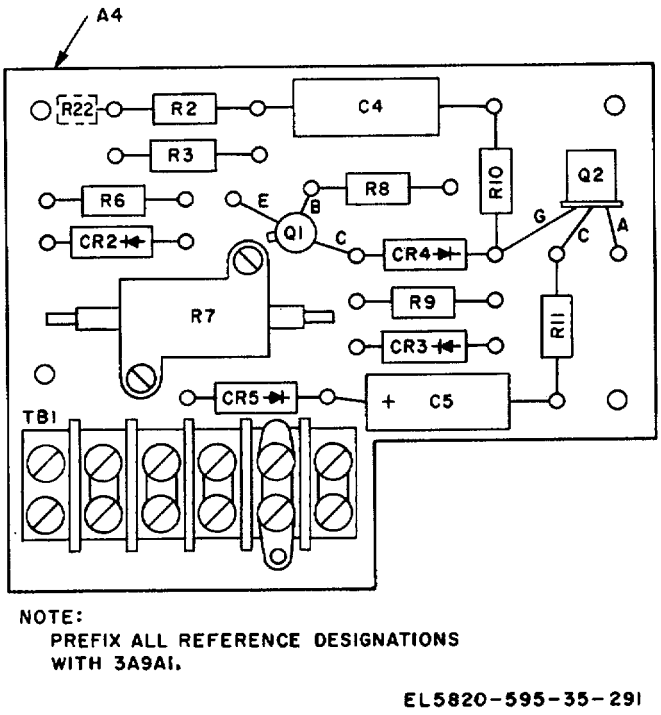


Figure 7-59. Subassembly 3A9AIA4, top view, parts location.

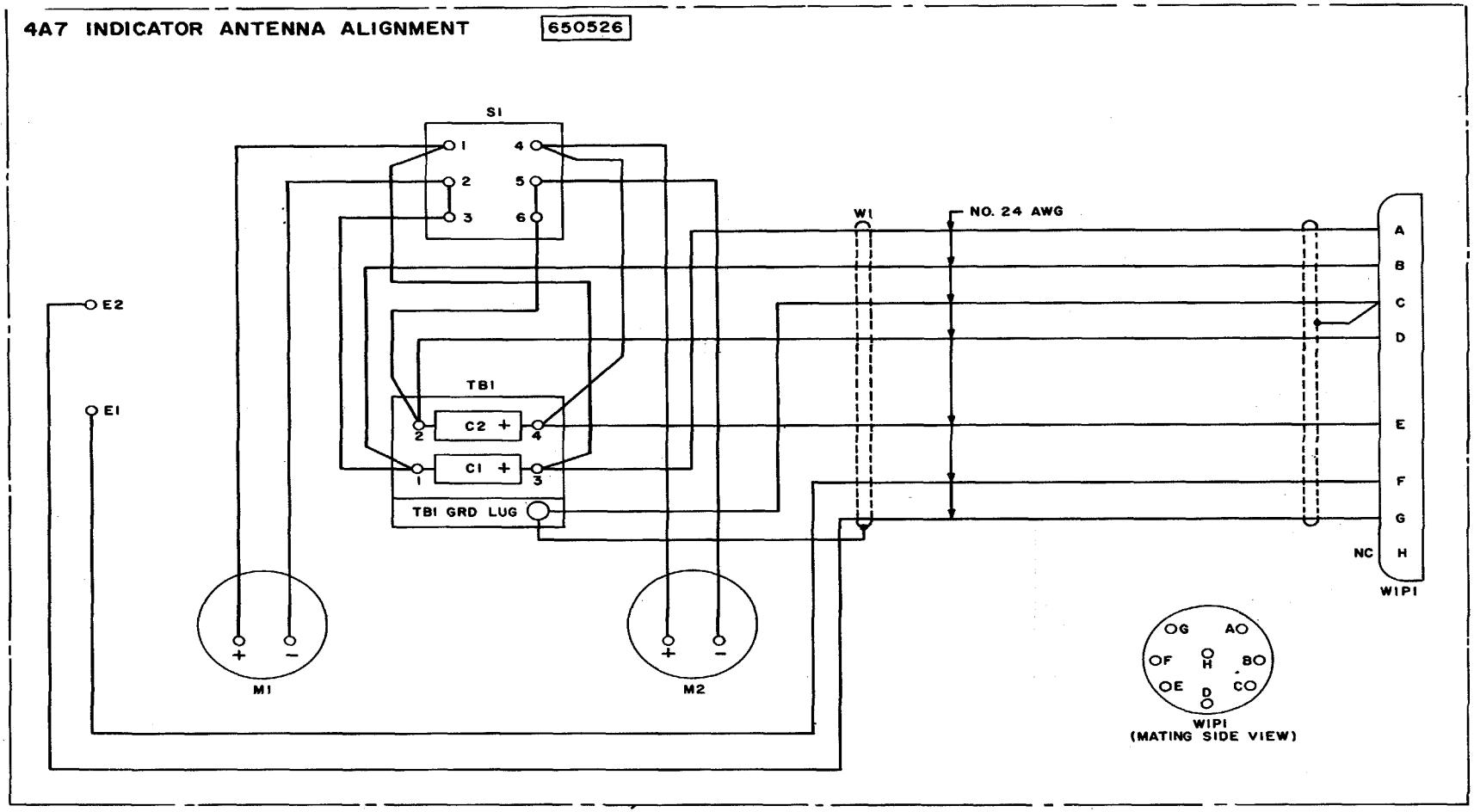


Figure 7-60. Antenna alignment indicator 4A7 assembly, wiring diagram.

CHAPTER 8

FOLDOUT ILLUSTRATIONS

8-1. General

All foldout illustrations referenced in chapters 1 through 7 are located at the end of this manual. Color code marking illustrations, block diagrams, schematics, timing diagrams, interconnecting diagrams, wiring diagrams, and parts location diagrams are included in the group.

8-2. Radio Set Illustrations

The overall block diagram for the radio set is shown in figure 8-3. The schematic for the radio set consists of interconnecting diagrams, supported by supplementary diagrams for each major component of the radio set (transmitter, receiver, and power amplifier).

8-3. Transmitter Foldout Illustrations

a. Block Diagrams. Figures 8-4 through 8-13 and figure 8-15.

b. Interconnecting Diagrams and Schematics. Figure 8-14, figures 8-16 through 8-47, and figure 8-49.

c. Timing Diagram. Figure 8-48.

d. Wiring Diagrams and Parts Location Diagrams. Figures 8-74 through 8-102.

8-4. Receiver Foldout Illustrations

a. Block Diagrams. Figures 8-50 through 8-58.

b. Interconnecting Diagrams and Schematics Figures 8-59 through 8-66.

c. Wiring Diagrams and Parts Location Diagrams. Figures 8-103 through 8-115.

8-5. Power Amplifier Foldout Illustrations

a. Block Diagrams. Figures 8-67 and 868.

b. Interconnecting Diagrams and Schematics. Figures 8-69 through 8-124.

c. Wiring Diagrams and Parts Location Diagrams. Figures 8-116 through 8-124.

APPENDIX

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DA Pam 310-7	Index of Modification Work Orders.
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TM 11-5820-595-12	Operator and Organizational Maintenance Manual for Radio Set AN/GRC-143, including Repair Parts and Special Tools List.
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By Order of the Secretary of the Army:

W. C. WESTMORELAND
General, United States Army,
Chief of Staff.

Official:

VERNE L. BOWERS,-
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The Adjutant General.

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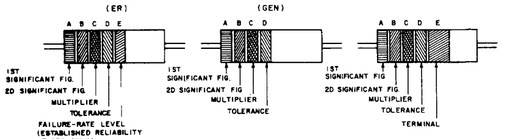


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE 1
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M	
BROWN	1	BROWN	1	BROWN	10			RED	P	
RED	2	RED	2	RED	100			ORANGE	R	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY).			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	1.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL. ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

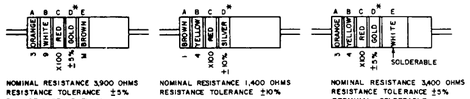
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

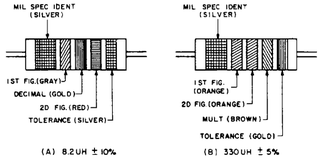
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES, AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

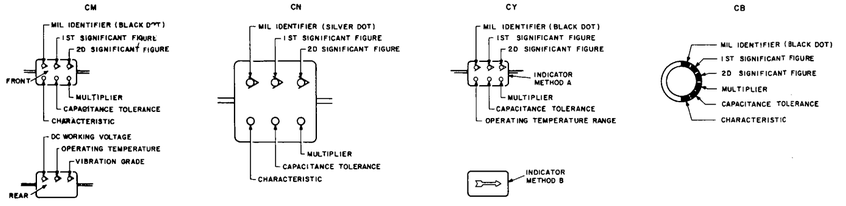
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

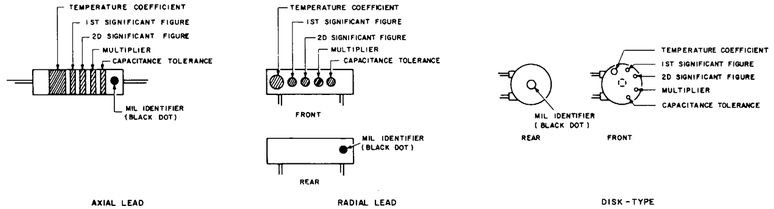
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.





C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

T/TABLE 3 - FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE			CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CN	CB	CM	CY, CM	CN
BLACK	CM, CY, CB	0	0	1			±20%	±20%		A			10-55 Hz
BROWN		1	1	10					B	E	B		
RED		2	2	100	±2%		±2%	±2%	C			-55°TO+70°C	
ORANGE		3	3	1,000		±30%			D		D	300	
YELLOW		4	4	10,000					E			-55°TO+125°C	10-2,000Hz
GREEN		5	5		±5%				F			500	
BLUE		6	6									-55°TO+150°C	
PURPLE (VIOLET)		7	7										
GREY		8	8										
WHITE		9	9										
GOLD				0.1			±5%	±5%					
SILVER	CN				±10%	±30%	±10%	±10%					

T/TABEL 4 - TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	±10%		
GOLD	+100					±1.0 UUF	
SILVER			/				

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

ESC-FM 4113-89

Figure 8-1/8-2. Color code marking for MIL-STD resistors, inductors, and capacitors.

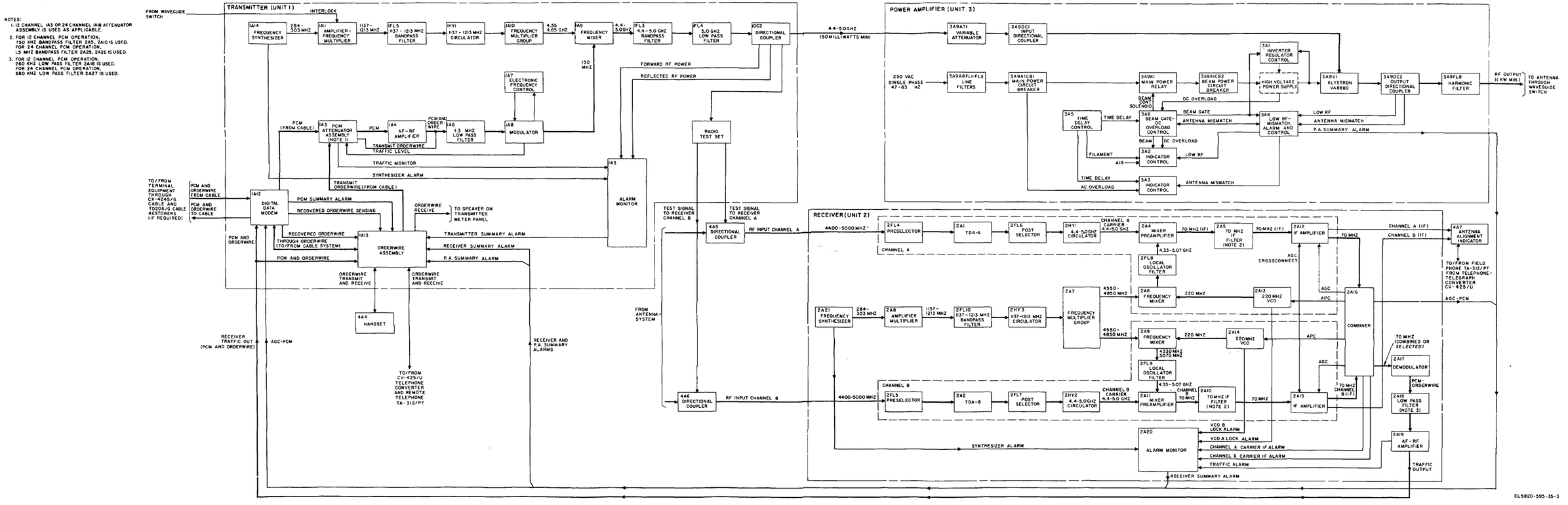


Figure 8-3. Radio Set AN/GRC-143 block diagram.

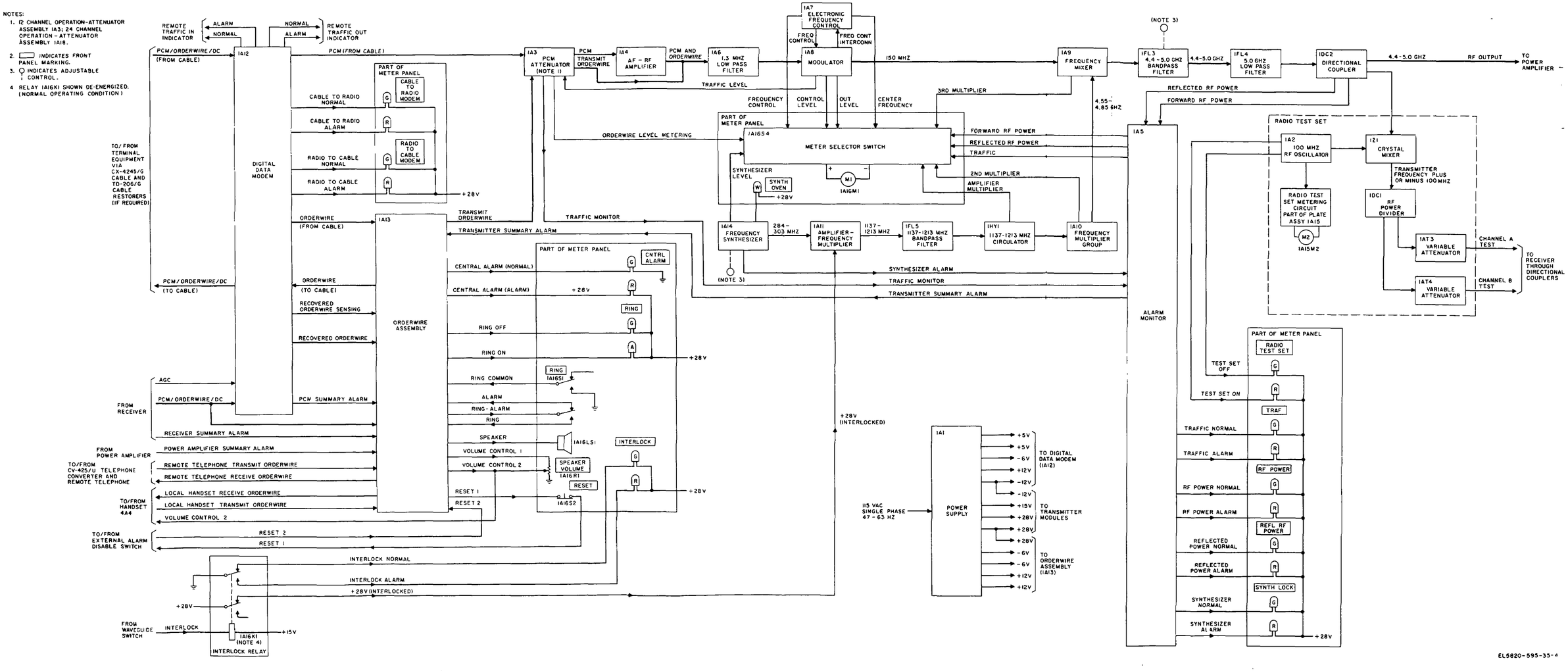


Figure 8-4. Transmitter block diagram.

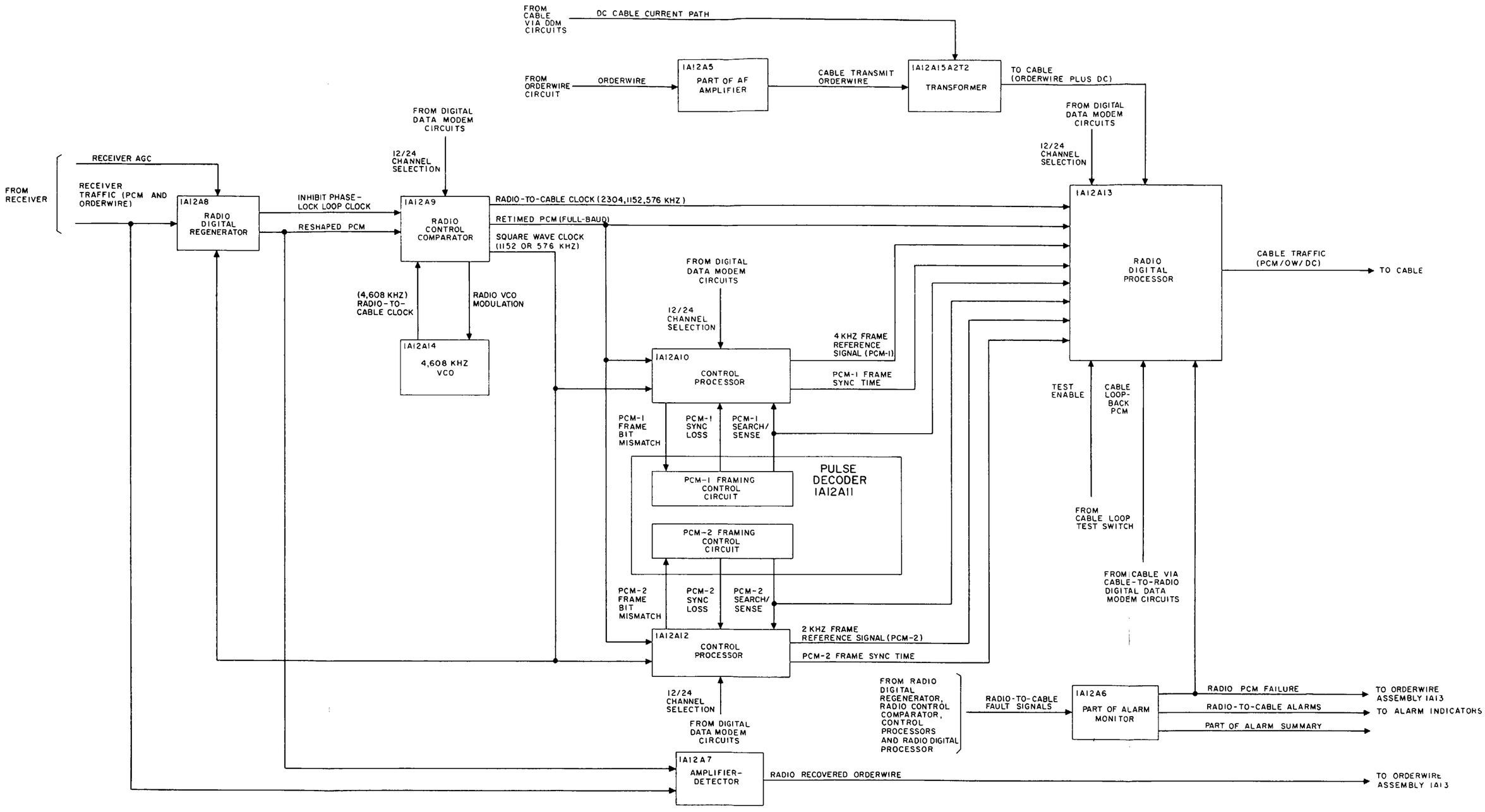


Figure 8-5. Digital data modem 1A12, radio-to-cable functional block diagram.

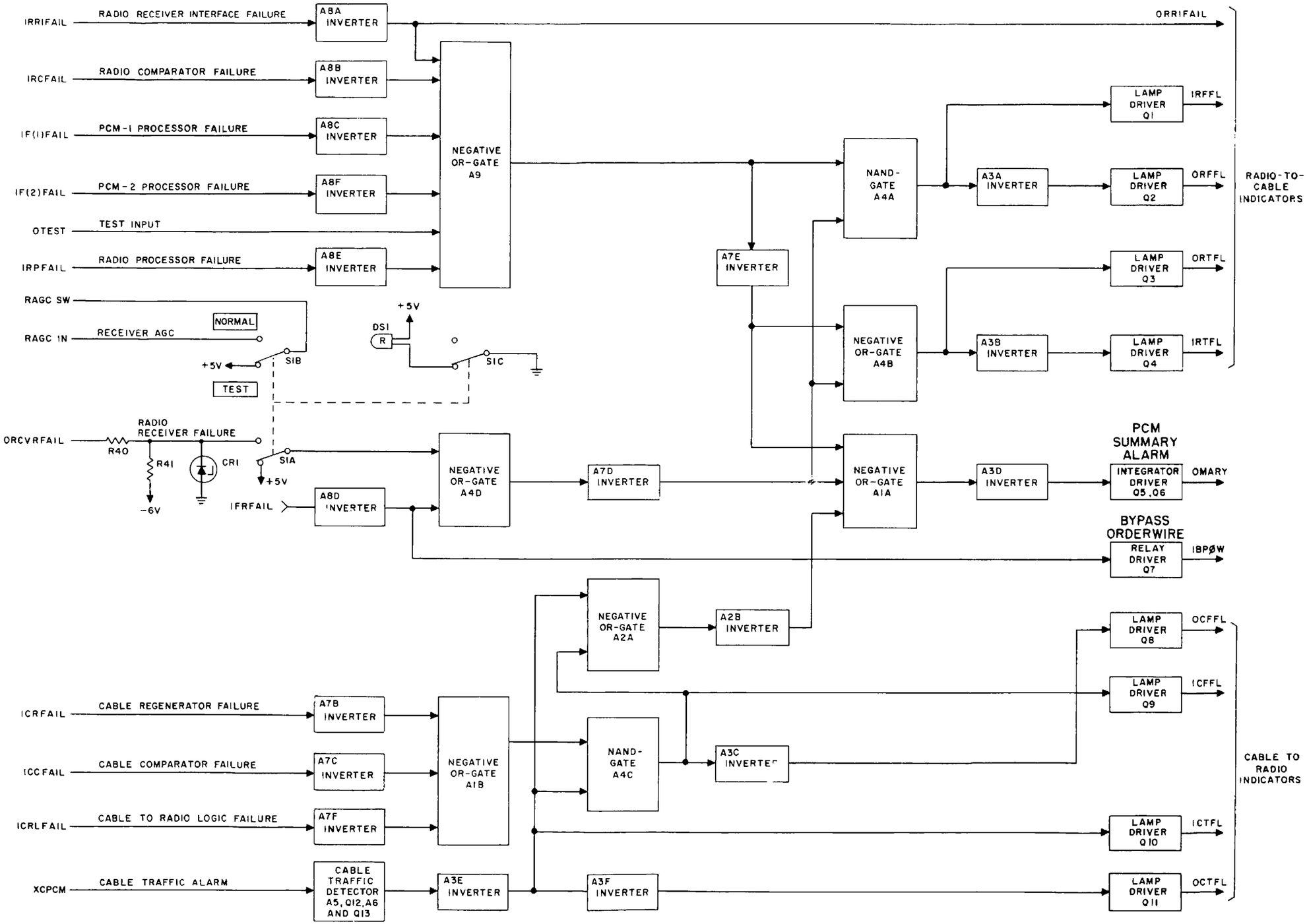


Figure 8-6. Alarm monitor 1A12A6, block diagram.

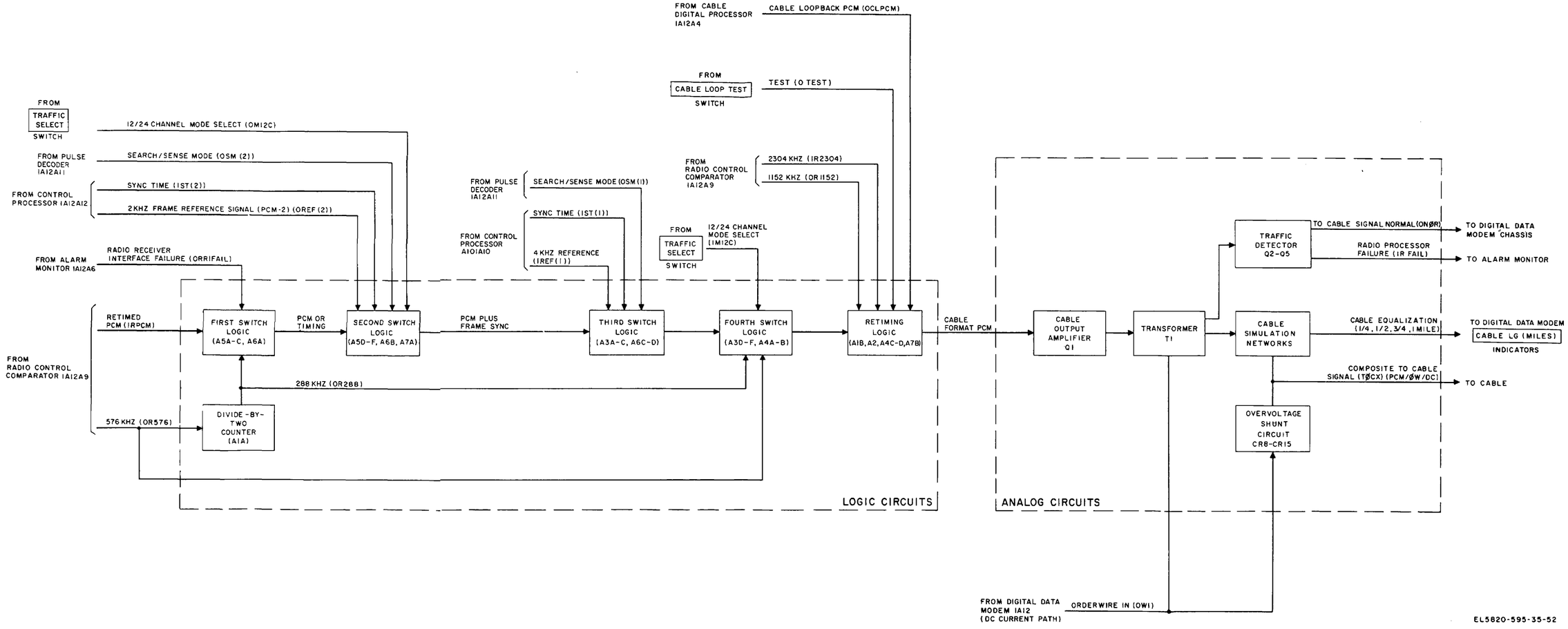


Figure 8-7. Radio digital processor 1A12A13, block diagram.

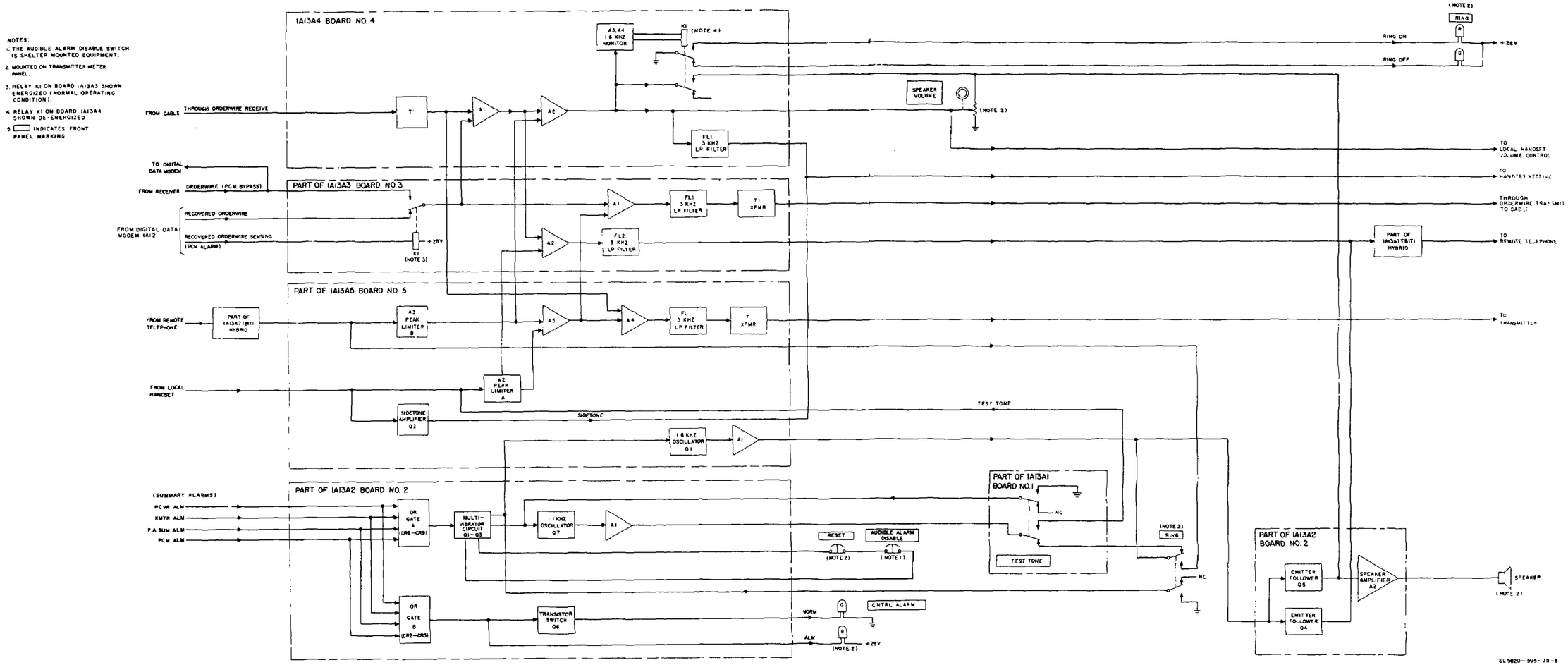


Figure 8-8. Orderwire assembly 1A13 signal distribution block diagram.

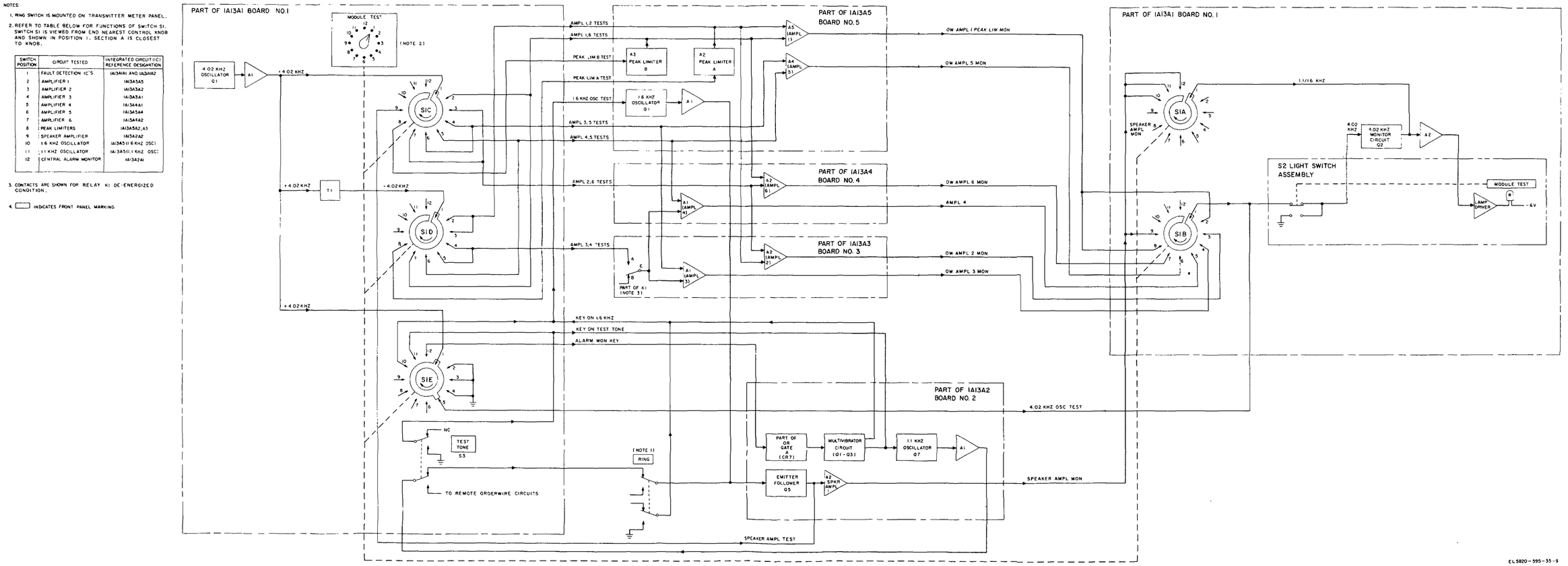


Figure 8-9. Orderwire assembly 1A13 fault detection block diagram.

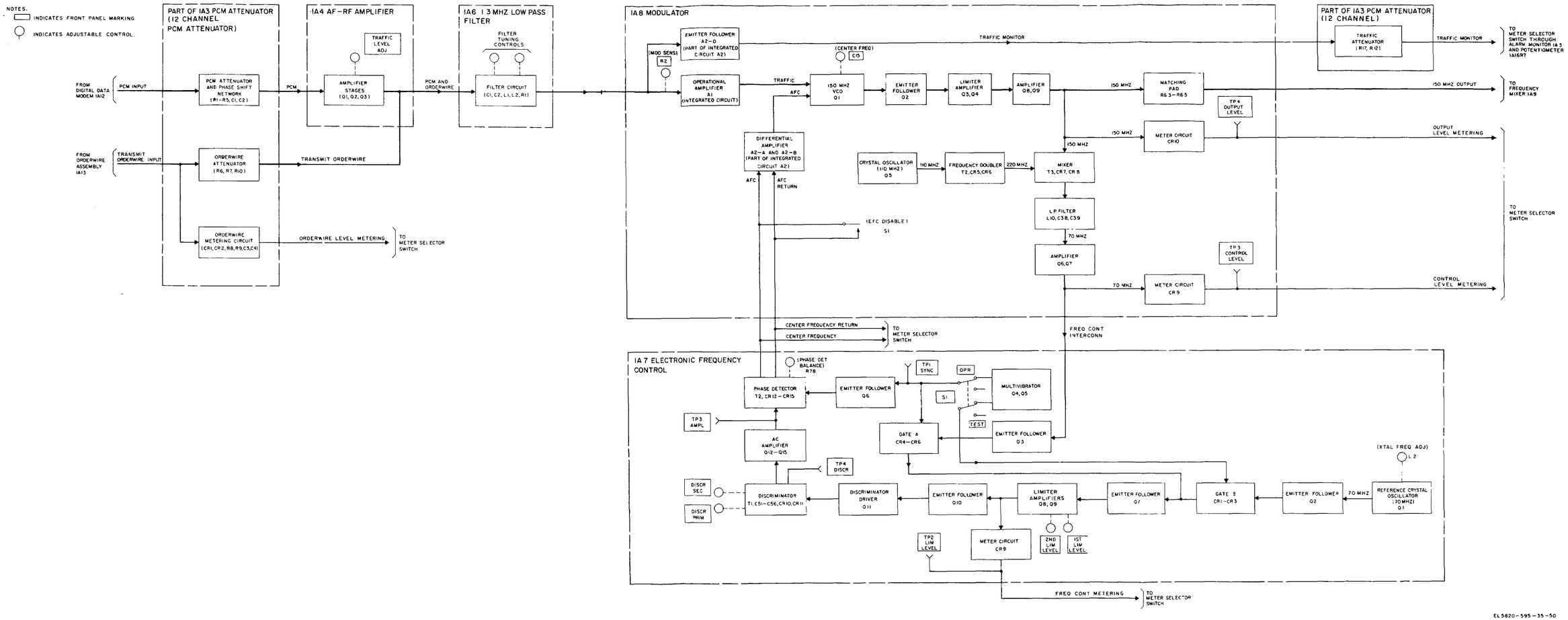


Figure 8-10. Transmitter modulator circuits, block diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A14 (TRANSMITTER) OR 2A21 (RECEIVER).
2. THE SYNTH OUTPUT IS SENT TO AMPLIFIER-MULTIPLIER 2A8 IN THE RECEIVER.
3. THE SYNTH ALARM IS SENT TO ALARM MONITOR 2A20 IN THE RECEIVER.

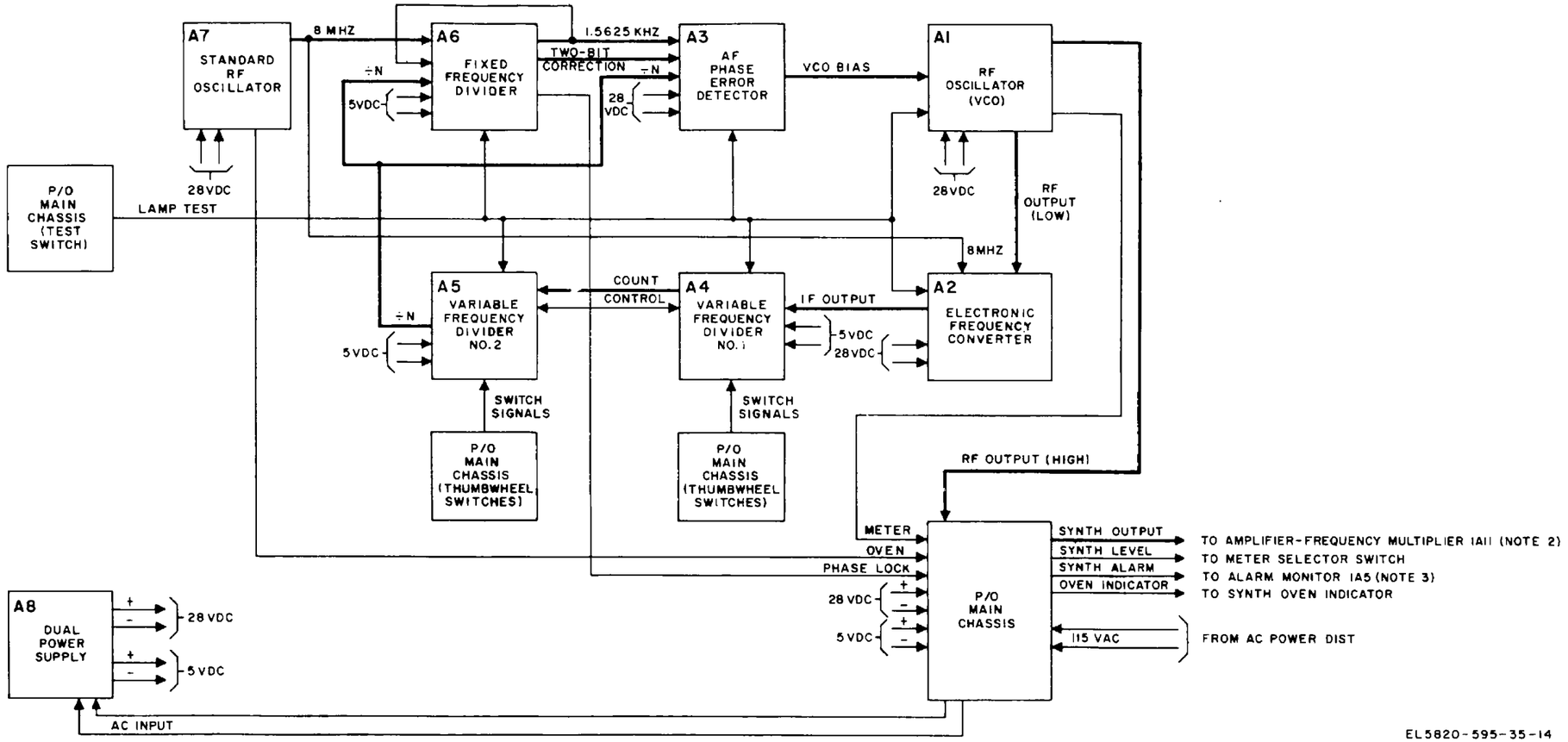


Figure 8-11. Frequency synthesizer 1A14/2A21, block diagram.

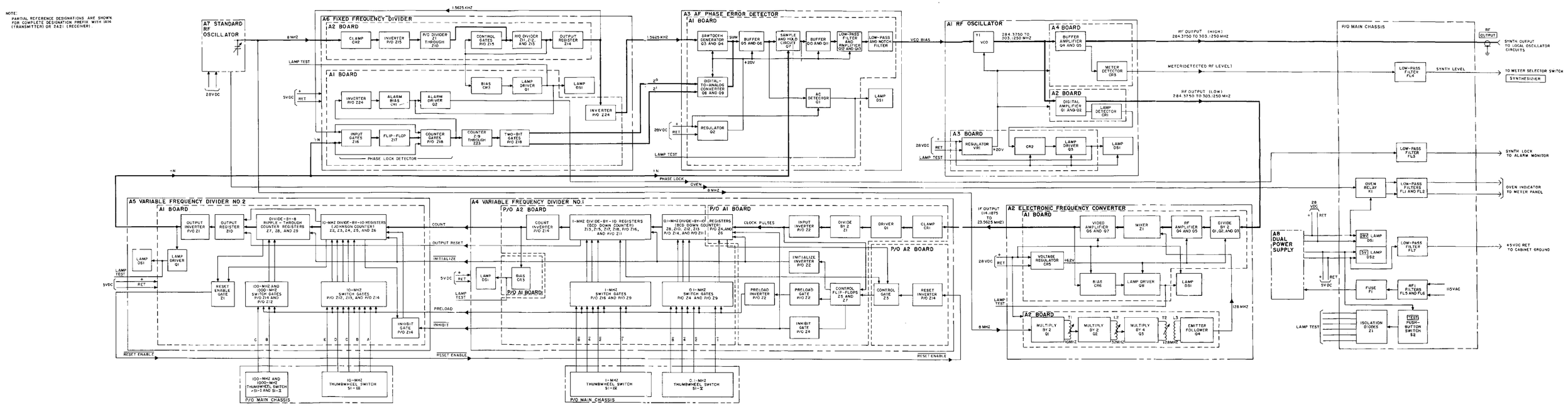


Figure 8-12. Frequency synthesizer 1A14/2A21, module, block diagram

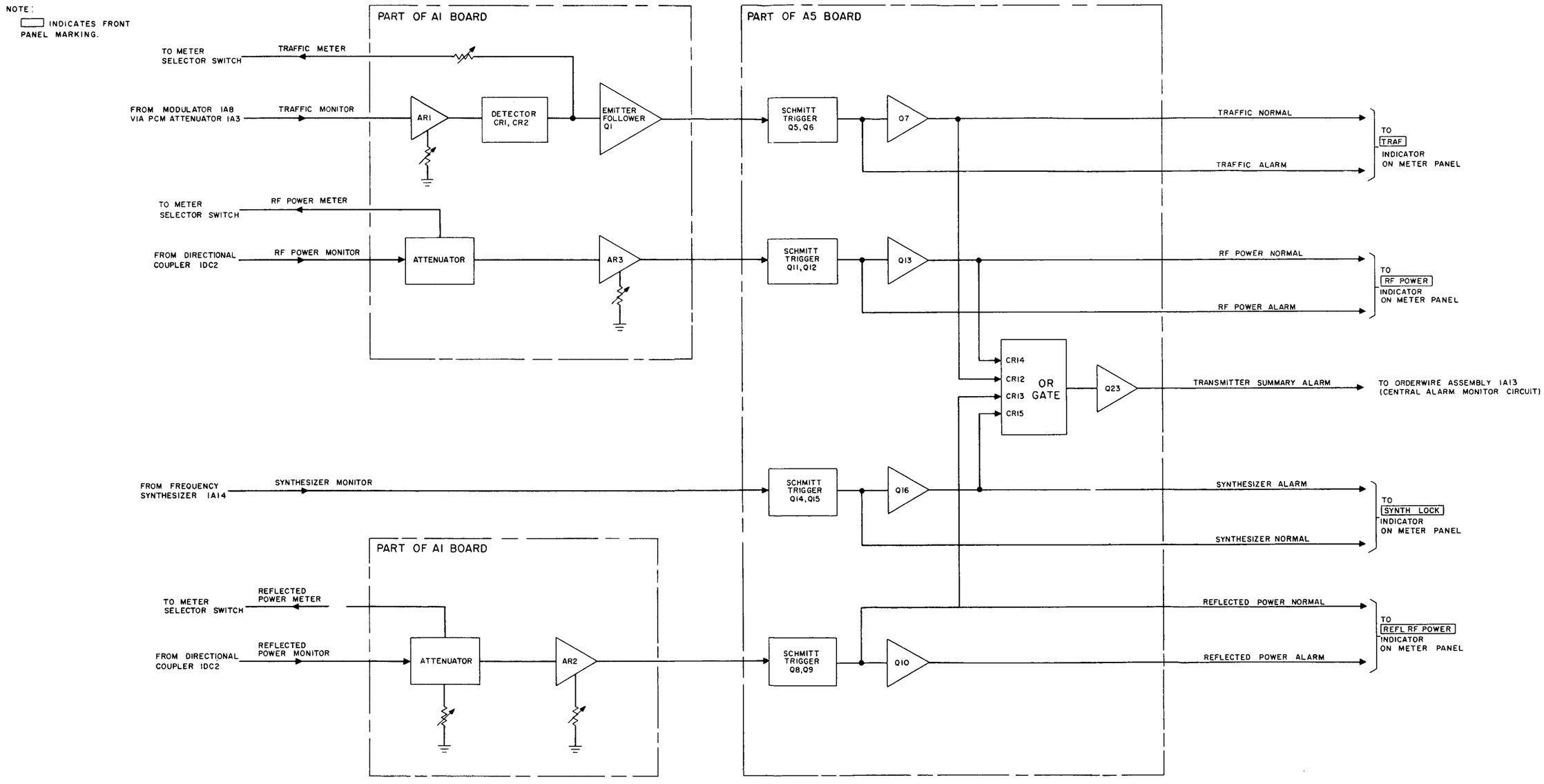


Figure 8-13. Alarm monitor 1A5, block diagram

UNIT 1, TRANSMITTER, RADIO T-961/GRC-143

NOTES.

1. UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS
2. REFERENCE DESIGNATIONS OF ASSEMBLIES THAT ARE NOT PHYSICALLY SHOWN ON DIAGRAM.
   1A15 - PLATE ASSEMBLY
   1A16 - CABINET, ELECTRICAL EQUIPMENT
   1A15W1 - WIRING HARNESS, BRANCHED (PLATE ASSY)
   1A16W18 - WIRING HARNESS, BRANCHED (AC WIRING BETWEEN 1A16T1 AND 1A16W18XA1)
   1A16W19 - WIRING HARNESS, BRANCHED (CABINET, MAIN WIRING HARNESS).
3. TERMINALS INDICATED ARE USED FOR INTERNAL MODULE CONNECTIONS. DO NOT CONNECT EXTERNALLY.
4. UNLESS OTHERWISE SPECIFIED, ALL WIRE SHALL BE STRANDED, TEFLON INSULATED, SIZES AS FOLLOWS:
   NO. 16 AWG - FOR 115V AC POWER
   NO. 20 AWG - FOR LOW VOLTAGE AC AND DC AND GROUND.
   NO. 22 AWG - FOR ALL OTHER WIRING
5. CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN IN TABLE I. PINS A1, A2, A3 ARE FOR COAX CONTACTS.
6. THE SYMBOL ◄P DENOTES TWISTED PAIR.
7. RELAY 1A16K1 IS SHOWN IN THE DE-ENERGISED STATE.
8. SWITCH 1A16S4 IS VIEWED FROM END OPPOSITE CONTROL KNOB. SECTION A IS CLOSEST TO KNOB.
9. CONTROL, INDICATOR, AND SWITCH OUTLINES SHOWING TERMINAL LOCATION ARE PROVIDED BELOW. ALL VIEWS ARE FROM WIRING SIDE.

TABLE I
CONNECTOR PIN ARRANGEMENTS (MATING SIDE VIEW)

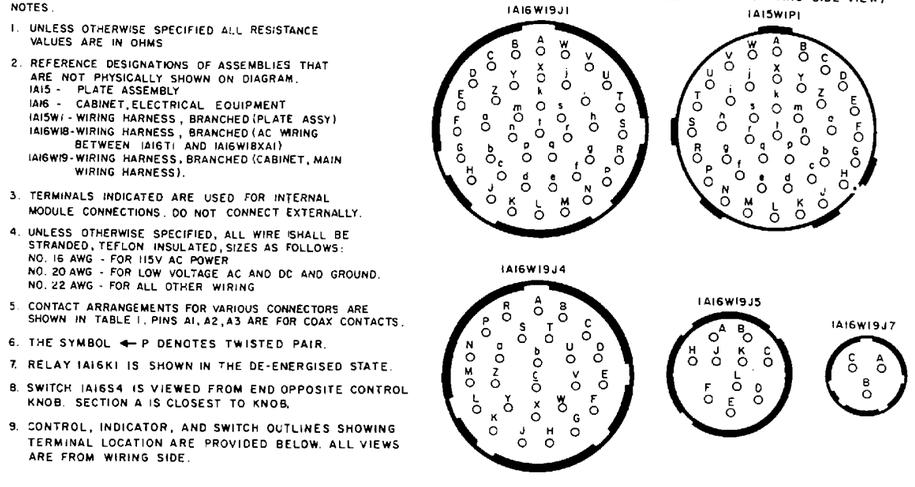


Figure 8-14 (1) Transmitter (unit 1), interconnecting diagram (part 1 of 3

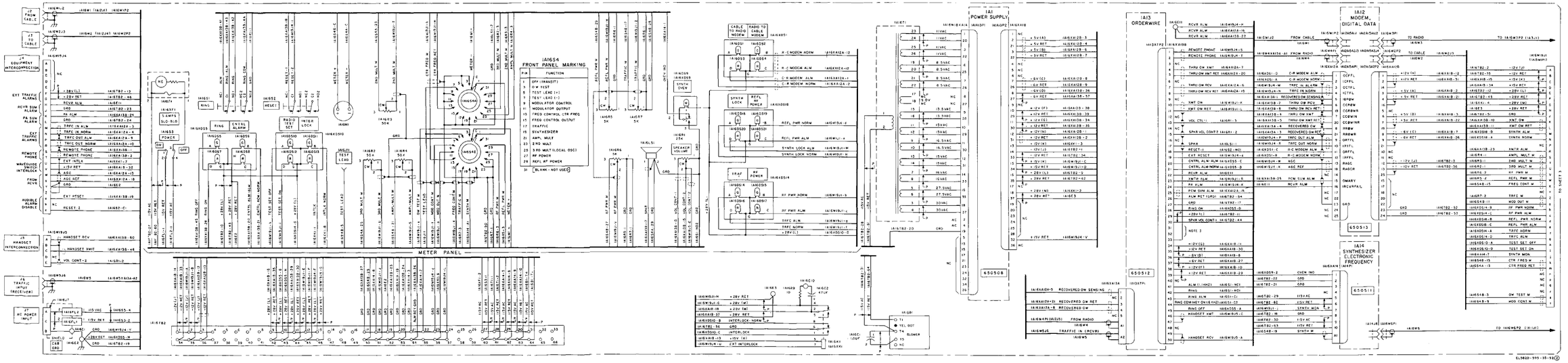


Figure 8-14 (2) Transmitter (unit 1), interconnecting diagram (part 2 of 3

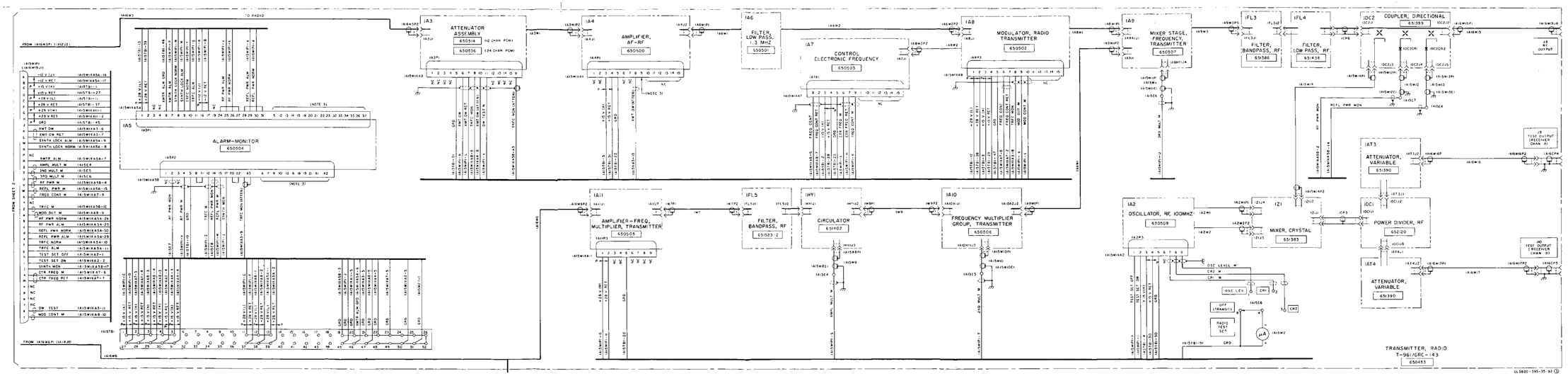


Figure 8-14 (3) Transmitter (unit 1), interconnecting diagram (part 3 of 3)

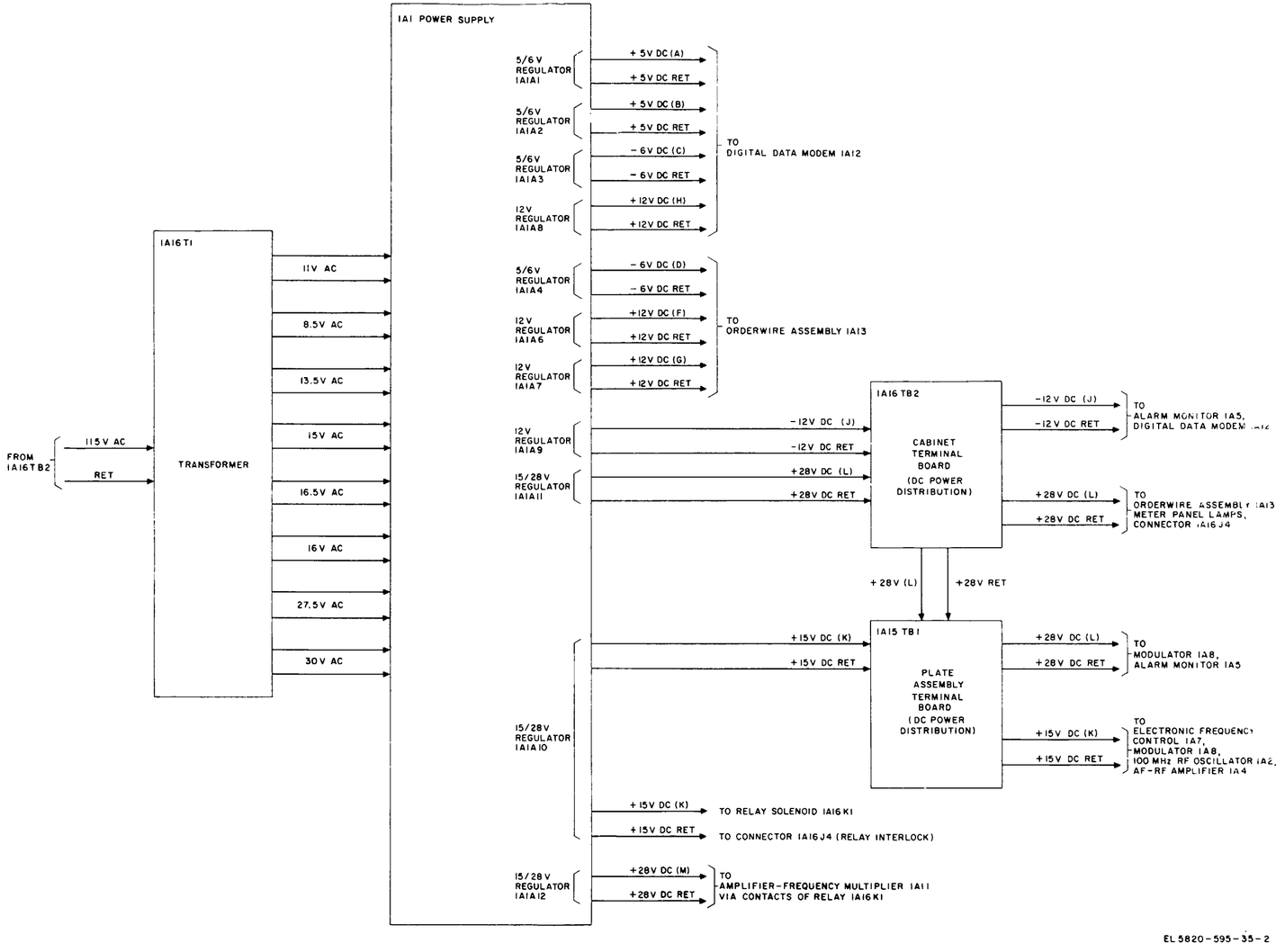
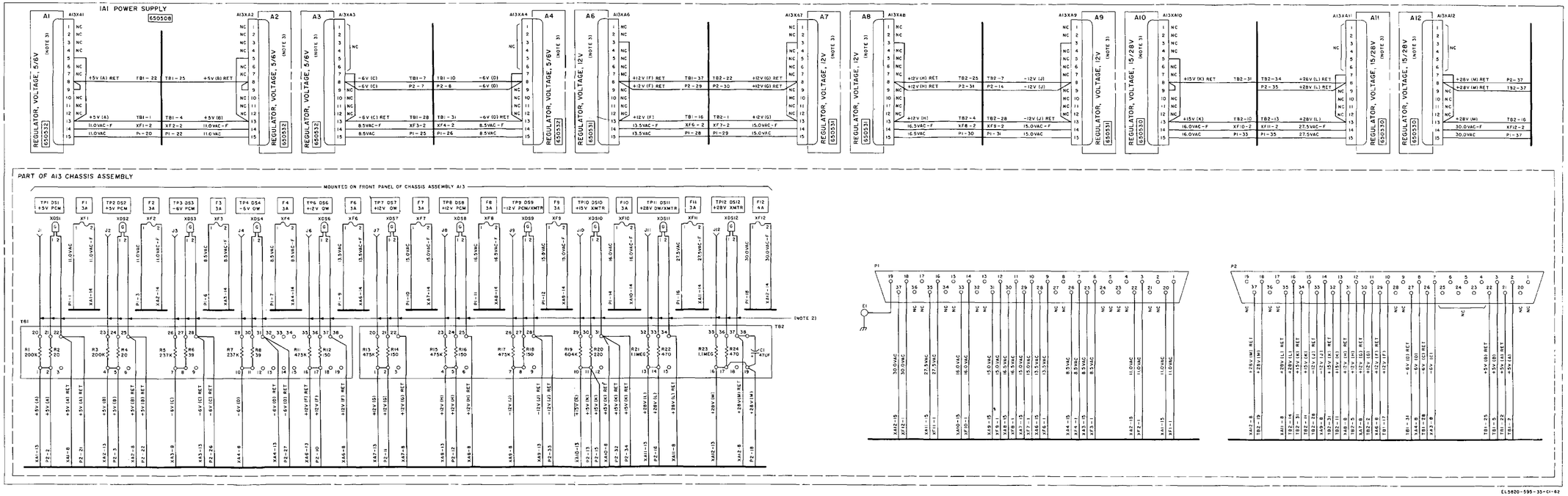


Figure 8-15. Transmitter dc power distribution.

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 20 AWG STRANDED, TEFLON INSULATED, EXCEPT FOR WIRES ON J1 THRU J12 AND XDS1 THRU XDS12 WHICH IS NO. 24 AWG.
3. CONNECTORS ON A1 THRU A12 ARE ETCHED CONTACTS ON PRINTED WIRING BOARD.
4. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS.



Change 1 Figure 8-16. Power supply 1A1, interconnecting diagram.

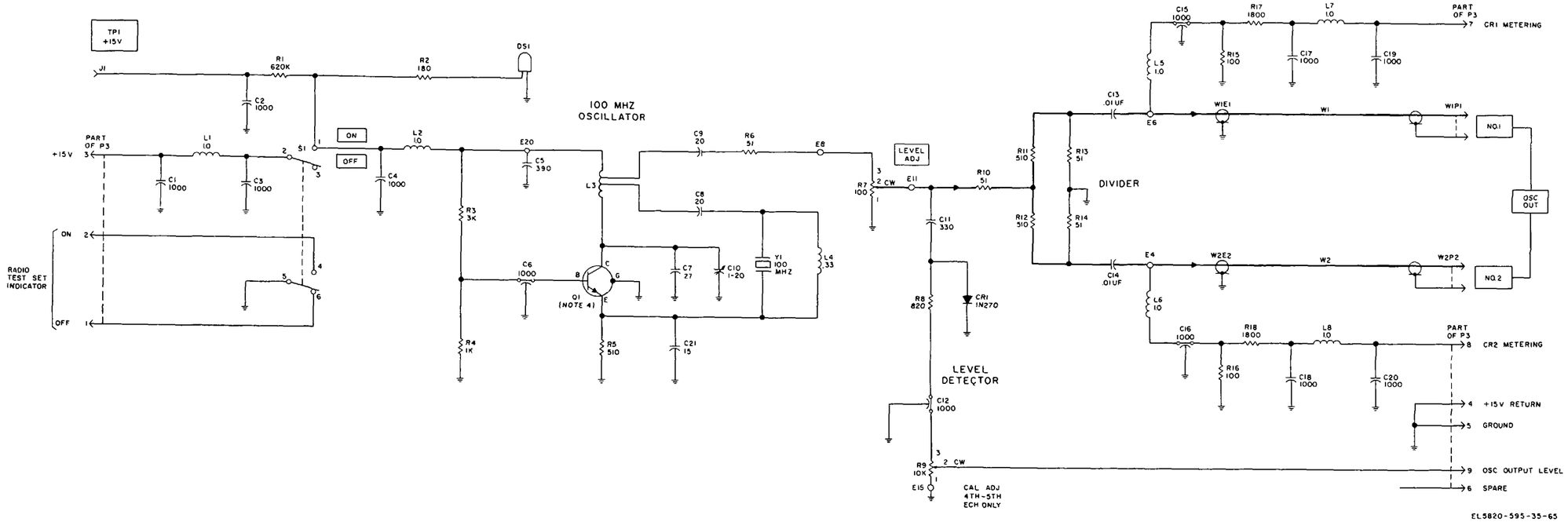
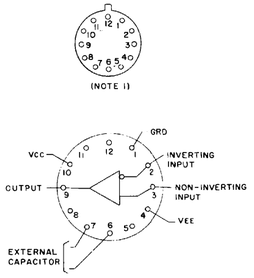


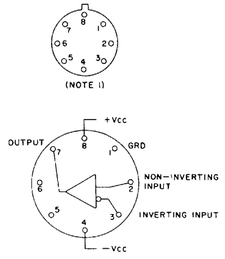
Figure 8-17. 100 MHz RF oscillator 1A2, schematic diagram.

NOTES:
1. DENOTES PIN LOCATION AS VIEWED FROM BOTTOM (PIN SIDE) OF INTEGRATED CIRCUIT.
2. DENOTES PIN LOCATION AS VIEWED FROM TOP (OPPOSITE PIN SIDE) OF INTEGRATED CIRCUIT.

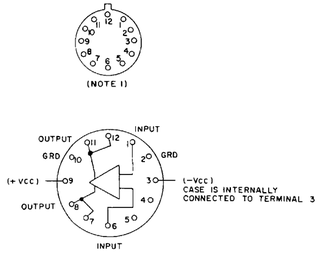
CA3015
OPERATIONAL AMPLIFIER



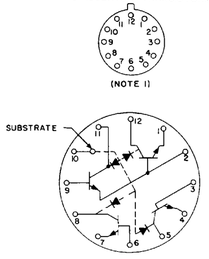
μ5B771031X OR LM710 OR UA710 (SPECIAL)
HIGH SPEED DIFFERENTIAL COMPARATOR



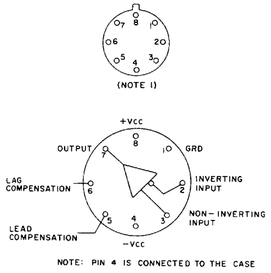
CA3001
LINEAR AMPLIFIER



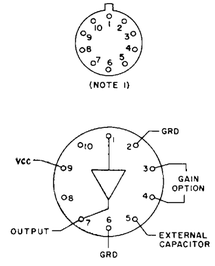
80286
LINEAR ARRAY-DARLINGTON PAIR AND TWO ISOLATED TRANSISTORS



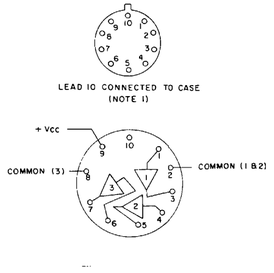
U5B770231X
OPERATIONAL AMPLIFIER



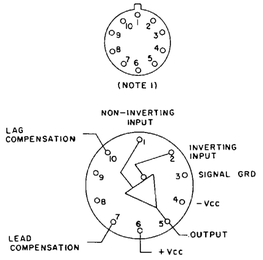
MC1553G
LINEAR AMPLIFIER



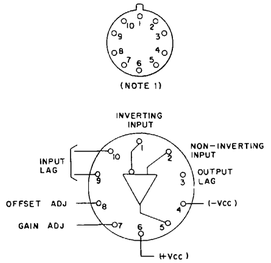
CA3035
3-IN-1 WIDEBAND AMPLIFIER ARRAY



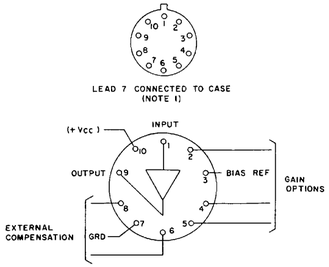
MC1531G
OPERATIONAL AMPLIFIER



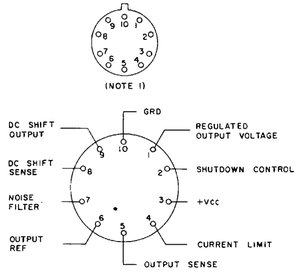
MC1533G
OPERATIONAL AMPLIFIER



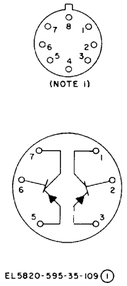
MC1554G
ONE WATT POWER AMPLIFIER



MC1560G
VOLTAGE REGULATOR



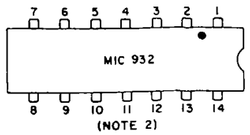
MD2905
DUAL PNP

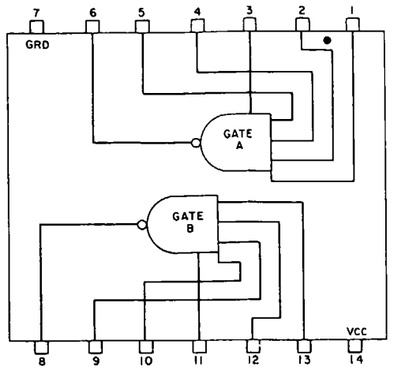


EL5820-595-35-109 (1)

Figure 8-18 (1). Integrated circuit schematic diagrams (part 1 of 4).

TYPE MIC932-ID
DUAL 4-INPUT BUFFER

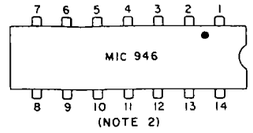


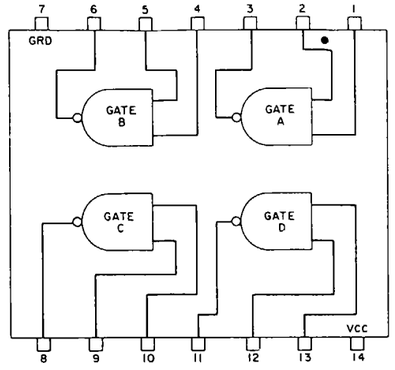


POSITIVE LOGIC
$6 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot (3EXP)}$
$8 = 9 \cdot 10 \cdot 12 \cdot 13 \cdot (11EXP)$

NOTE:
PINS 3 AND 11 ARE EXPANDER INPUTS

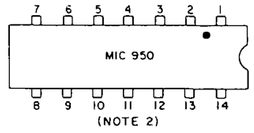
TYPE MIC946-ID, 949-ID, U6A90025IX, OR SL50604
QUAD 2-INPUT NAND-GATE

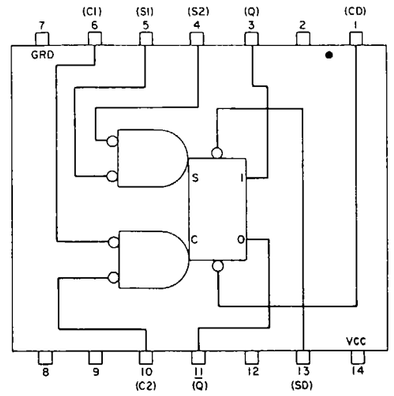




POSITIVE LOGIC
$3 = \overline{1 \cdot 2}$
$6 = \overline{4 \cdot 5}$
$8 = \overline{9 \cdot 10}$
$11 = \overline{12 \cdot 13}$

TYPE MIC950-ID OR MSC6847L
PULSE-TRIGGERED BINARY FLIP-FLOP

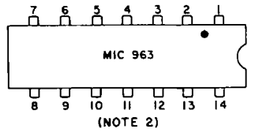


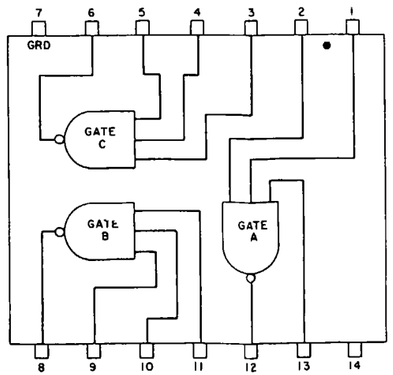


TRUTH TABLE

INPUT				OUTPUT
S1	S2	C1	C2	Q
0	0	1	0 → 1	1
0	0	0 → 1	1	1
1	0 → 1	1	0	0
0 → 1	1	1	0	0

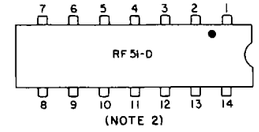
TYPE MIC963-ID
TRIPLE 3-INPUT NAND-GATE

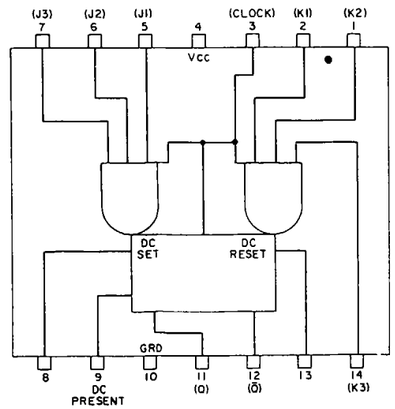




POSITIVE LOGIC
$6 = \overline{3 \cdot 4 \cdot 5}$
$8 = \overline{9 \cdot 10 \cdot 11}$
$12 = \overline{1 \cdot 2 \cdot 13}$

TYPE RF51D OR SF51-03
J-K FLIP-FLOP

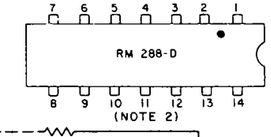


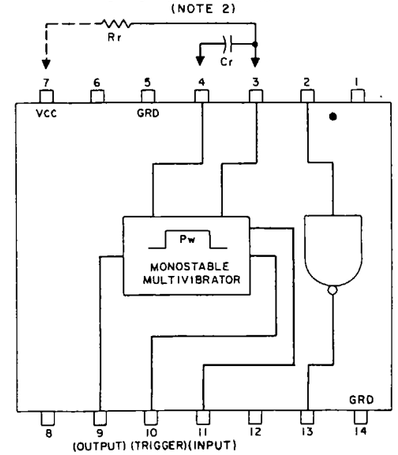


J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

NOTE:
J = J1·J2·J3
K = K1·K2·K3
Qn = BIT TIME BEFORE CLOCK PULSE
Qn+1 = BIT TIME AFTER CLOCK PULSE

TYPE RM288-D OR WM218K
MONOSTABLE MULTIVIBRATOR





NOTE:
Pw IS ESTABLISHED BY THE VALUES OF CAPACITOR Cr AND RESISTOR Rr WHICH ARE CONNECTED EXTERNALLY AS SHOWN ABOVE.

EL5820-595-35-CI-60 (2)

Figure 8-18 (2). Integrated circuit schematic diagrams (part 2 of 4).

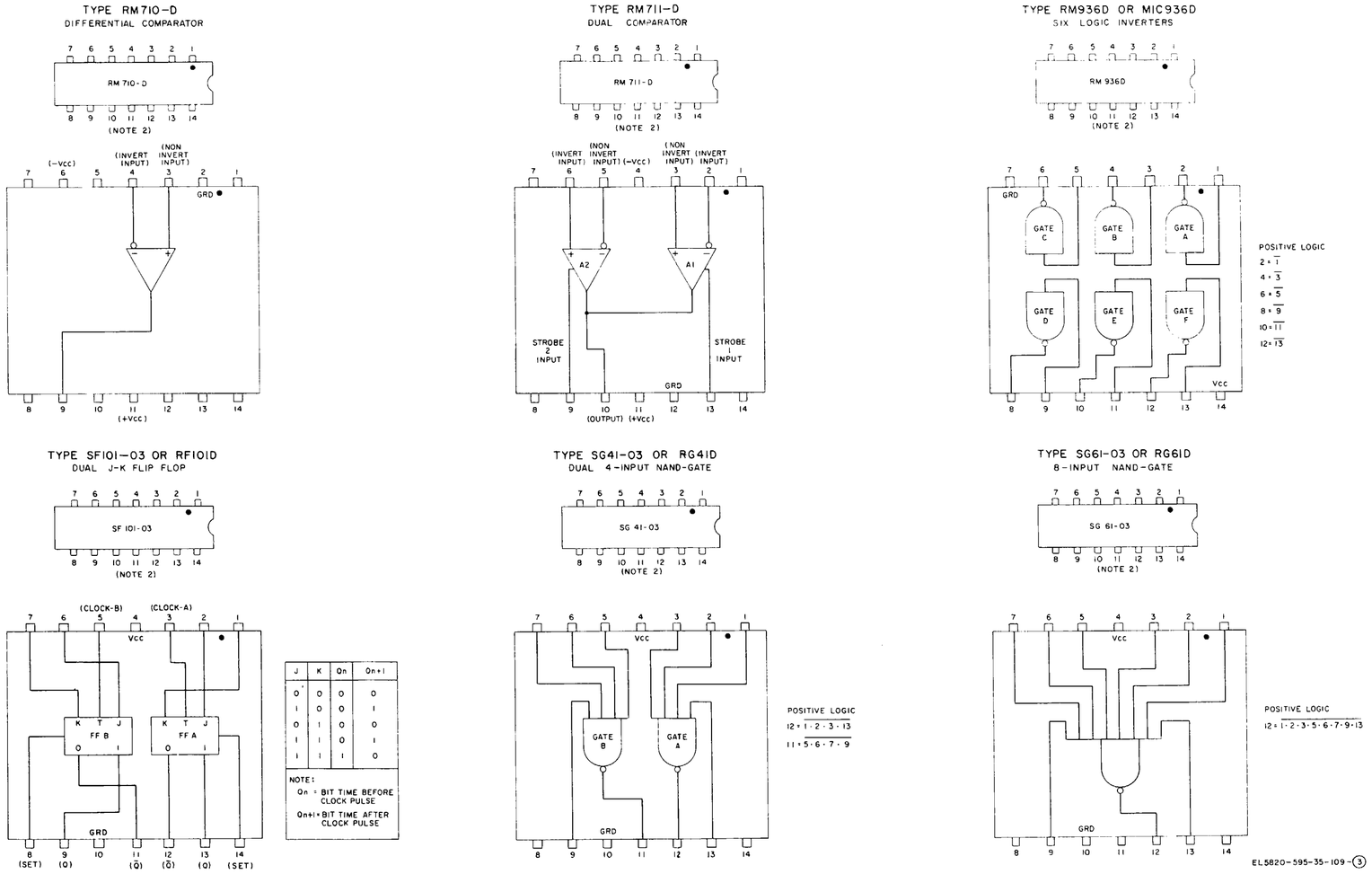
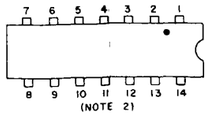
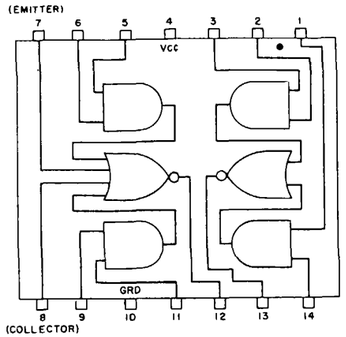


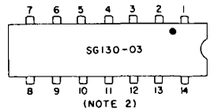
Figure 8-18 (3). Integrated circuit schematic diagrams (part 3 of 4).

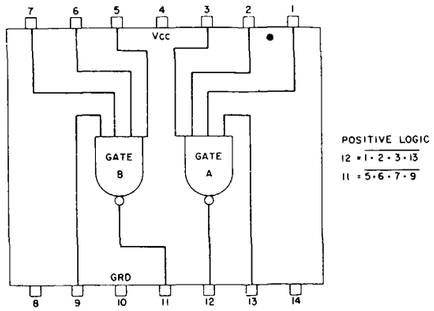
TYPE SG71-03 OR RG71D





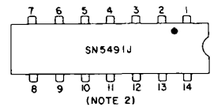
TYPE SG130-03 OR RG130D
DUAL 4-INPUT NAND-GATE

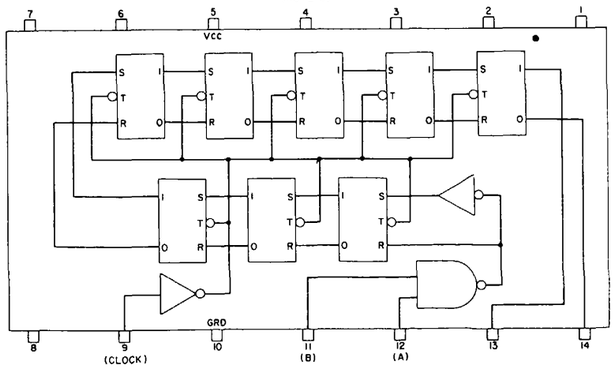




POSITIVE LOGIC
$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$
$11 = \overline{5 \cdot 6 \cdot 7 \cdot 9}$

TYPE SN5491J
8-BIT SHIFT REGISTER

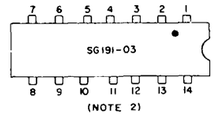


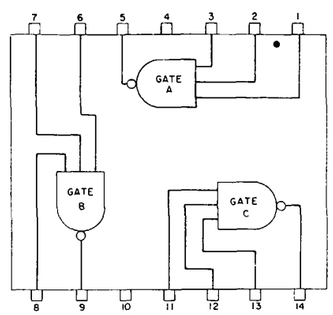


Tn		Tn+8
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTE:
Tn = BIT TIME BEFORE CLOCK PULSE
Tn+8 = BIT TIME AFTER 8 CLOCK PULSES

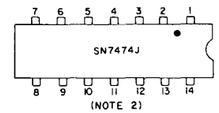
TYPE SG191-03 OR RG191D
TRIPLE 3-INPUT NAND-GATE

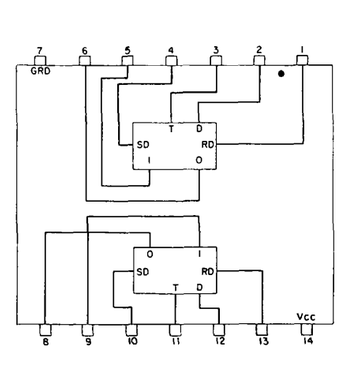




POSITIVE LOGIC
$5 = \overline{1 \cdot 2 \cdot 3}$
$9 = \overline{6 \cdot 7 \cdot 8}$
$14 = \overline{11 \cdot 12 \cdot 13}$

TYPE SN5474J
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

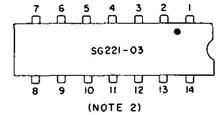


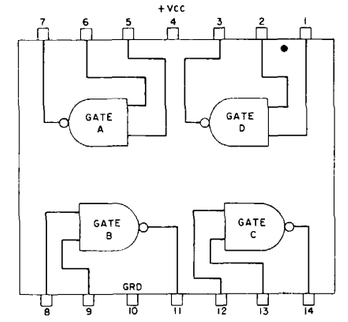


D	Qn	Qn+1
0	0	0
1	0	1
0	1	0

NOTE:
Qn = BIT TIME BEFORE CLOCK PULSE
Qn+1 = BIT TIME AFTER CLOCK PULSE

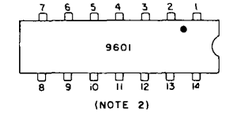
TYPE SG221-03, 141-03, RG141D
QUAD 2-INPUT NAND-GATE

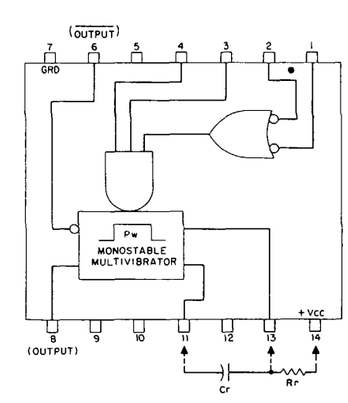




POSITIVE LOGIC
$3 = \overline{1 \cdot 2}$
$7 = \overline{5 \cdot 6}$
$11 = \overline{8 \cdot 9}$
$14 = \overline{12 \cdot 13}$

TYPE µA96A0151IX OR MIC9601-1D
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR





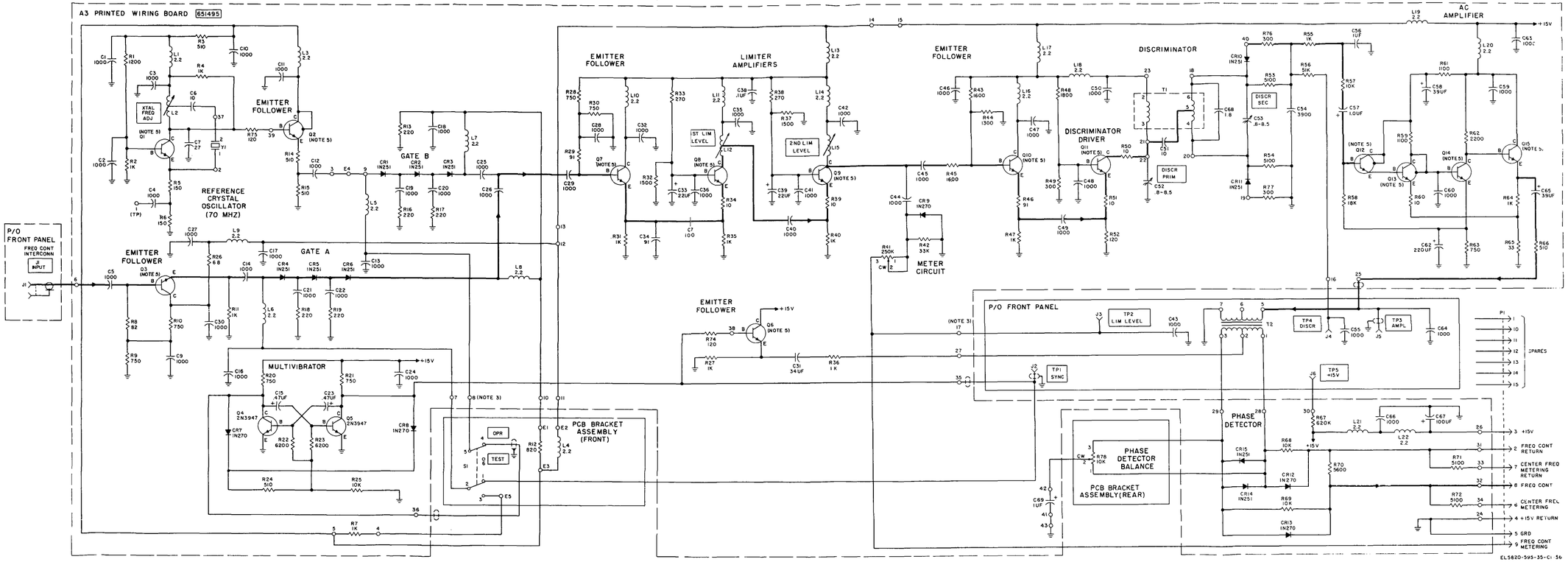
NOTE:
Pw IS ESTABLISHED BY THE VALUES OF CAPACITOR Cr AND RESISTOR Rr WHICH ARE CONNECTED EXTERNALLY AS SHOWN ABOVE.

EL5820-595-35-109 (4)

Figure 8-18 (4). Integrated circuit schematic diagrams (part 4 of 4).

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN PICOFARADS
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A7.
3. TERMINALS 1 THROUGH 11, 16, 17 AND 24 THROUGH 39 ARE MOUNTED ON THE PRINTED WIRING BOARD. TERMINALS 12 THROUGH 15 AND 18 THROUGH 23 ARE PADS ON THE PRINTED WIRING BOARD.
4. [ ] INDICATES MARKING ON EQUIPMENT.
5. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING.

REFERENCE DESIGNATION	SPECIFICATION DRAWING
Q1, Q3, Q7, Q11	SM-B-653437-1
Q6, Q14, Q15	SM-B-653417
Q8, Q9, Q10	SM-B-653437-2
Q2, Q12, Q13	SM-B-653389

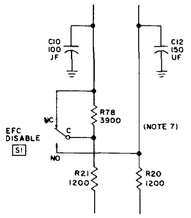


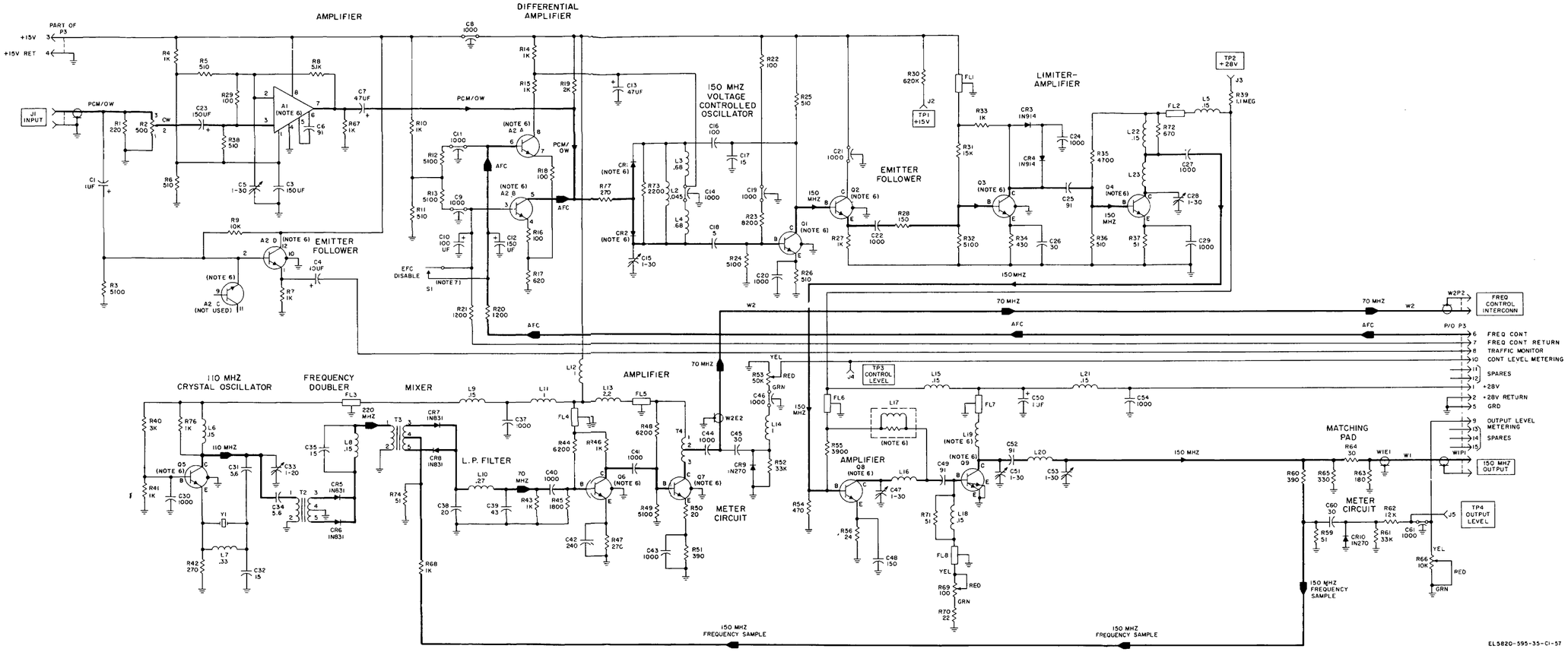
Change 1 **Figure 8-19. Electronic frequency control 1A7, schematic diagram.**

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN PICOFARADS INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX REFERENCE DESIGNATIONS WITH 1A8.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. THE COMPLETE TYPE DESIGNATOR FOR U702 IS US8770231X.
5. LEGEND:
   - MAIN SIGNAL FLOW
   - REFERENCE SIGNAL FLOW
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING.

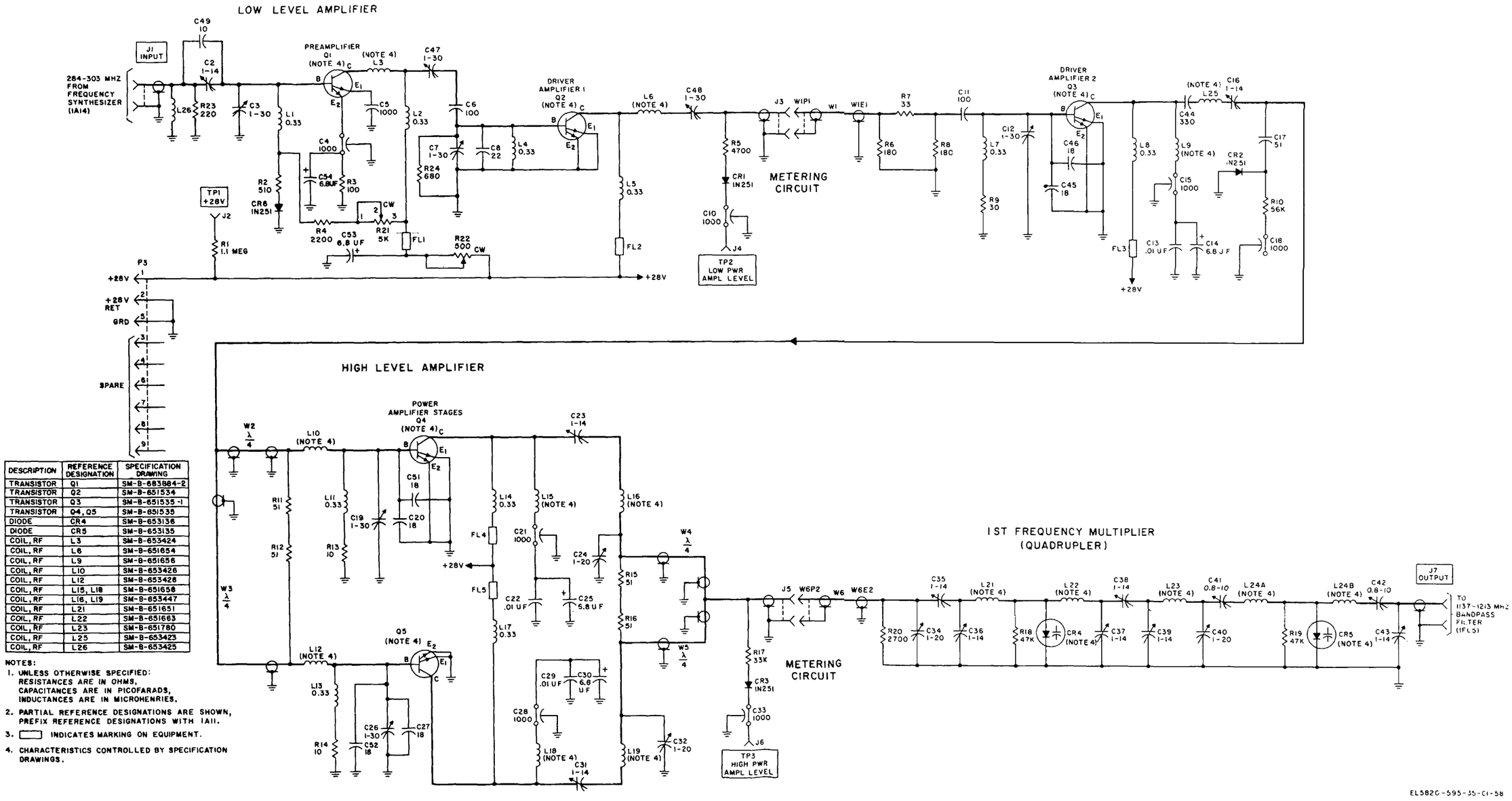
DESCRIPTION	REFERENCE DESIGNATION	SPECIFICATION DRAWING
TRANSISTOR	Q1, Q2, Q3, Q5 Q6, Q7	SM-B-653389
TRANSISTOR	Q9	SM-B-651535
COIL, RF	L19	SM-B-651365
DIODE	CR1, CR2	SM-B-653076
SUPPRESSOR	L17	SM-B-651350
OPERATIONAL AMPLIFIER	A1	SM-B-650746
LINEAR AMPLIFIER	A2	SM-B-653078
TRANSISTOR	Q4, Q8	SM-B-650721

7. IN SOME COMPONENTS RESISTOR R78 IS ADDED AND SWITCH S1 IS SPDT AS SHOWN IN PARTIAL SCHEMATIC BELOW.





Change 1 **Figure 8-20. Modulator 1A8, schematic diagram.**



DESCRIPTION	REFERENCE DESIGNATION	SPECIFICATION DRAWING
TRANSISTOR	Q1	SM-B-683884-2
TRANSISTOR	Q2	SM-B-651534
TRANSISTOR	Q3	SM-B-651535-1
TRANSISTOR	Q4, Q5	SM-B-651535
DIODE	CR4	SM-B-653136
DIODE	CR5	SM-B-653135
COIL, RF	L3	SM-B-653424
COIL, RF	L6	SM-B-651654
COIL, RF	L9	SM-B-651656
COIL, RF	L10	SM-B-653426
COIL, RF	L12	SM-B-653428
COIL, RF	L15, L18	SM-B-651658
COIL, RF	L16, L19	SM-B-653447
COIL, RF	L21	SM-B-651651
COIL, RF	L22	SM-B-651663
COIL, RF	L23	SM-B-651780
COIL, RF	L25	SM-B-653423
COIL, RF	L26	SM-B-653425

NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN PICOFARADS, INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 1A11.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWINGS.

Change 1 **Figure 8-21. Amplifier-frequency multiplier 1A11, schematic diagram.**

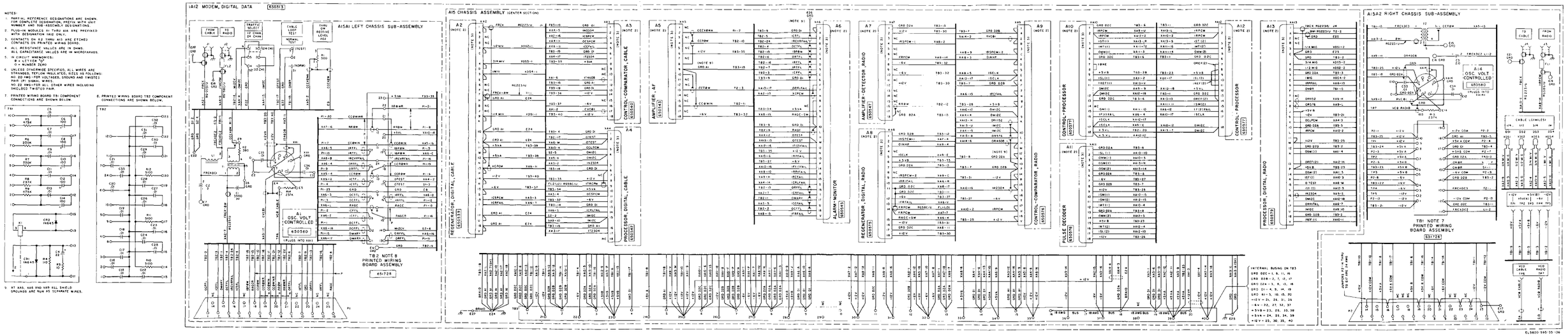


Figure 8-22. Digital data modem 1A12, interconnecting diagram

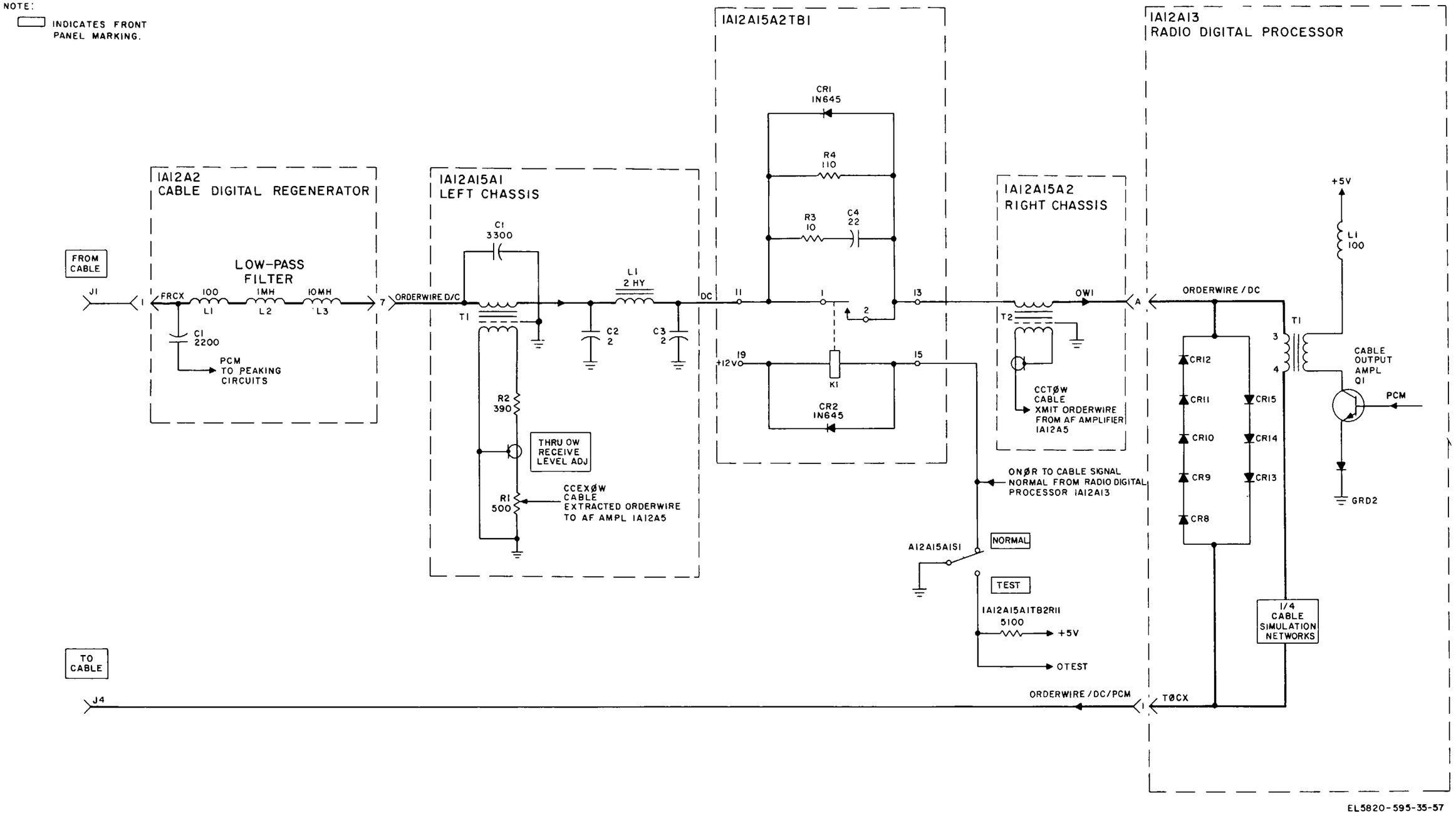


Figure 8-23. Transmitter cable dc current path, simplified schematic diagram.

NOTES

1. UNLESS OTHERWISE SPECIFIED
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS
   INDUCTANCES ARE IN MICROHENRIES
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A12A2
3. ALL TERMINALS PREFIXED WITH E ARE TEST POINTS
4. REFER TO TABLE FOR STRAPPING CONFIGURATIONS

TABLE

CABLE LENGTH	CONNECTIONS MADE WHEN P2 IS INSERTED INTO J3
1/4MILE	AI TO A2, A3 TO A4, A5 TO A6, A7 TO A8, A9 TO A10
1/2MILE	BI TO B2, B5 TO B6, B7 TO B8, B9 TO B10
3/4MILE	CI TO C2, C7 TO C8, C9 TO C10
1 MILE	DI TO D2, D9 TO D10

5. INTEGRATED CIRCUIT A1 IS A SPECIALLY SELECTED UA710 PER ITTDCD DRAWING SM-B-683816.

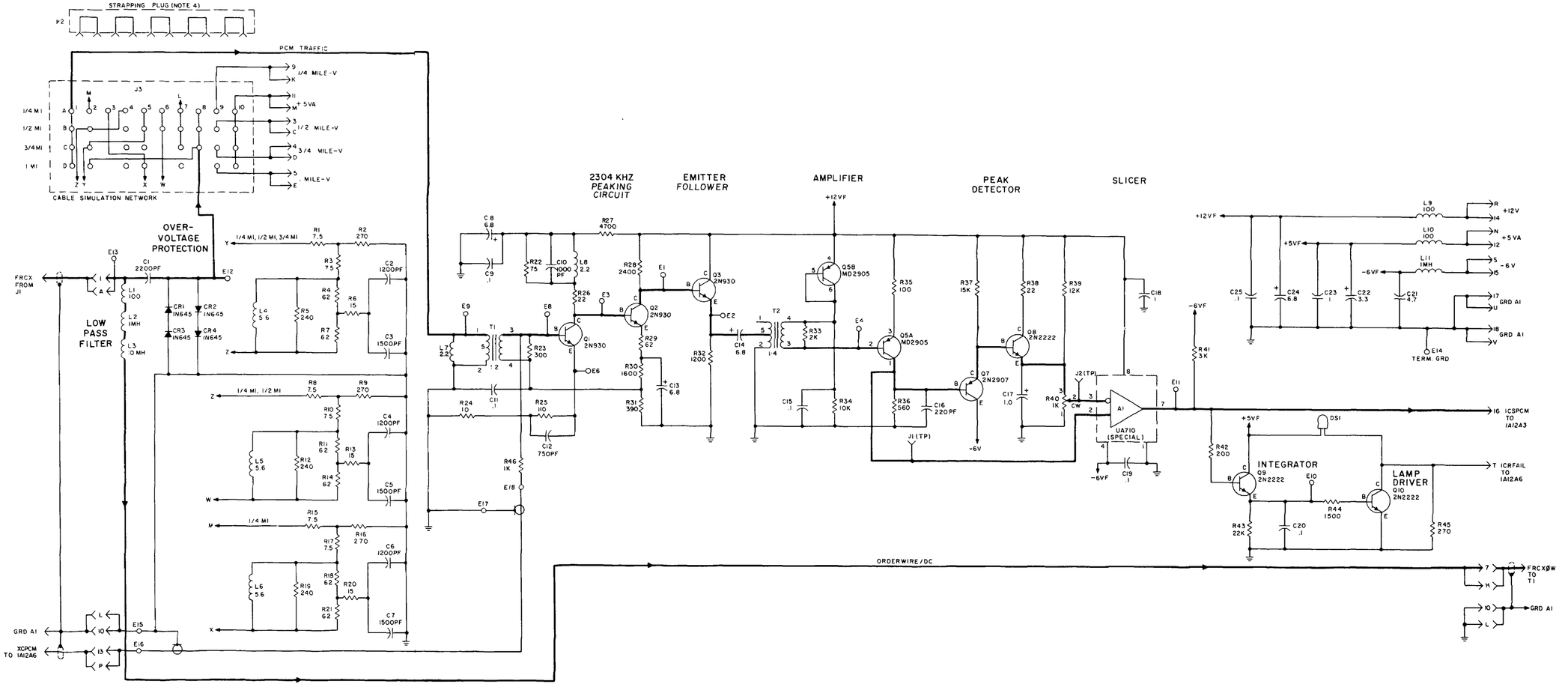


Figure 8-24. Cable digital regenerator 1A12A2, schematic diagram.

Change 1

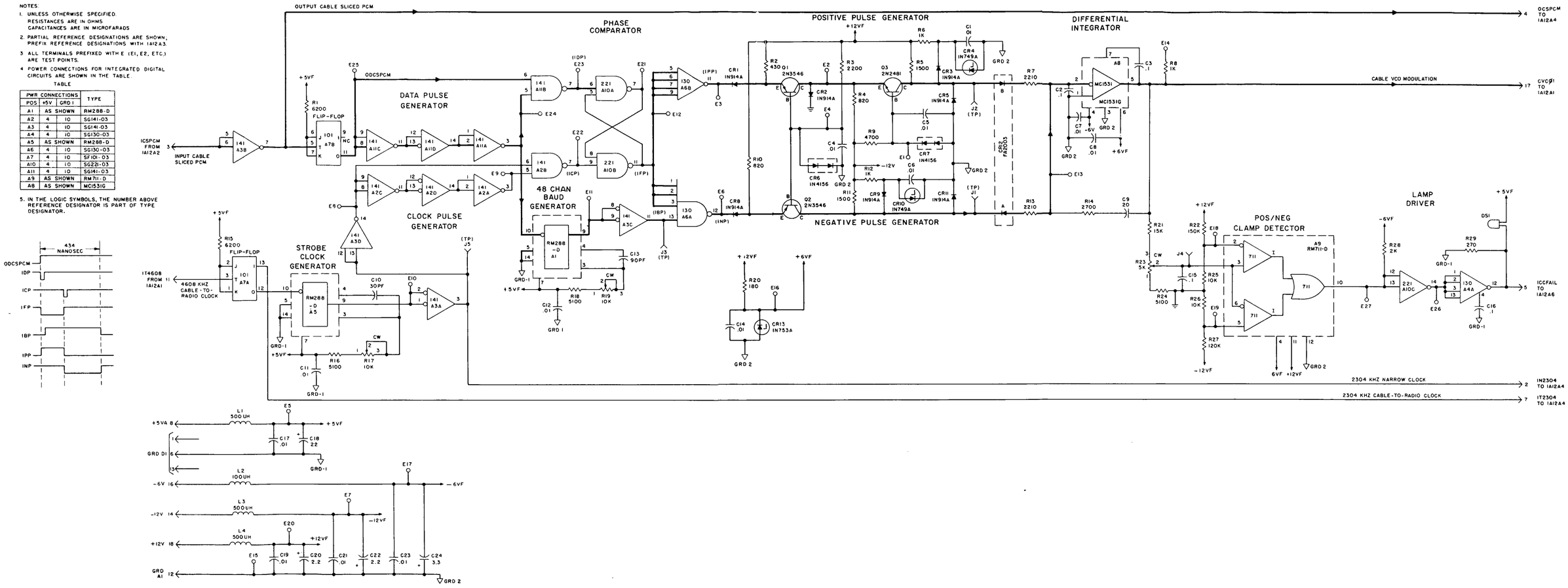


Figure 8-25. Cable control comparator 1A12A3, schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A12A4.
3. STRAPPING OPTIONS ARE SHOWN AS FOLLOWS: OPTION Y FOR G1 (12-24 CHANNEL OPERATION) OPTION Z FOR G2 (48 CHANNEL OPERATION) NUMBERS 1 THRU 6 MARKED PADS ON THE BOARD.
4. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS.
5. IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
6. POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN THE TABLE.

TABLE

POS	POWER CONNECTIONS +5VF	GRD 1	GRD 2	GRD 3	TYPE
A1	SHOWN CONNECTED				U6A960151X
A2	14	7			SN5474-J
A3	4	10			SG41-03
A4	4	10			SG141-03
A5	4	10			SG191-03
A6	4	10			SG141-03
A7	4		10		SG101-03
A8	4		10		SG141-03
A9	4		10		SG141-03
A10	14		7		SN5474-J
A11	4		10		SG130-03
A12	4			10	SG141-03
A13	SHOWN CONNECTED				MC1531G
A14	SHOWN CONNECTED				U6A960151X
A15	SHOWN CONNECTED				RM710-D

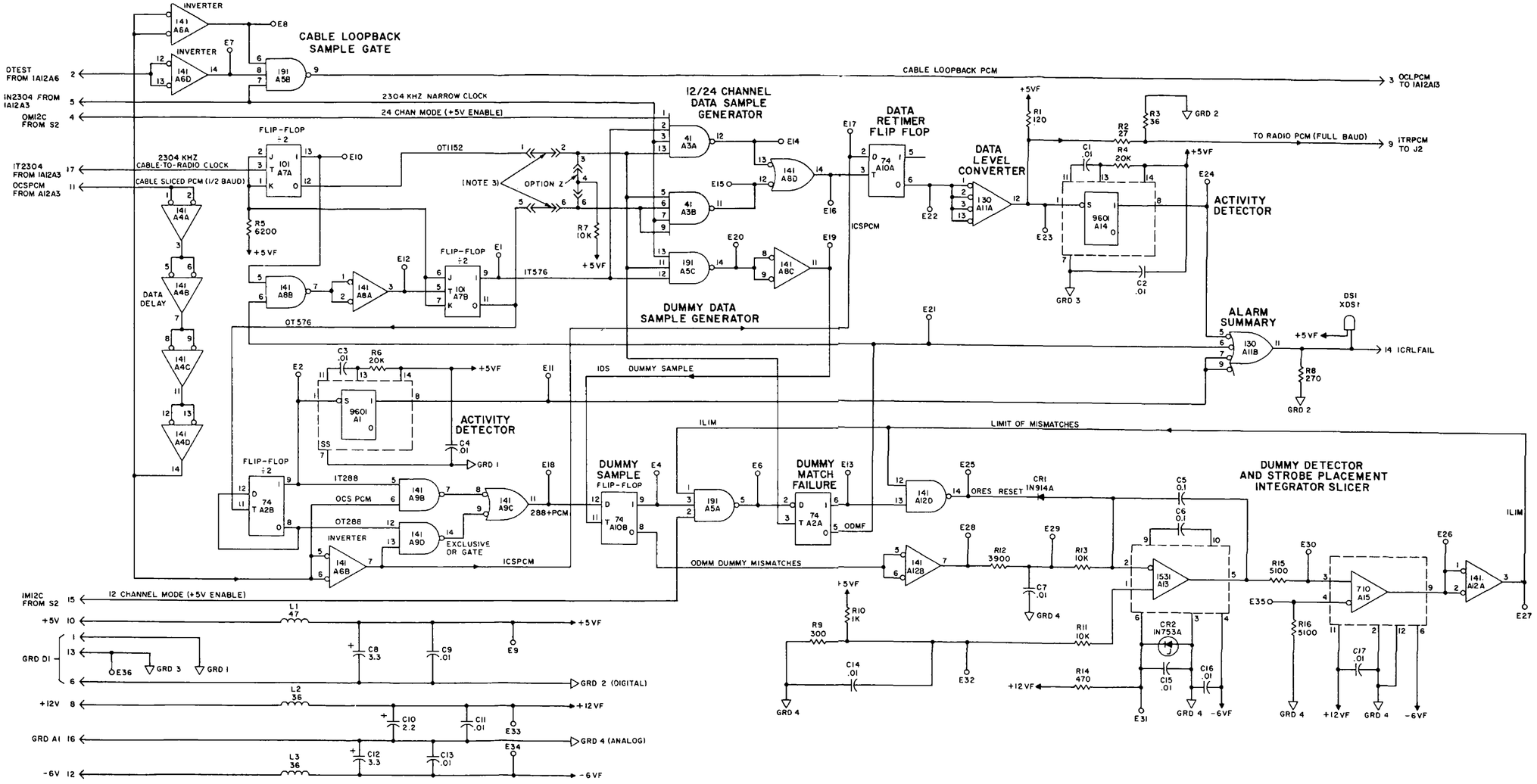
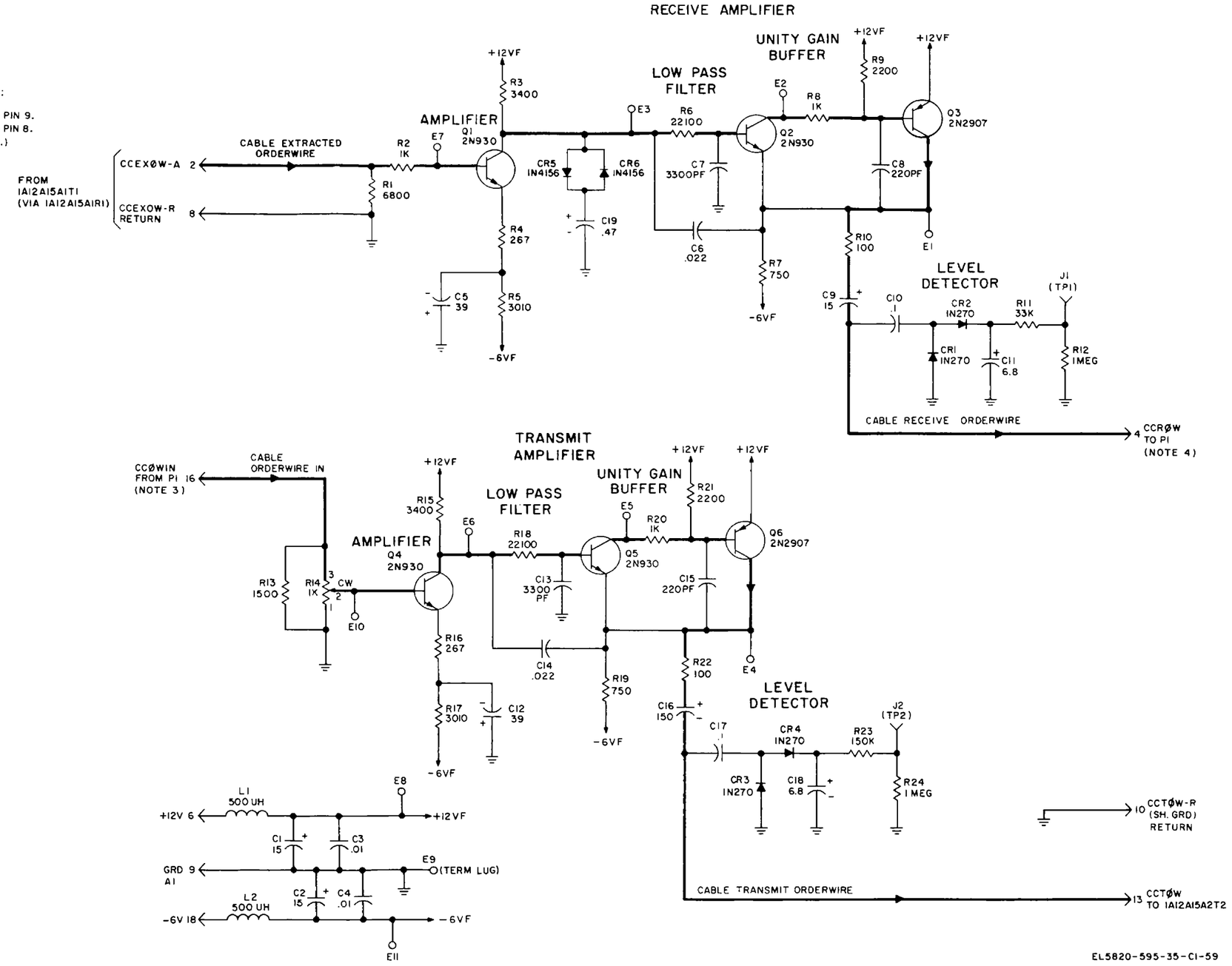


Figure 8-26. Cable digital processor 1A12A4, schematic diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 1A12A5.
3. SIGNAL RETURN FOR CCØWIN IS CONNECTED TO PIN 9.
4. SIGNAL RETURN FOR CCRØW IS CONNECTED TO PIN 8.
5. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.



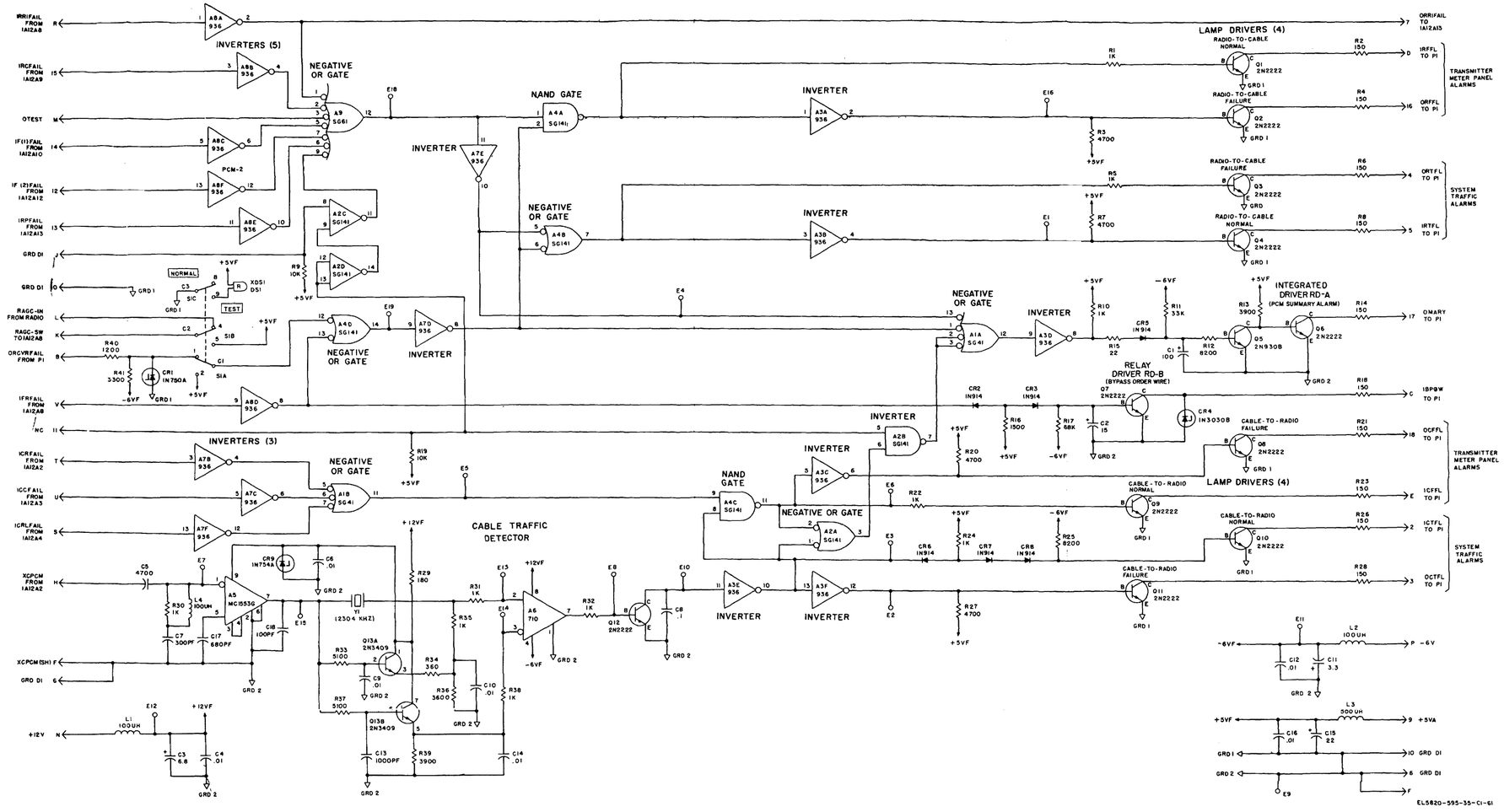
Change 1 **Figure 8-27. AF amplifier 1A12A5, schematic diagram.**

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A6.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
4. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

POWER CONNECTIONS			TYPE
POS	+5VF	GRD I	
A1	4	10	SG41-03
A2	4	10	SG141-03
A3	14	7	RM936D
A4	4	10	SG141-03
A7	14	7	RM936D
A8	14	7	RM936D
A9	4	10	SG61-03
A5	AS SHOWN		MC1553G
A6	AS SHOWN		U5877103HX

5. POWER CONNECTIONS FOR EACH INTEGRATED CIRCUIT ARE SHOWN IN THE TABLE ABOVE.



Change 1 **Figure 8-28. Alarm monitor 1A12A6, schematic diagram.**

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS
   INDUCTANCES ARE IN MICROHENRIES
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A7
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
4. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE IS PART OF THE TYPE DESIGNATOR.
5. THE COMPLETE TYPE DESIGNATOR FOR 1531 IS MC1531G.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-652264.

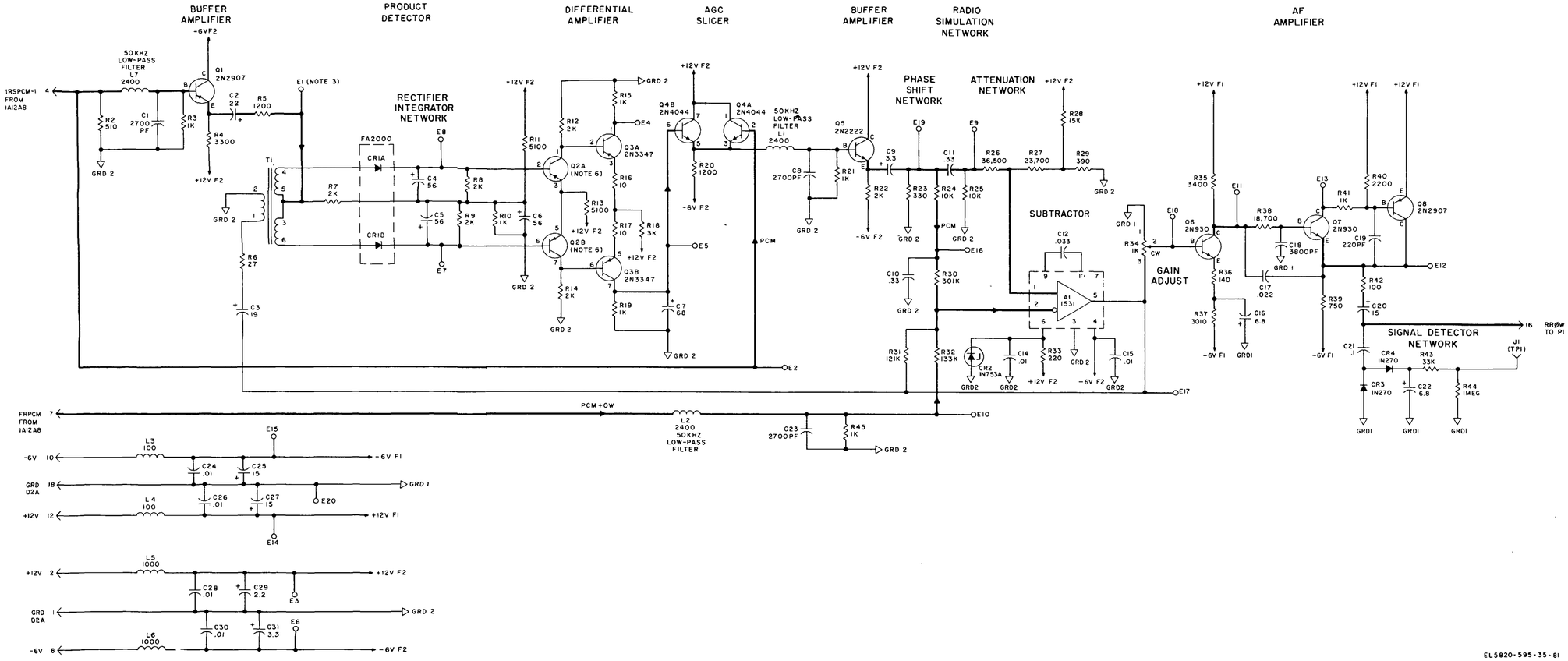


Figure 8-29. Amplifier-detector 1A12A7, schematic diagram.

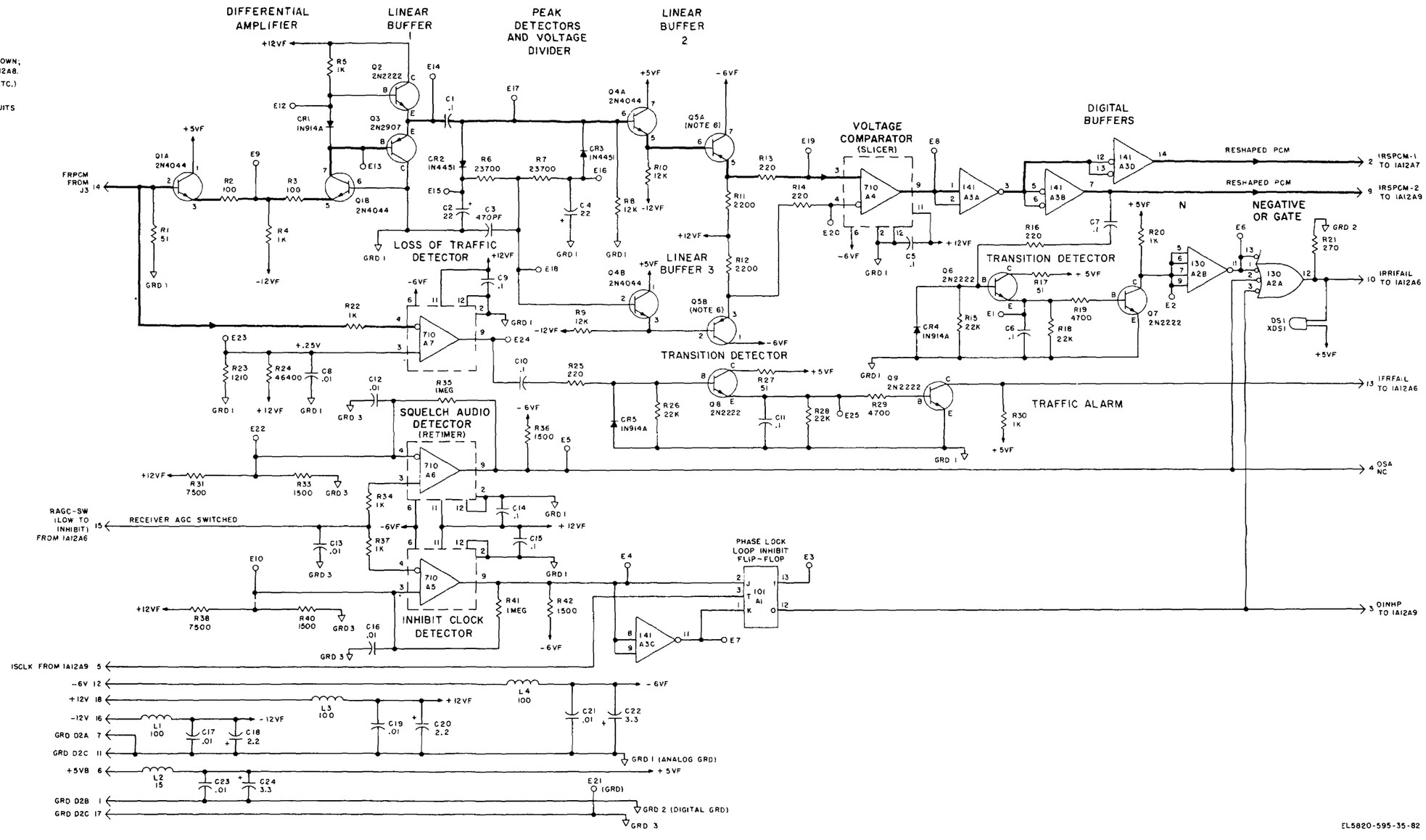
NOTES:

1. UNLESS OTHERWISE SPECIFIED. RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS. INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A8.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
4. POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN THE TABLE.

TABLE

	PWR CONNECTIONS		TYPE
	+5VF	GRD 2	
A1	4	10	SF101-03
A2	4	10	SG130-03
A3	4	10	SG141-03
A4	SHOWN CONNEC.		RM710-D
A5	SHOWN CONNEC.		RM710-D
A6	SHOWN CONNEC.		RM710-D
A7	SHOWN CONNEC.		RM710-D

5. IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-652264.



EL5820-595-35-82

Figure 8-30. Radio digital regenerator 1A12A8, schematic diagram.

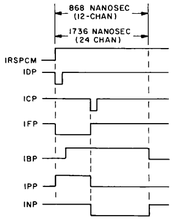
NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS. INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX REFERENCE DESIGNATIONS WITH 1A12A9.
3. ALL TERMINALS PREFIXED WITH E (E1,E2,ETC.) ARE TEST POINTS.
4. POWER CONNECTIONS FOR INTEGRATED DIGITAL CIRCUITS ARE SHOWN IN THE TABLE.

TABLE

PWR CONNECTIONS			TYPE
POS	+5V	GRD 1	
A2	4	10	SG221-03
A3	4	10	SG141-03
A4	4	10	SG141-03
A5	4	10	SG191-03
A7	4	10	SG130-03
A8	4	10	SG71-03
A9	4	10	SG130-03
A12	14	7	SN5474-J
A13	14	7	SN5474-J
A1	AS SHOWN		MC1531G
A6	AS SHOWN		RM288-D
A10	AS SHOWN		RM711-D
A11	AS SHOWN		RM288-D

5. IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.



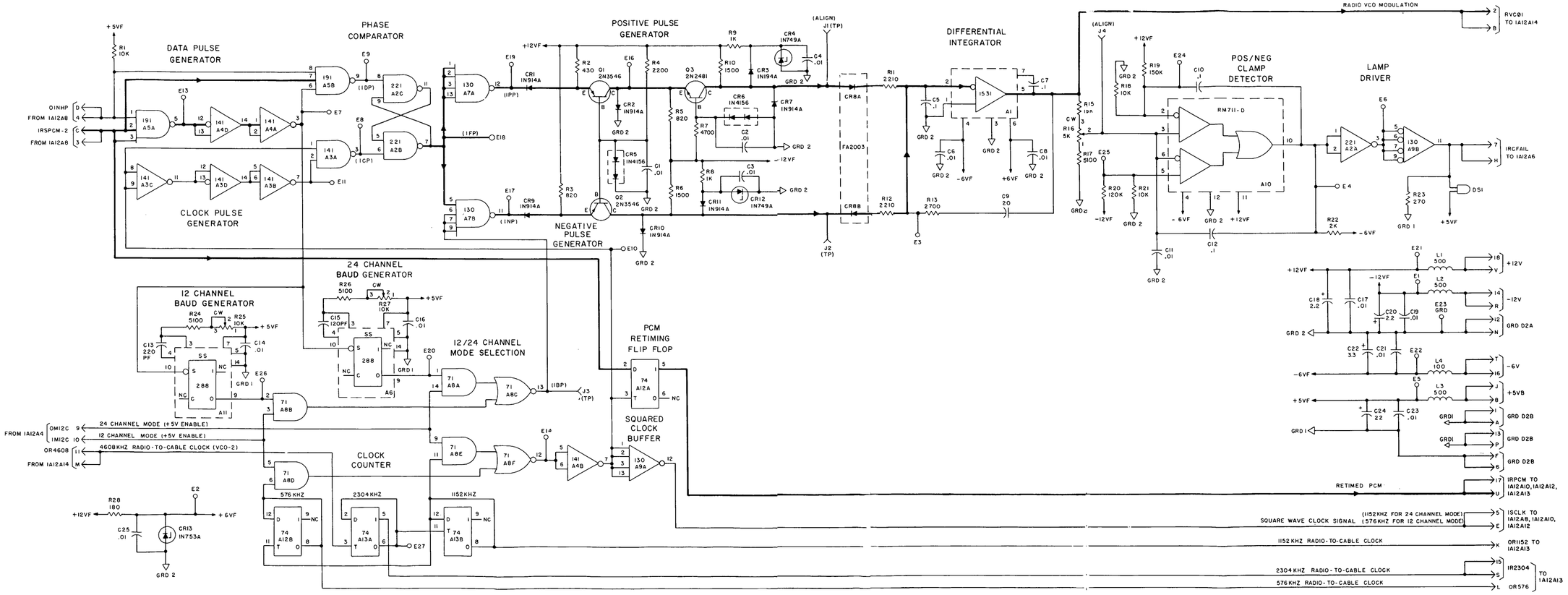


Figure 8-31. Radio control comparator 1A12A9, schematic diagram

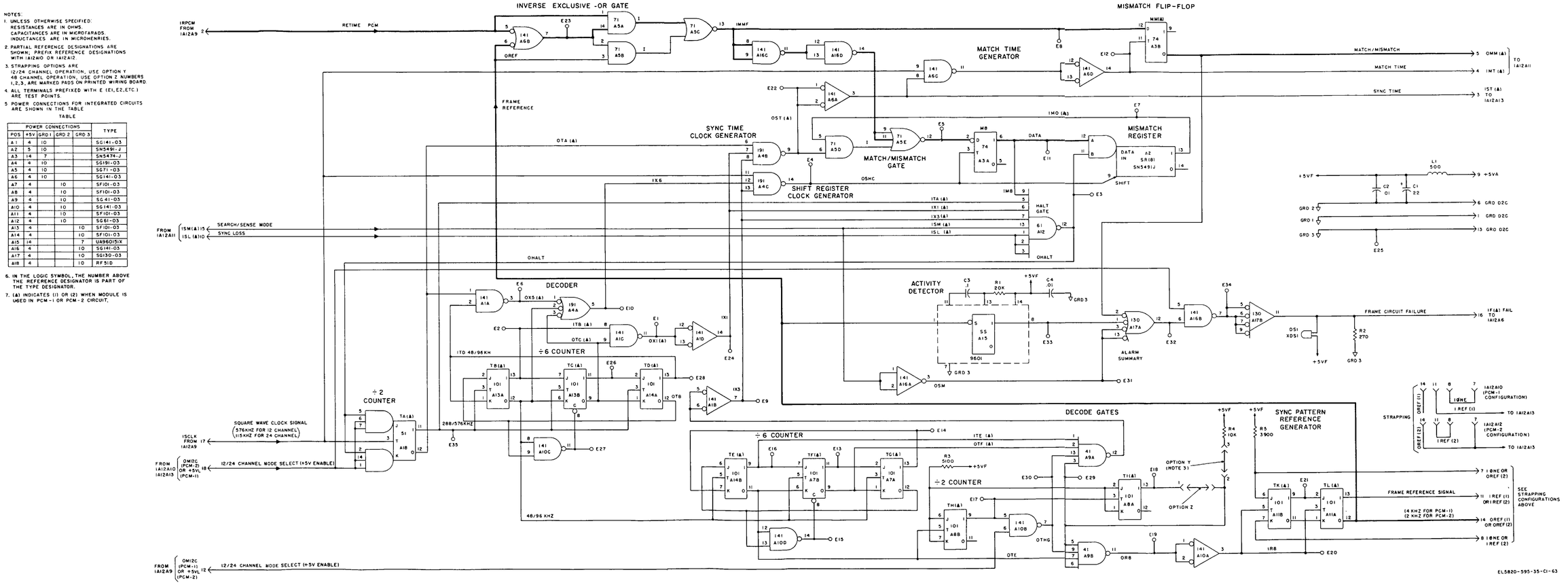


Figure 8-32. Control processor No. 1, 1A12A10 and No. 2, 1A12A12, schematic diagram.

Change 1

NOTES

1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICROFARADS INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A11.
3. JACKS J1 THROUGH J10 AND TERMINALS PREFIXED WITH E (E1,E2,ETC) ARE TEST POINTS.
4. INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

POS	TYPE
A1	MC1553G
A2	RM710-D
A3	MC1553G
A4	RM710-D
A5	RM710-D
A6	SF101-03
A7	MC1553G
A8	RM710-D
A9	MC1553G
A10	RM710-D
A11	RM710-D

5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
6. (1) INDICATES SIGNAL IS USED IN THE PCM-1 CIRCUIT. (2) INDICATES SIGNAL IS USED IN PCM-2 CIRCUIT.

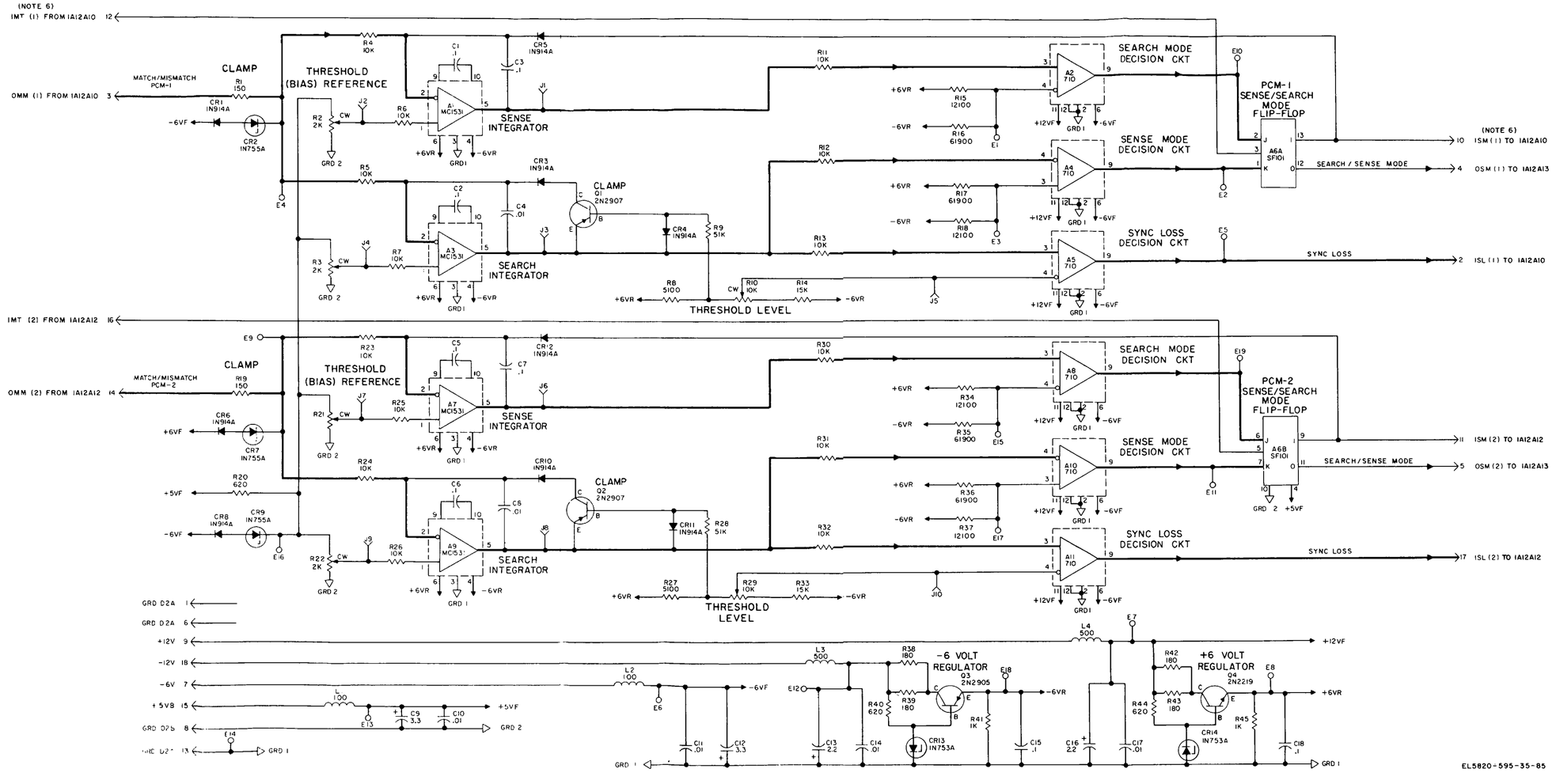


Figure 8-33. Pulse decoder 1A12A11, schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN MICROFARADS.
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 1A12A13.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.) ARE TEST POINTS.
4. REFER TO TABLE I FOR STRAPPING CONFIGURATIONS

TABLE I

CABLE LENGTH	CONNECTIONS MADE WHEN P2 IS INSERTED INTO J1
1/4 MILE	A1 TO A2, A3 TO A4, A5 TO A6, A7 TO A8, A9 TO A10
1/2 MILE	B1 TO B2, B3 TO B4, B7 TO B8, B9 TO B10
3/4 MILE	C1 TO C2, C7 TO C8, C9 TO C10
1 MILE	D7 TO D8, D9 TO D10

5. POWER CONNECTIONS FOR INTEGRATED CIRCUITS ARE SHOWN IN TABLE 2.

TABLE 2

PWR CONNECTIONS			TYPE
GATE	+5VF	GRD I	
A1	14	7	SN5474-J
A2	7	14	RM288-D
A3	4	10	SG71-03
A4	4	10	SG141-03
A5	4	10	SG71-03
A6	4	10	SG141-03
A7	4	10	SG19H-03

6. IN THE LOGIC SYMBOL, THE NUMBER ABOVE THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

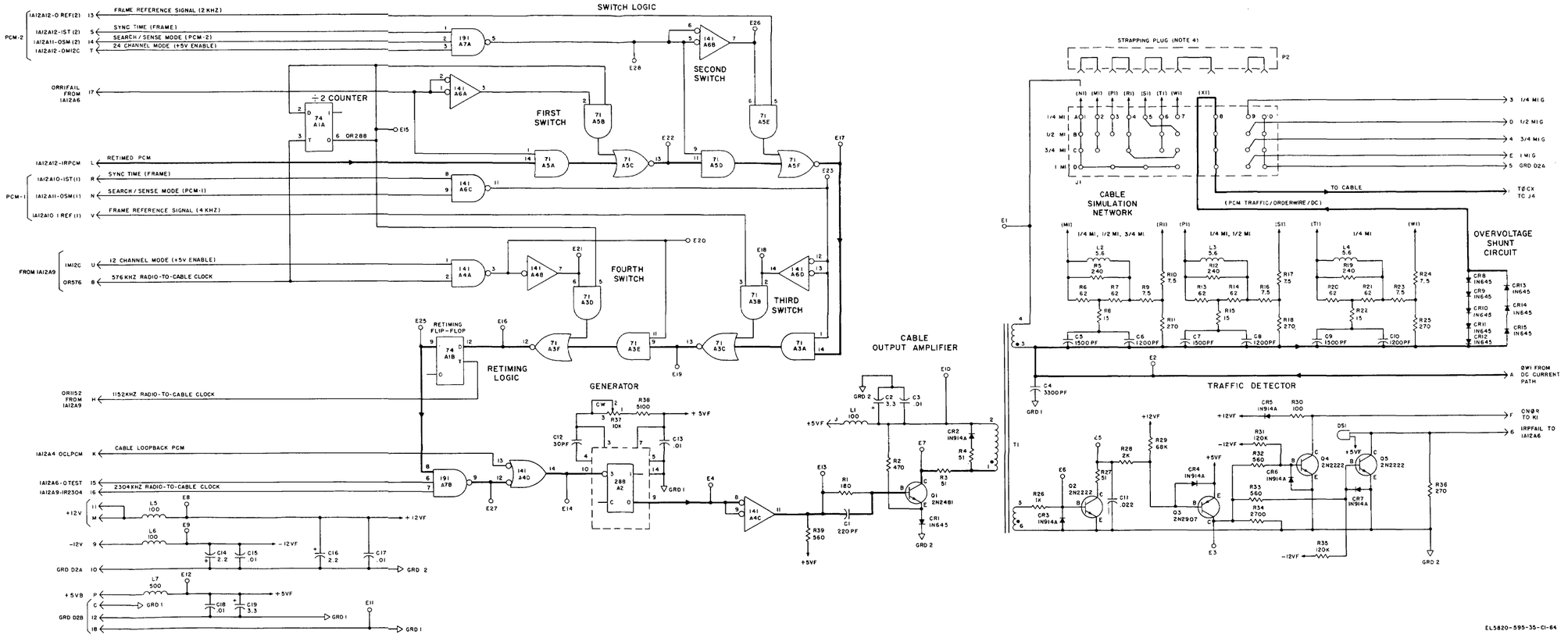


Figure 8-34. Radio digital processor 1A12A13, schematic diagram.

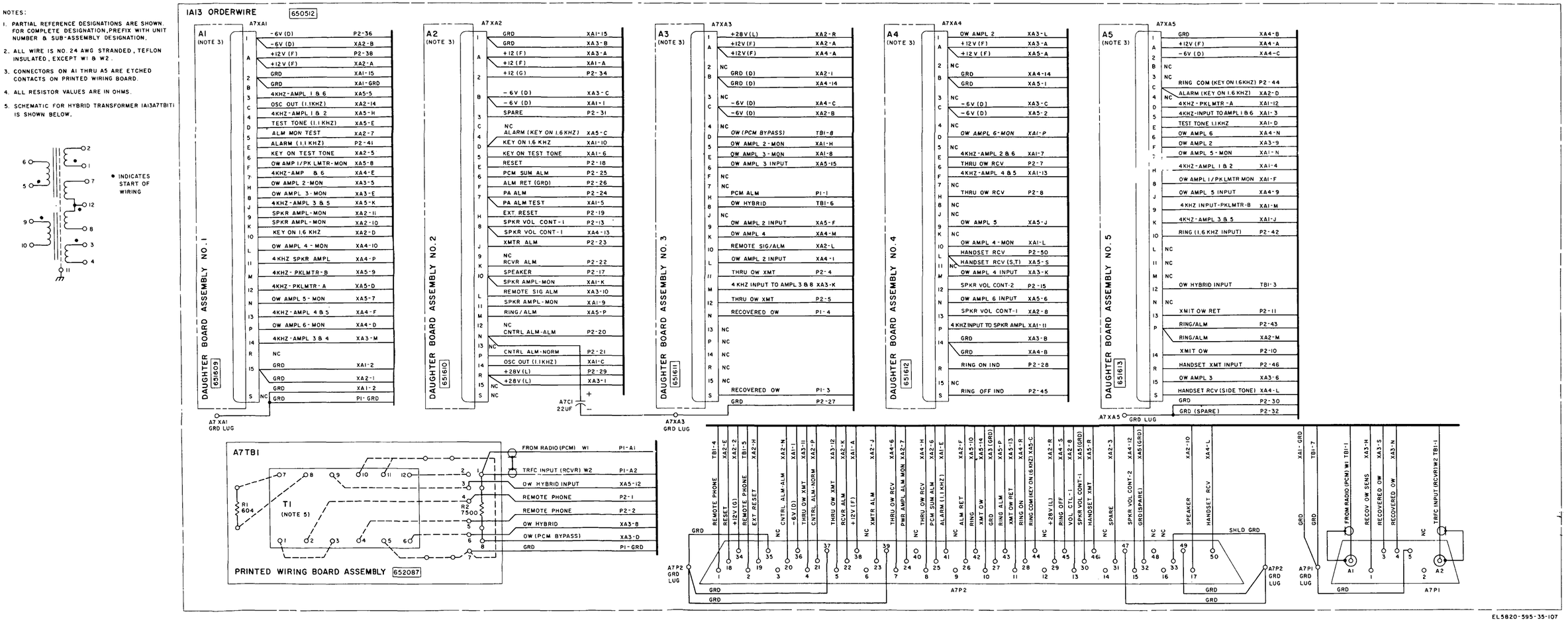


Figure 8-35. Orderwire assembly 1A13, interconnecting diagram.

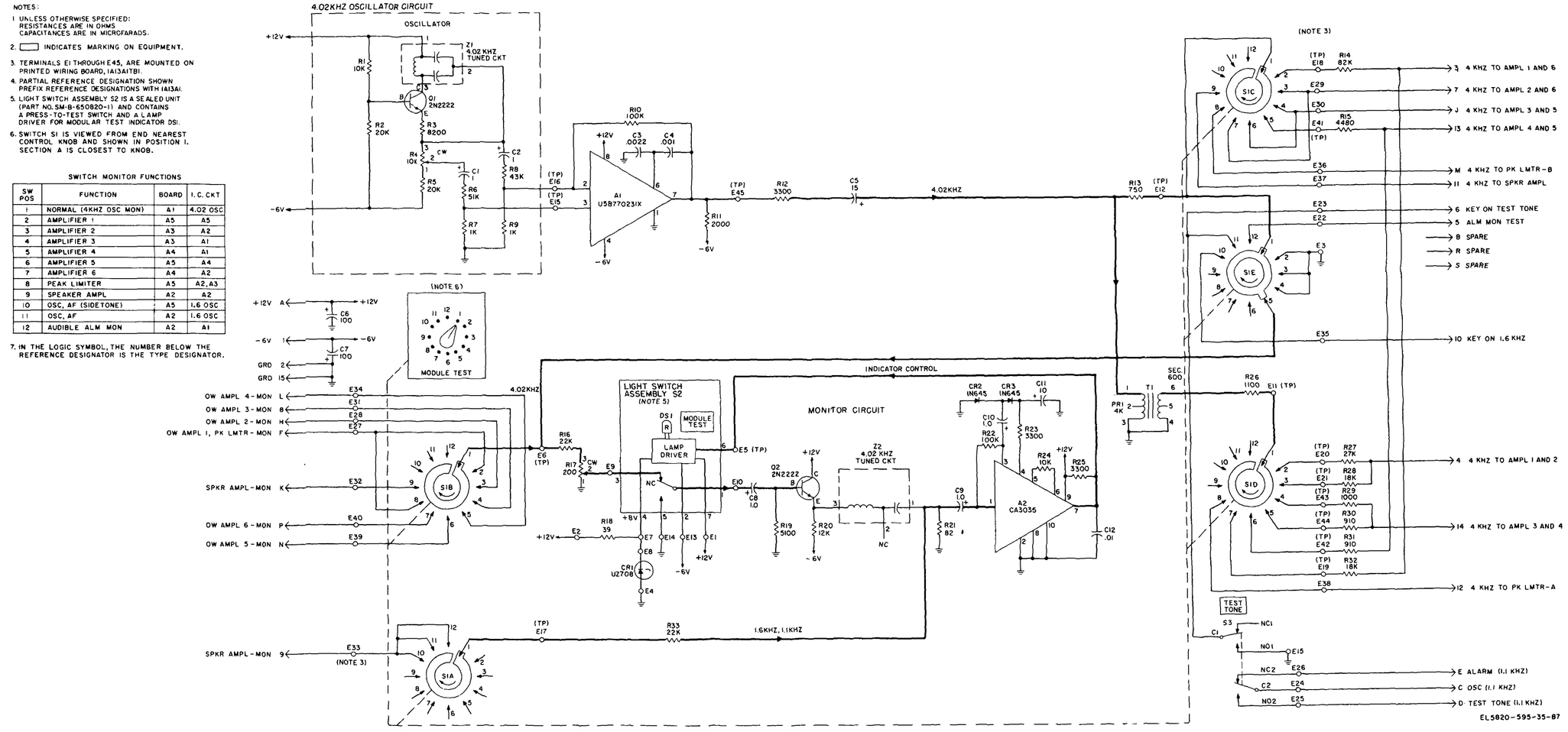


Figure 8-36. Board N0. 1, 1A13A1, schematic diagram

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 1A13A2
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS
4. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS THE TYPE DESIGNATOR.

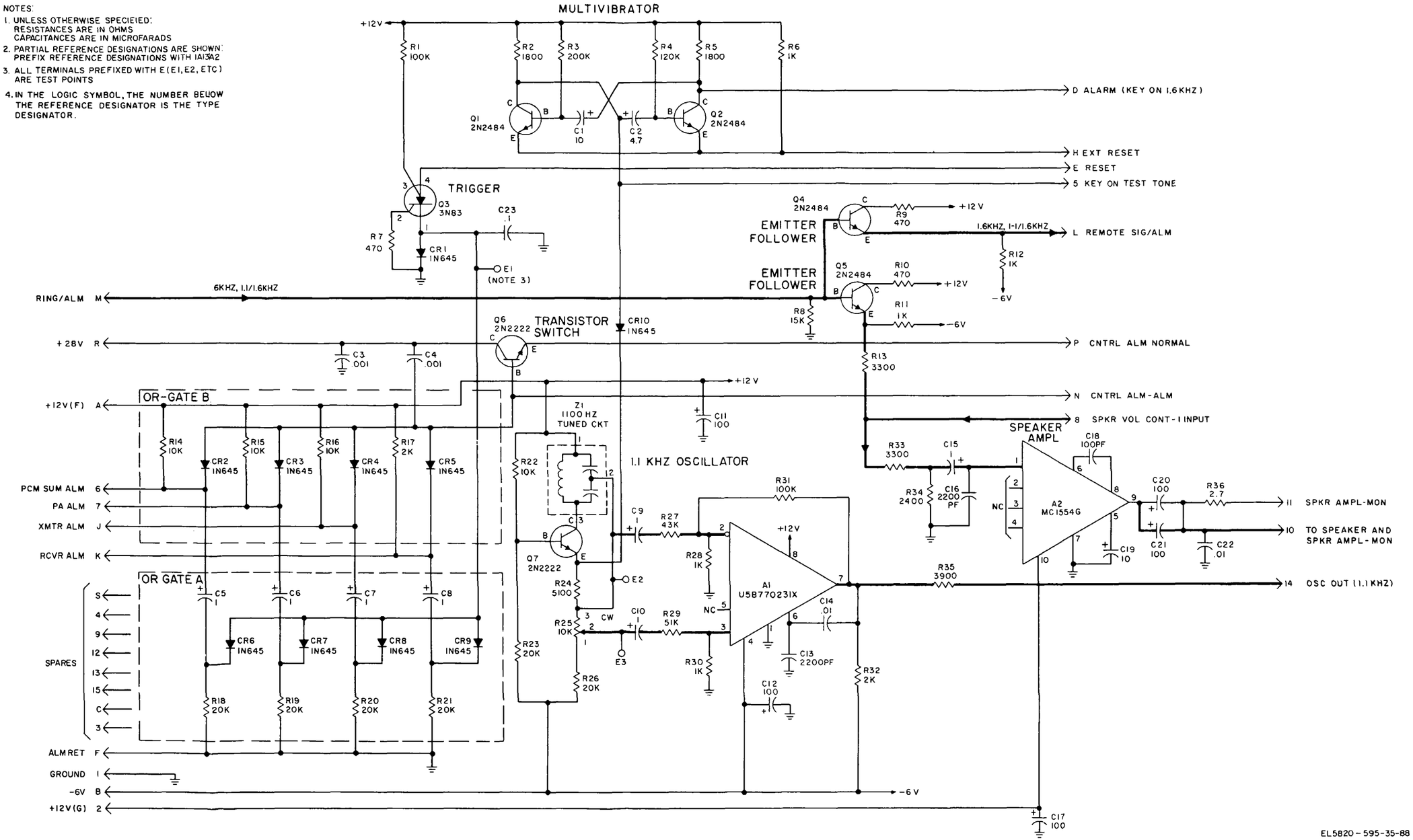


Figure 8-37. Board No. 2, 1A13A2, schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 1A13A3.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.)
   ARE TEST POINTS.
4. RELAY K1 SHOWN IN DE-ENERGIZED POSITION.
5. IN THE LOGIC SYMBOL, THE NUMBER BELOW
   THE REFERENCE DESIGNATOR IS THE TYPE
   DESIGNATOR.

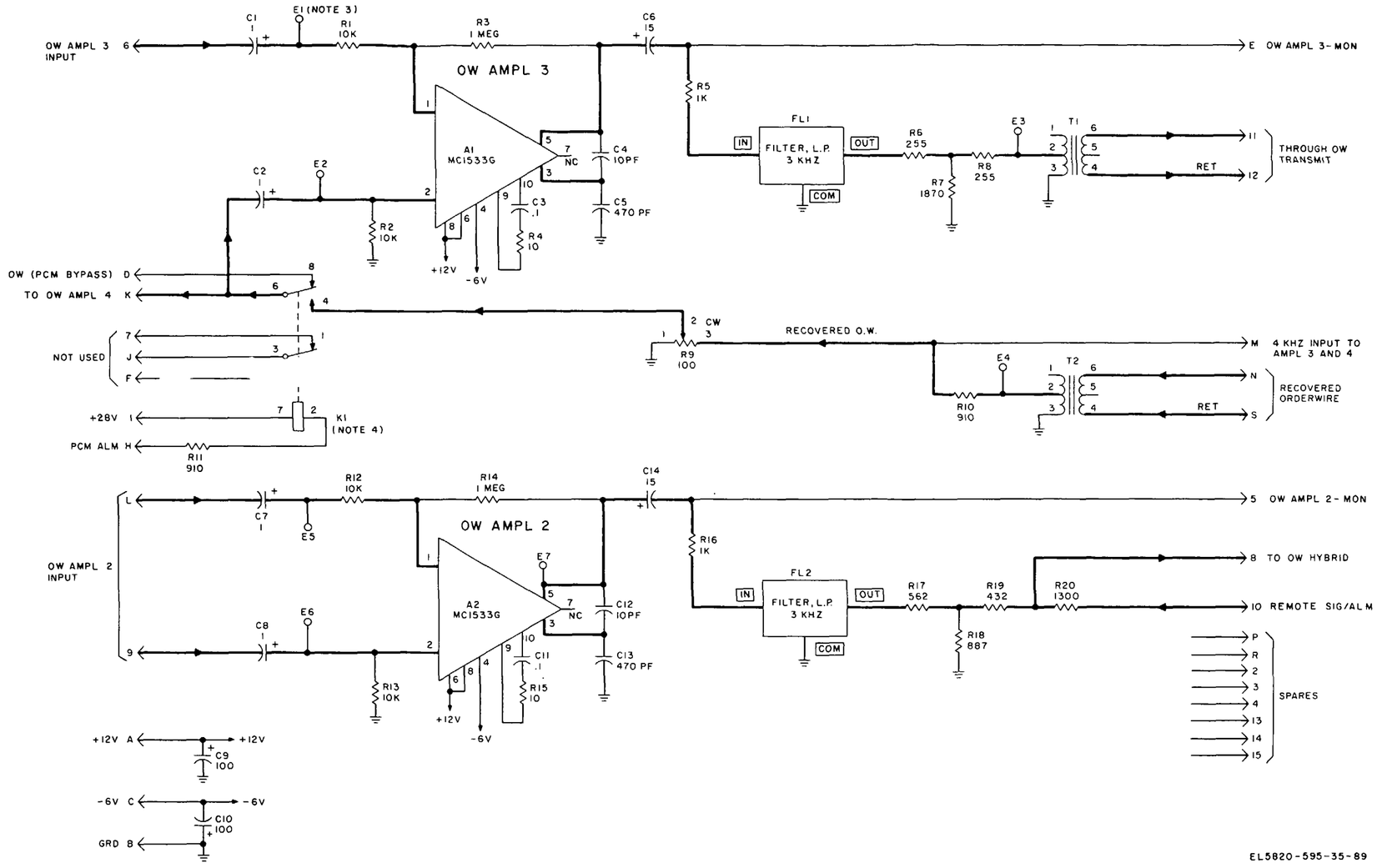


Figure 8-38. Board No. 3, 1A13A3, schematic diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS; CAPACITANCES MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX REFERENCE DESIGNATIONS WITH 1A13A4.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC) ARE TEST POINTS.
4. RELAY K1 SHOWN IN DE-ENERGIZED POSITION.
5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS THE TYPE DESIGNATOR.

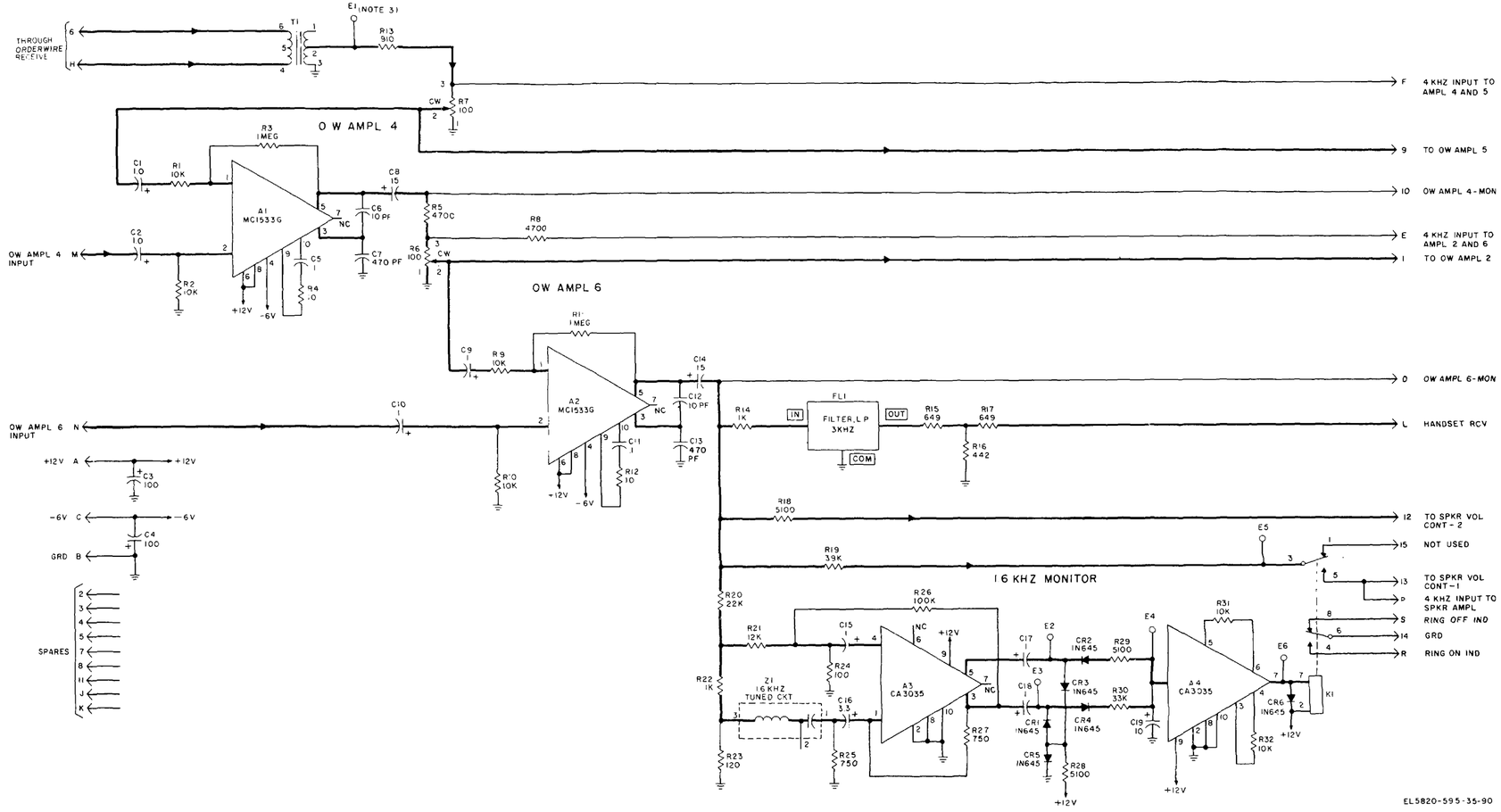


Figure 8-39. Board No. 4, 1A13A4, schematic diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
   PREFIX REFERENCE DESIGNATIONS WITH 1A13A5.
3. ALL TERMINALS PREFIXED WITH E (E1, E2, ETC.)
   ARE TEST POINTS.
4. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE
   REFERENCE DESIGNATOR IS THE TYPE DESIGNATOR.

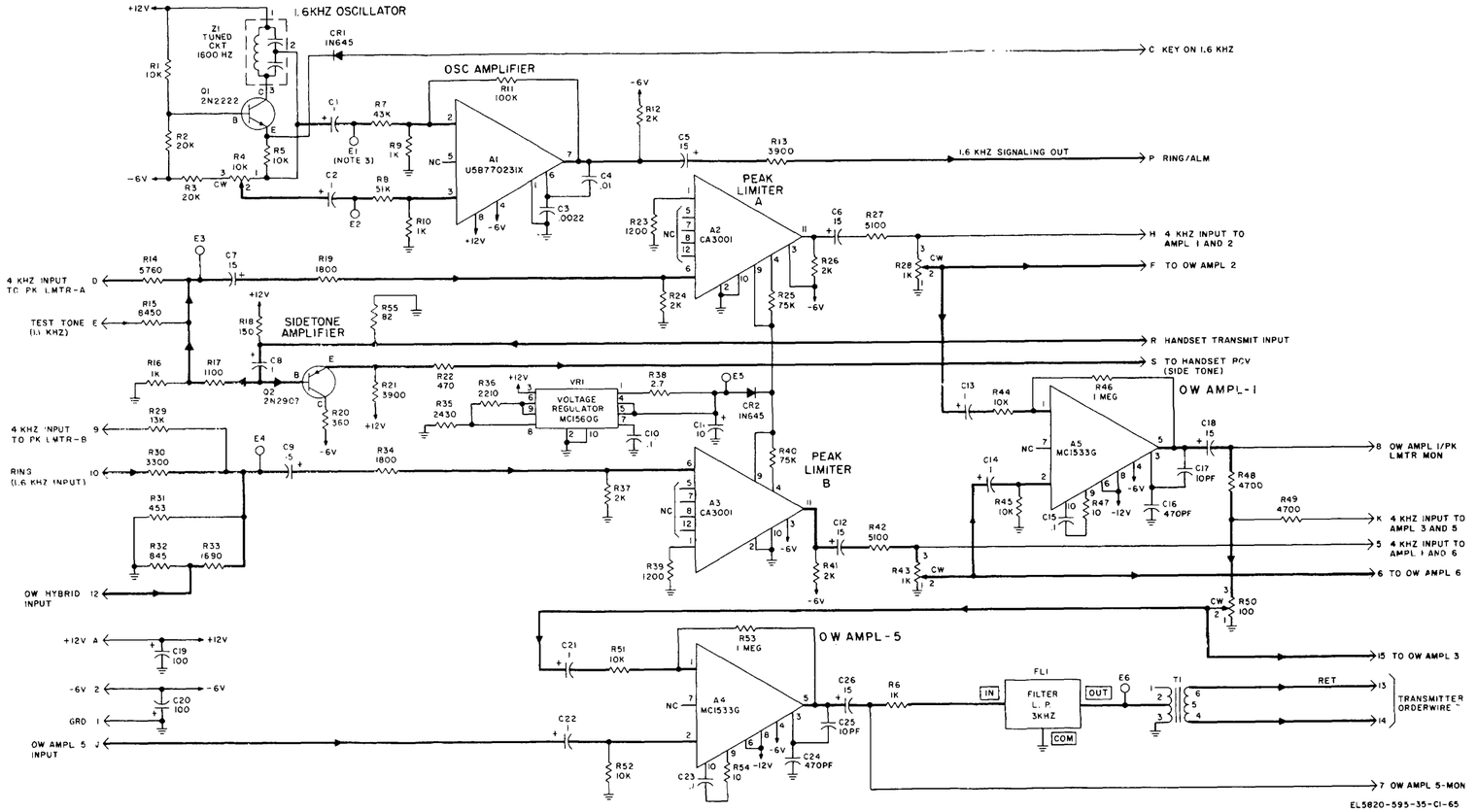


Figure 8-40. Board No 5, 1A13A5, schematic diagram.

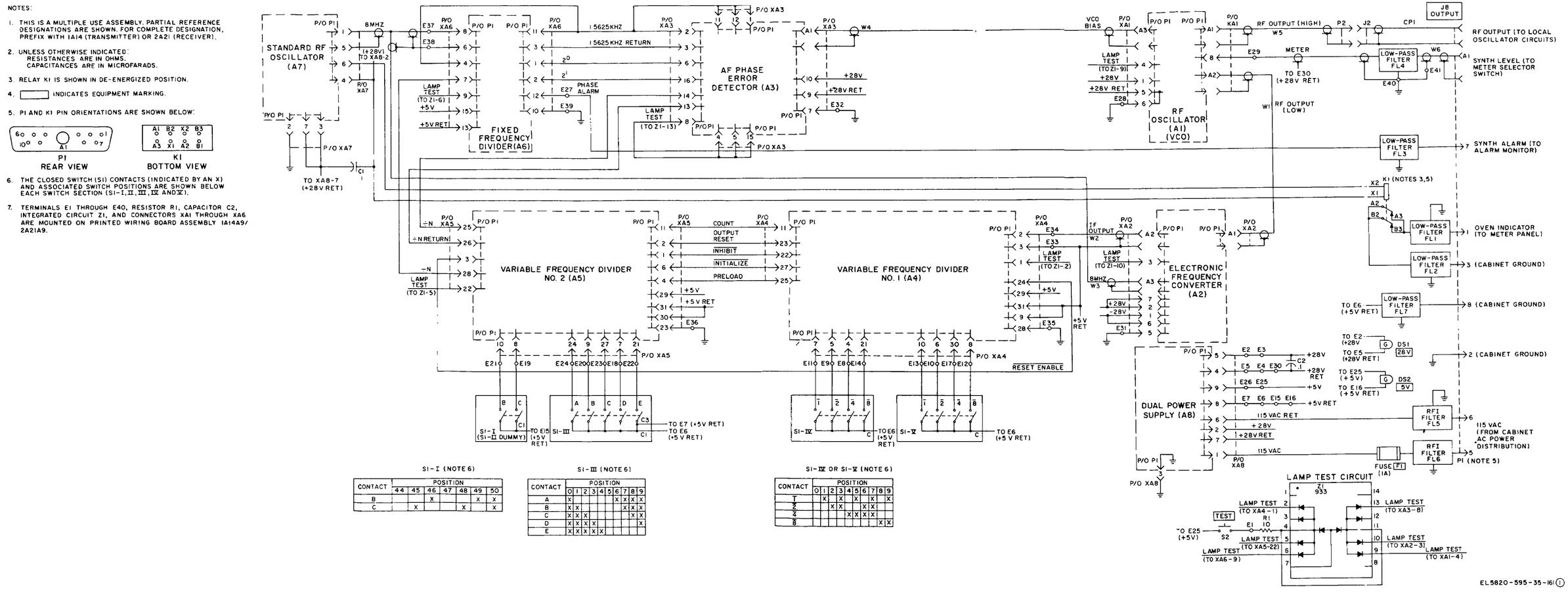


Figure 8-41 (1). Frequency synthesizer 1A14/2A21, interconnecting diagram (part 1 of 3).

NOTES:
1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT, UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO 26 AWG. UNLESS SPECIFIED AS NO. 22 AWG

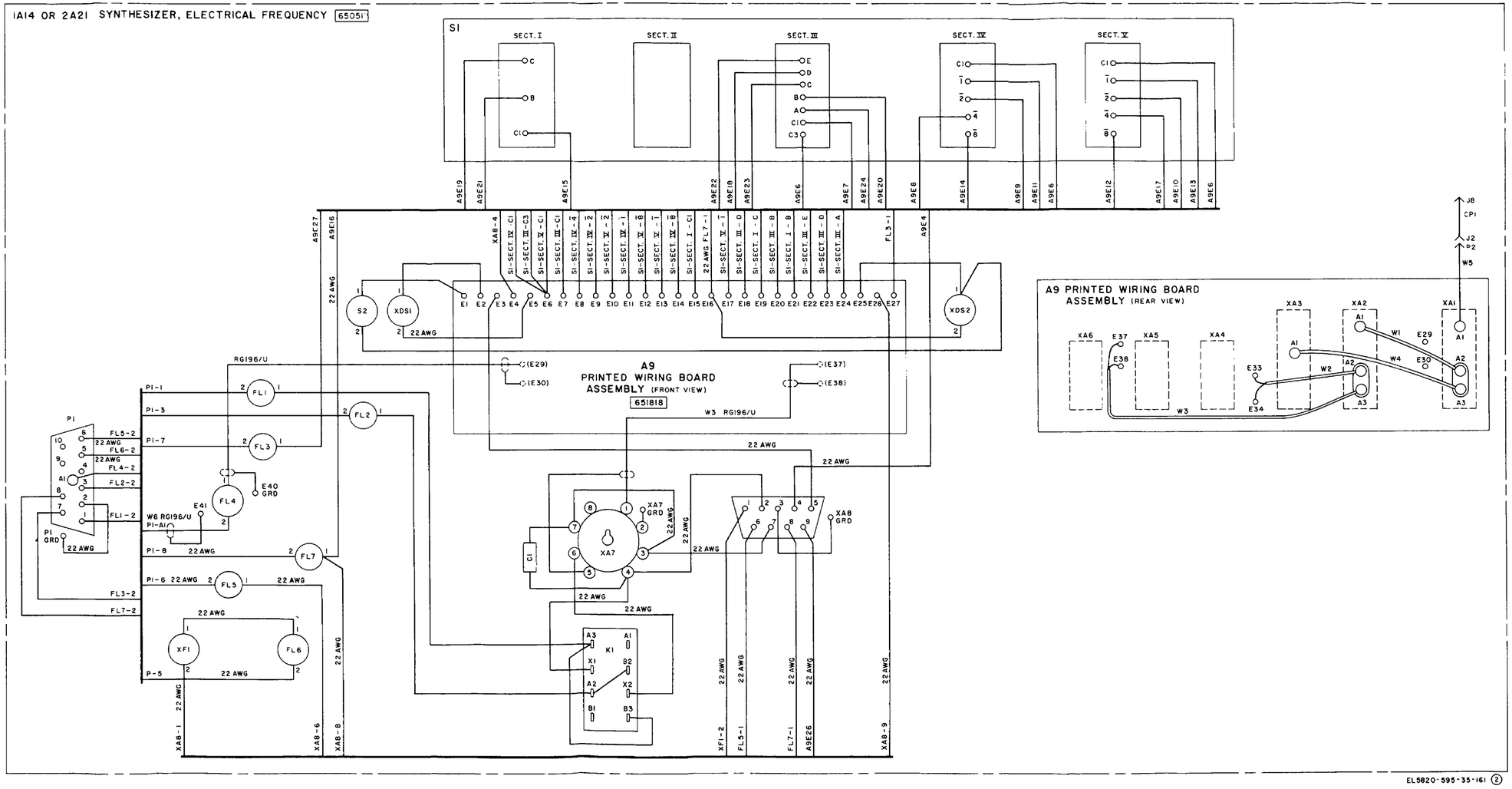
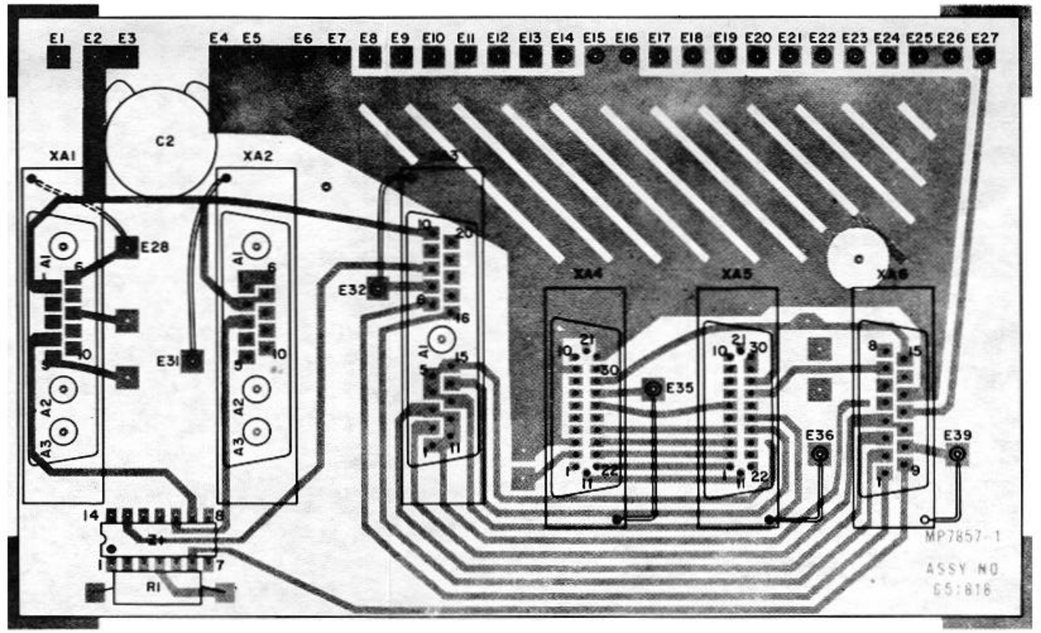


Figure 8-41 (2). Frequency synthesizer 1A14/2A21, interconnecting diagram (part 2 of 3).



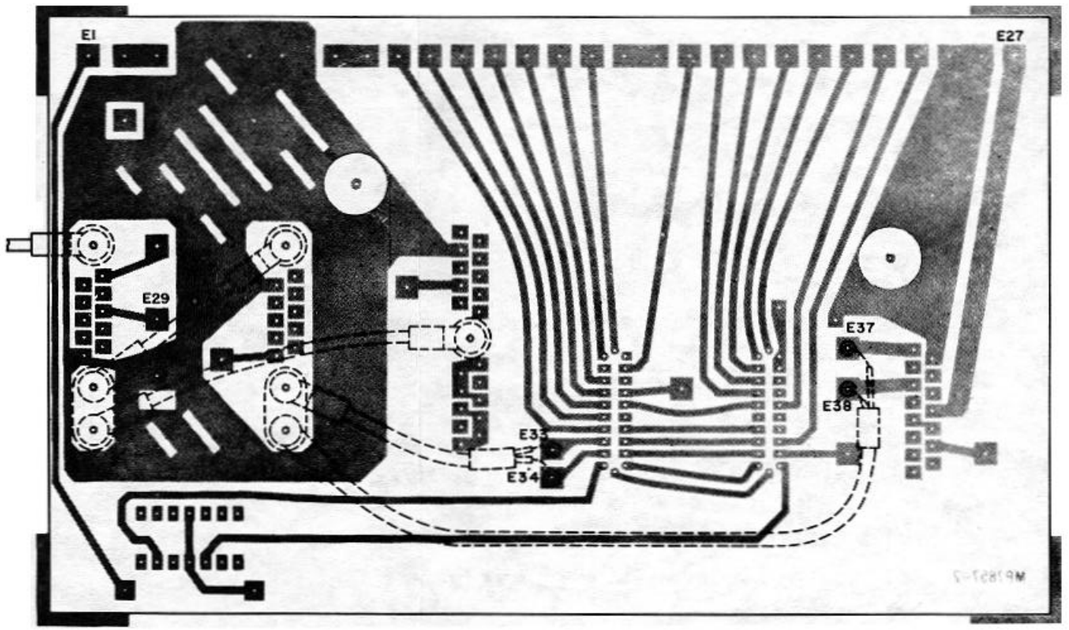


Figure 8-41 (3). Frequency synthesizer 1A14/2A21, interconnecting diagram (part 3 of 3).

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN PICOFARADS
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A14A1 (TRANSMITTER) OR 2A21A1 (RECEIVER).
3. VALUES FOR RESISTORS R20 AND R33 ARE DETERMINED DURING FINAL TESTS.
4. SPARE TERMINALS P1-2, P1-3, P1-7, P1-9 AND P1-10.

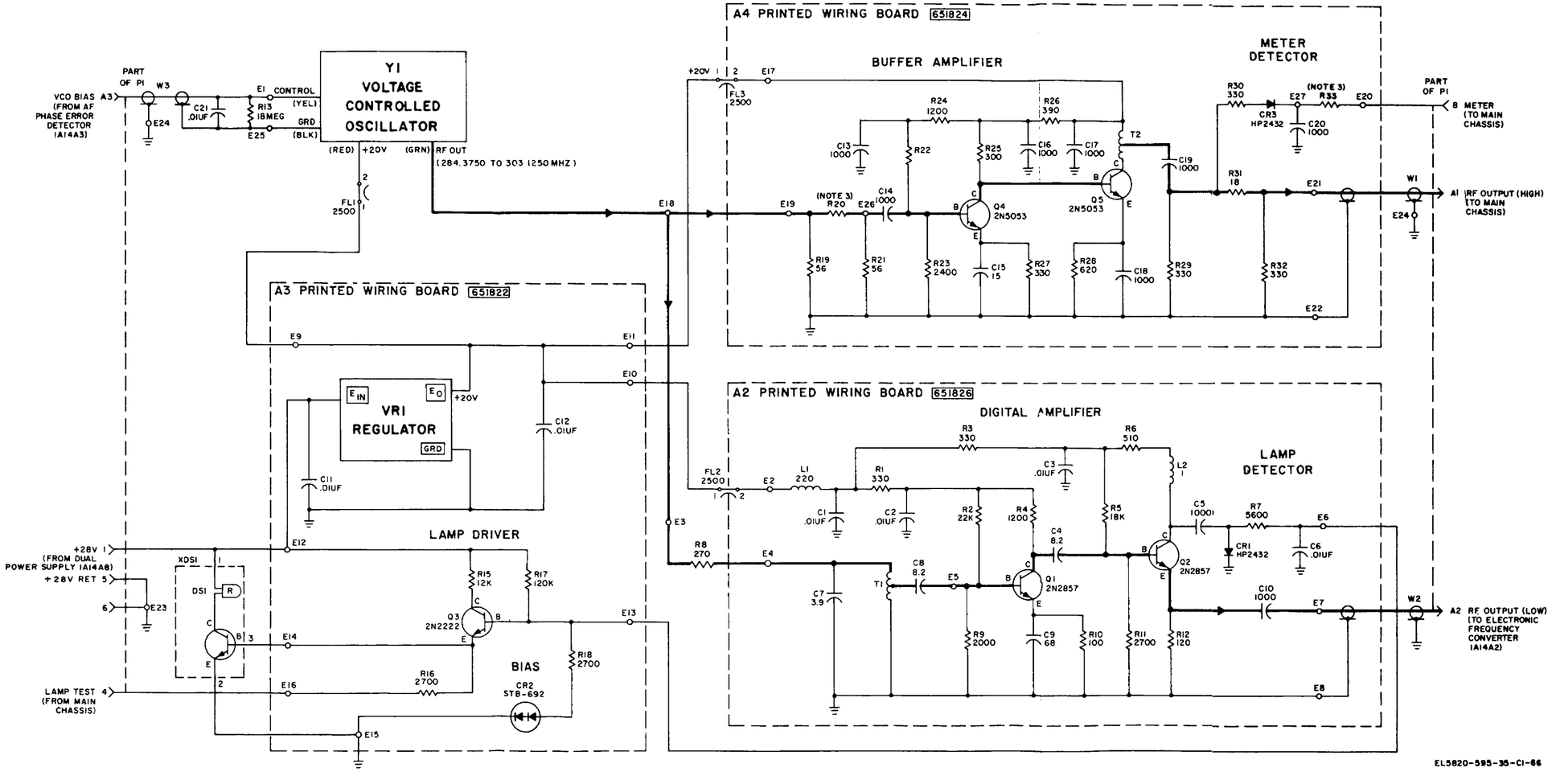


Figure 8-42. RF oscillator 1A14A1, schematic diagram.

Change 1

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS,
   CAPACITANCES ARE IN MICROFARADS.
   INDUCTANCES ARE IN MICROHENRIES.

2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A1A2 (TRANSMITTER) OR 2A2A2 (RECEIVER).

3. VALUE FOR RESISTOR R22 IS DETERMINED DURING FINAL TEST.

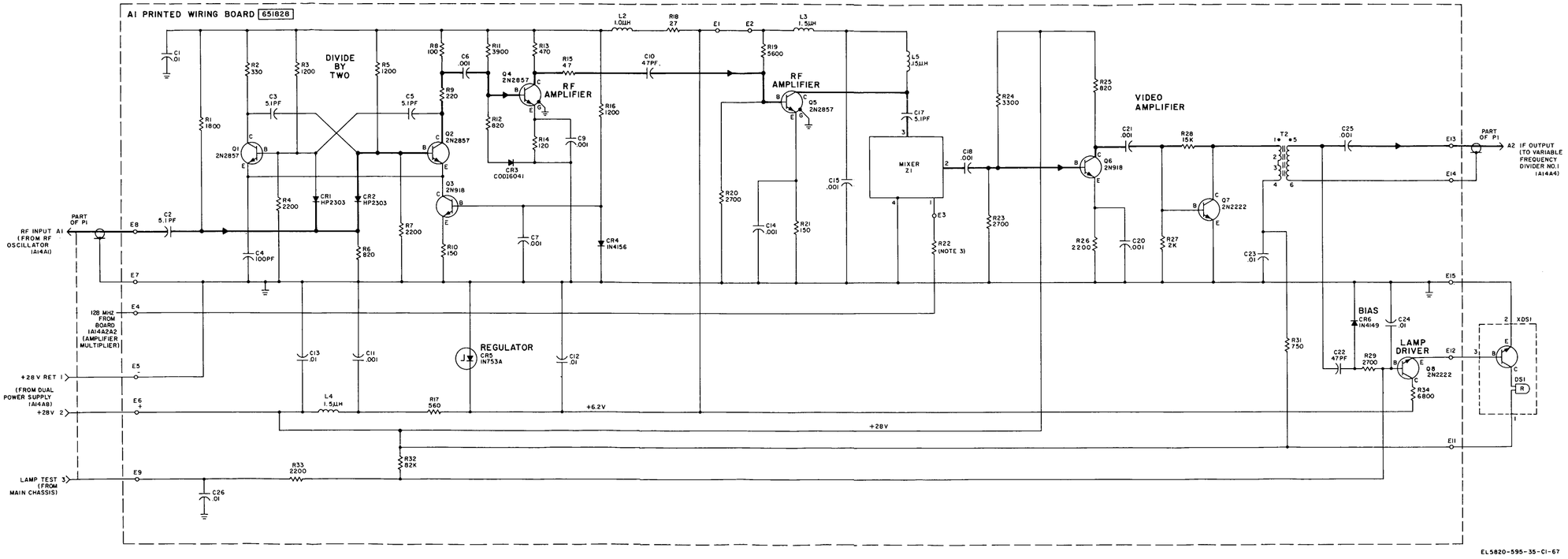
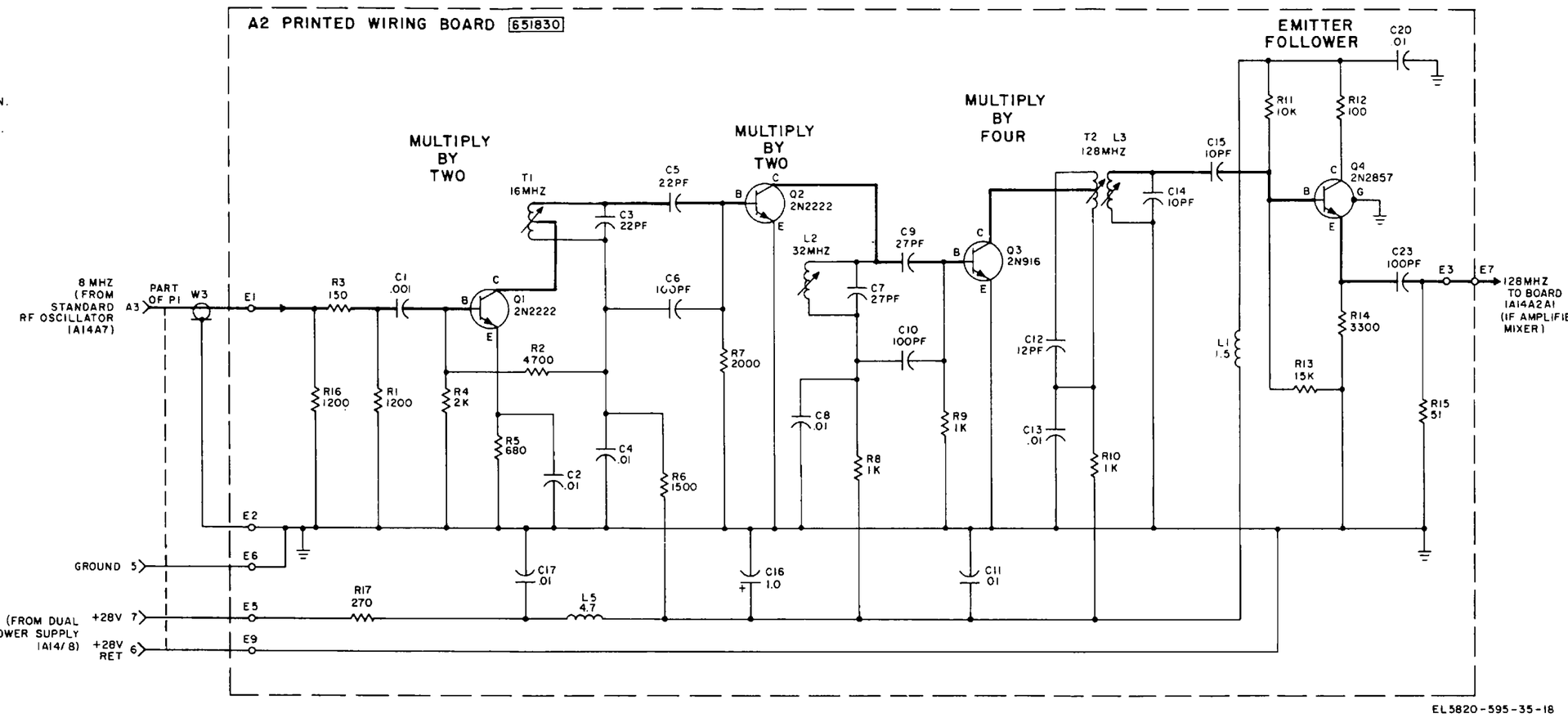


Figure 8-43. Electronic frequency converter board 1A4A2A1, schematic diagram.

Change 1

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS,
   CAPACITANCES ARE IN MICROFARADS,
   INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A14A2 (TRANSMITTER) OR 2A21A2 (RECEIVER).



EL5820-595-35-18

Figure 8-44. Electronic frequency converter board 1A14A2A2, schematic diagram.

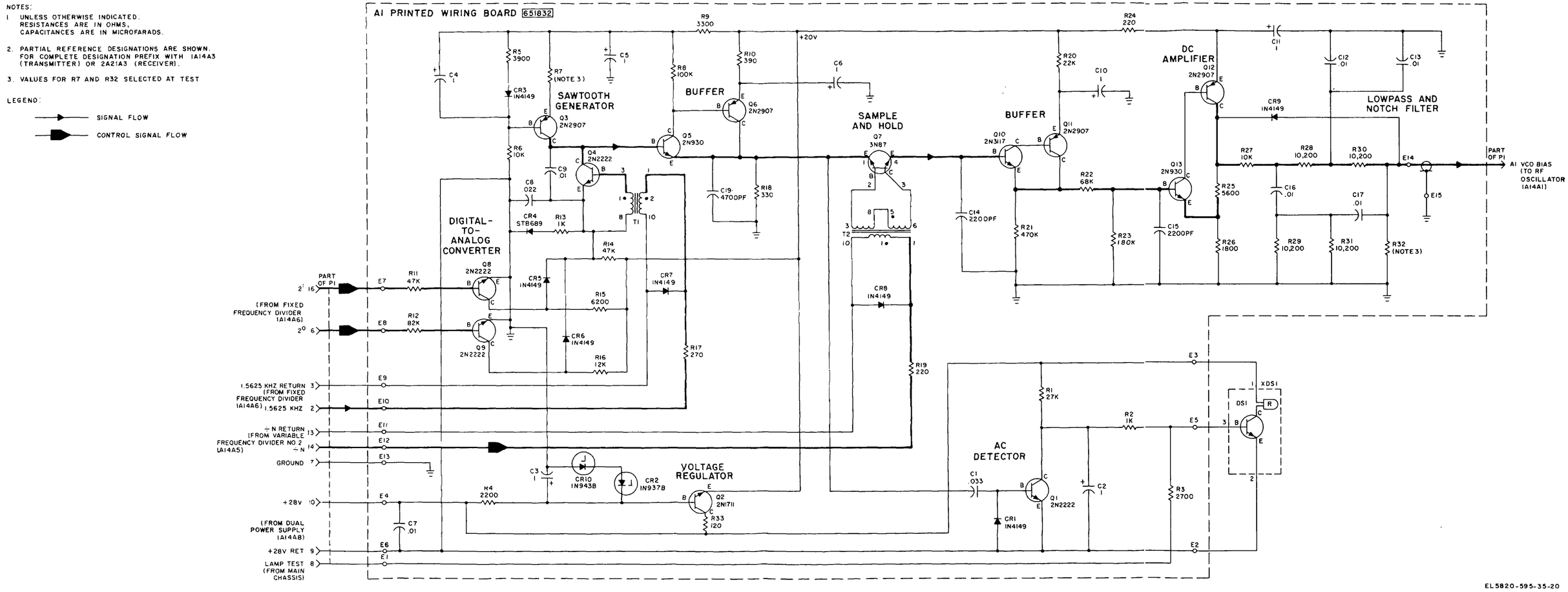


Figure 8-45. AF phase error detector 1A14A3, schematic diagram.

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS,
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A1A4 (TRANSMITTER) OR 2A2A4 (RECEIVER).
3. PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS; .
   PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO GROUND.
4. INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

Z1	MSC6847L	Z10	MIC950-1D
Z2	SL50604	Z11	MIC963-1D
Z3	MIC932-1D	Z12	MIC950-1D
Z4	MIC963-1D	Z13	MIC950-1D
Z5	MSC6847L	Z14	SL50604
Z6	MSC6847L	Z15	MIC950-1D
Z7	MSC6847L	Z16	MIC949-1D
Z8	MIC950-1D	Z17	MIC950-1D
Z9	MIC949-1D	Z18	MIC950-1D

5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

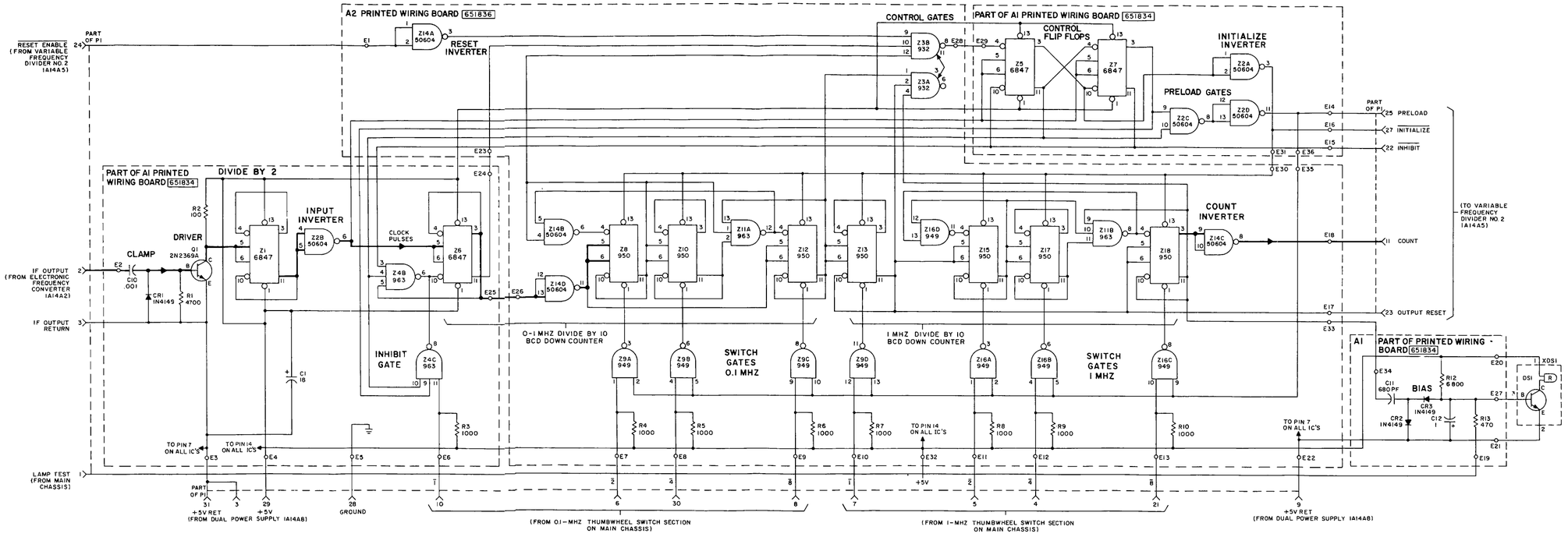


Figure 8-46. Variable frequency divider No. 1, 1A14A4, schematic diagram.

Change 1

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A14A5 (TRANSMITTER) OR 2A21A5 (RECEIVER).
3. PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS; PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO GROUND.
4. INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

Z1	MIC932-1D	Z8	MIC950-1D
Z2	MIC950-1D	Z9	MIC950-1D
Z3	MIC950-1D	Z10	MIC950-1D
Z4	MIC950-1D	Z11	—
Z5	MIC950-1D	Z12	MIC946-1D
Z6	MIC950-1D	Z13	MIC946-1D
Z7	MIC950-1D	Z14	MIC946-1D

5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION CONTROL DRAWING SM-C-653451.

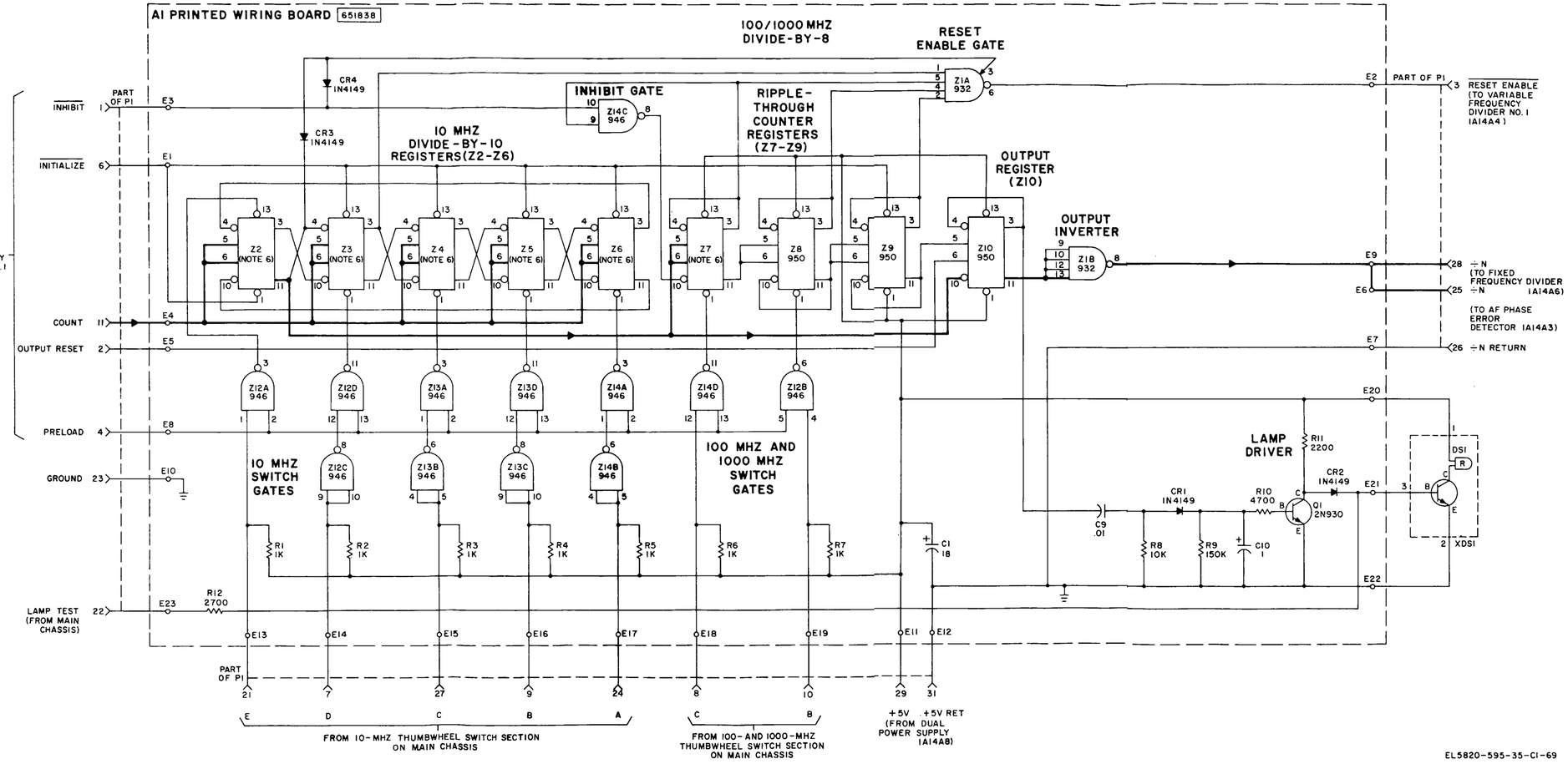


Figure 8-47. Variable frequency divider No. 2, 1A14A5, schematic diagram.

Change 1

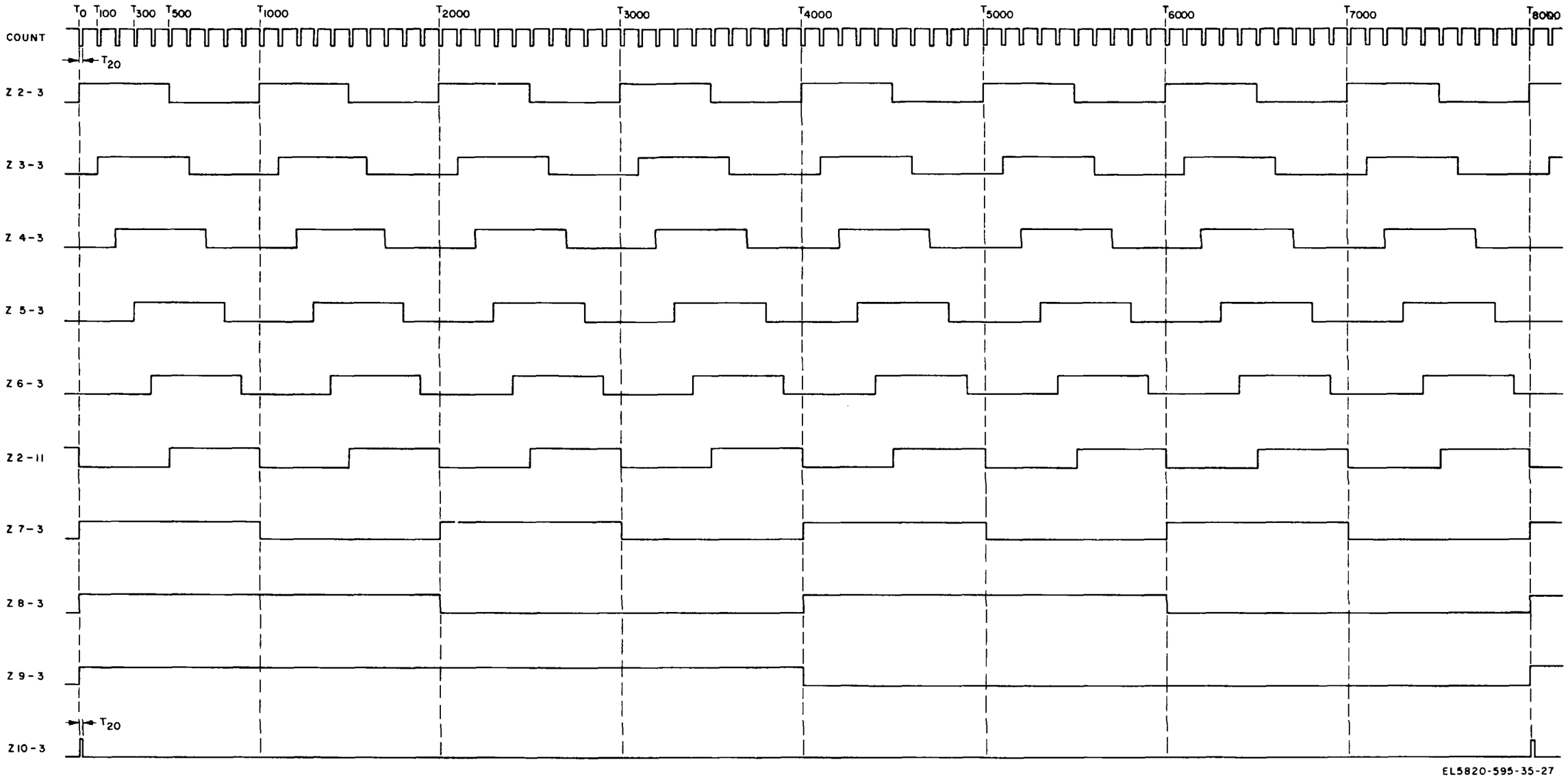


Figure 8-48. Variable frequency divider No. 2, 1A14A5, timing without jump count.

NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTANCES ARE IN OHMS,
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH A14A6 (TRANSMITTER) OR 2A2A6 (RECEIVER).
3. PIN 14 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO +5 VOLTS. PIN 7 ON EACH INTEGRATED CIRCUIT IS CONNECTED TO GROUND.
4. INTEGRATED CIRCUIT TYPES ARE LISTED IN TABLE.

Z1	MIC950-1D	Z13	MIC950-1D
Z2	MIC950-1D	Z14	MIC950-1D
Z3	MIC950-1D	Z15	U6A900251X
Z4	MIC950-1D	Z16	MIC946-1D
Z5	MIC950-1D	Z17	MIC950-1D
Z6	MIC950-1D	Z18	MIC946-1D
Z7	MIC950-1D	Z19	MIC950-1D
Z8	MIC950-1D	Z20	MIC950-1D
Z9	MIC950-1D	Z21	MIC950-1D
Z10	MIC950-1D	Z22	MIC950-1D
Z11	MIC950-1D	Z23	MIC950-1D
Z12	MIC950-1D	Z24	MIC932-1D

5. IN THE LOGIC SYMBOL, THE NUMBER BELOW THE REFERENCE DESIGNATOR IS PART OF THE TYPE DESIGNATOR.

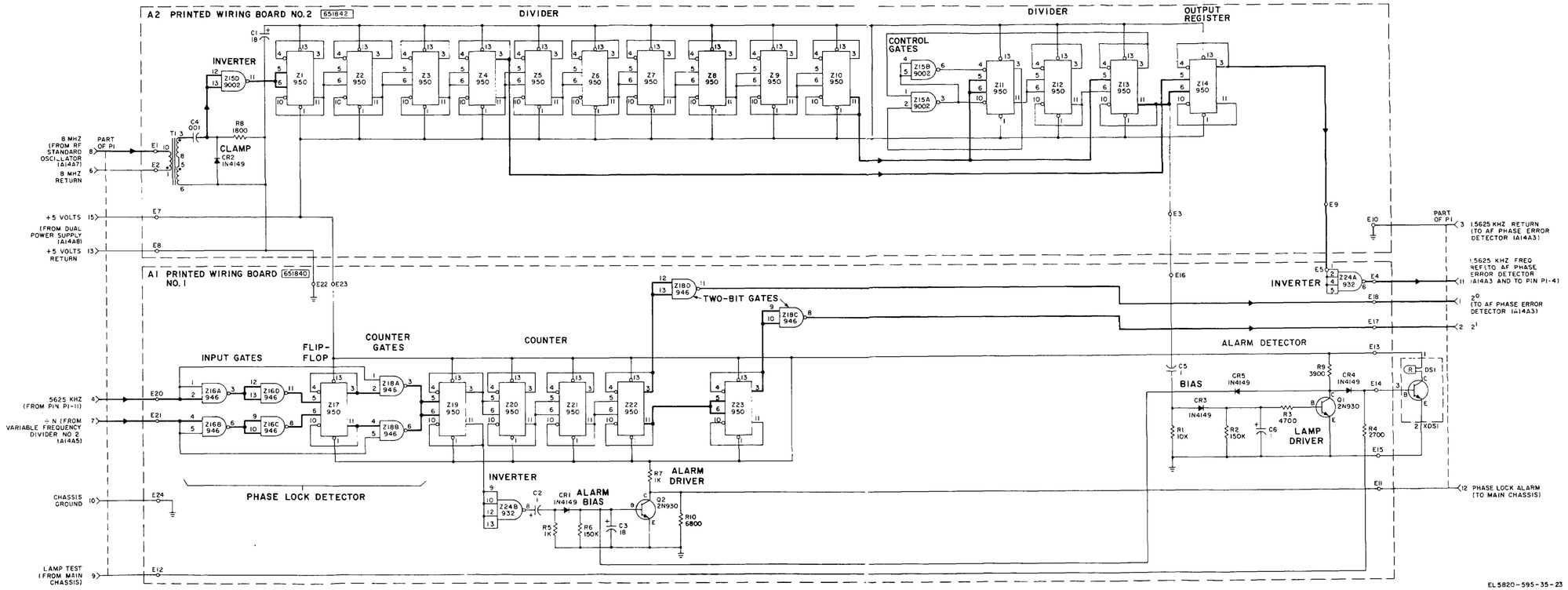


Figure 8-49. Fixed frequency divider 1A14A6, schematic diagram.

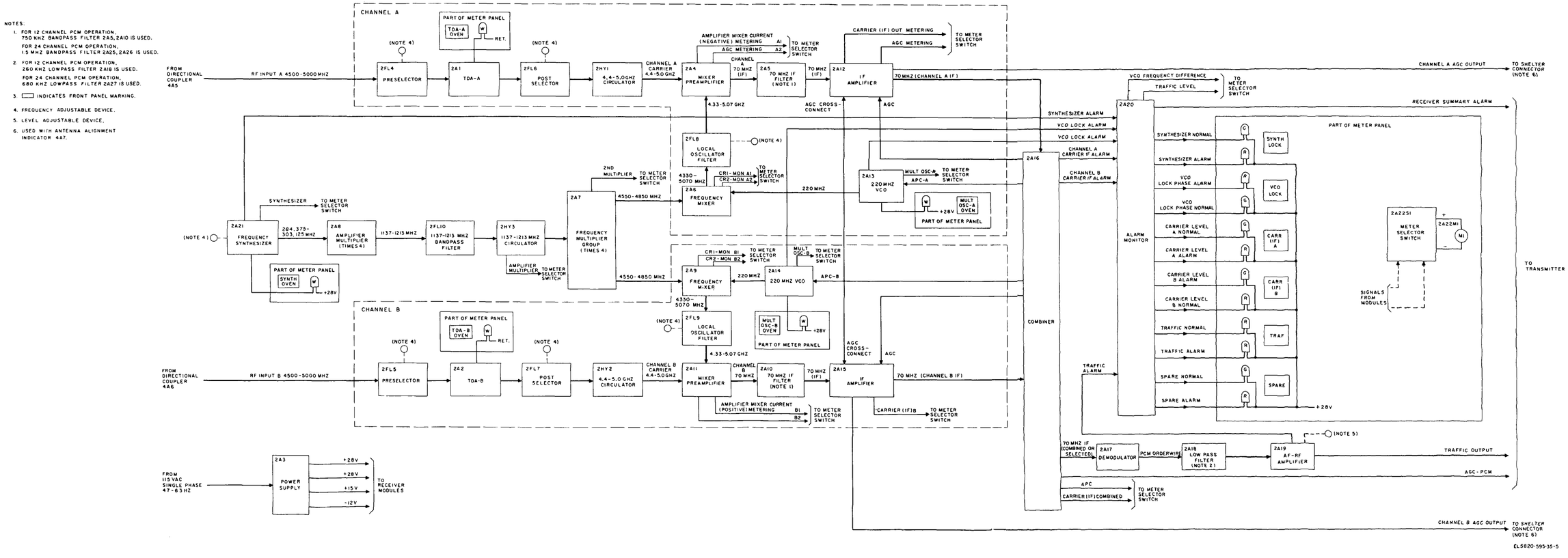


Figure 8-50. Receiver block diagram.

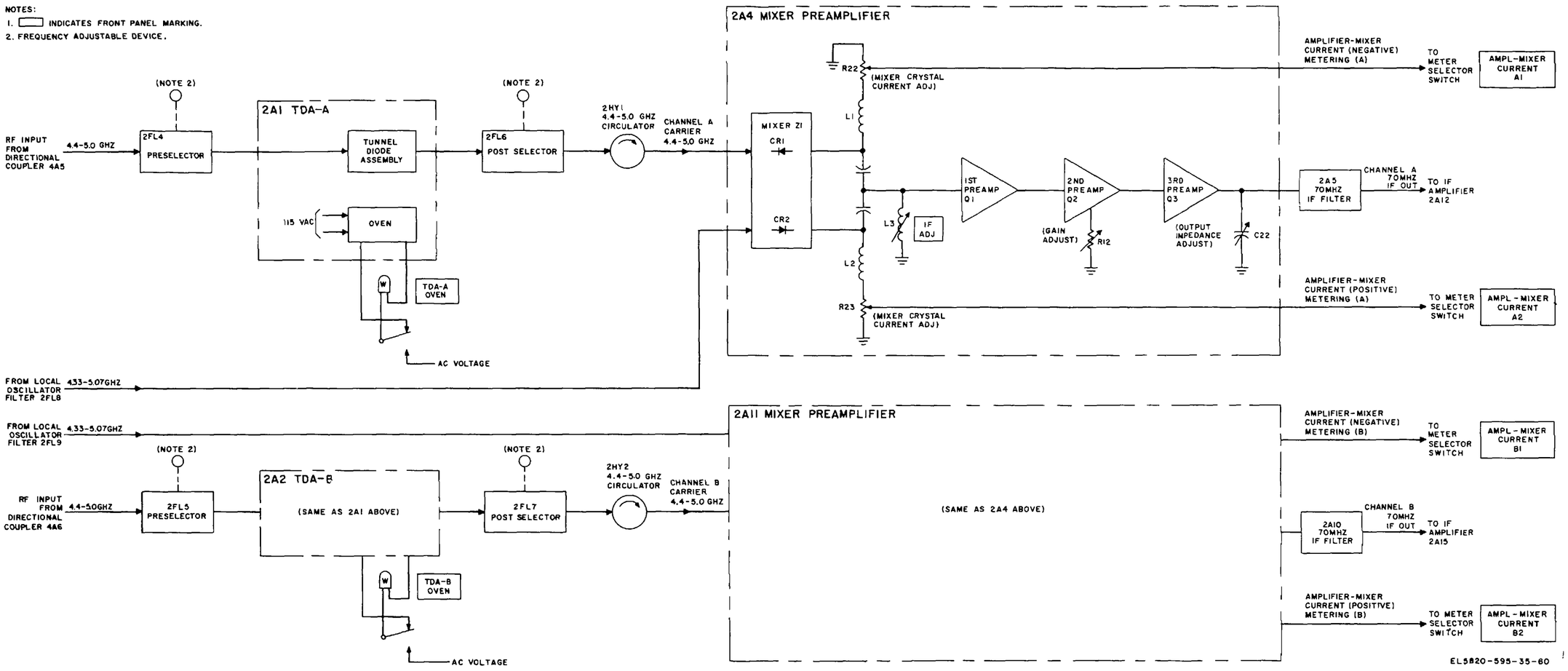


Figure 8-51. Receiver RF input and mixer circuits, block diagram.

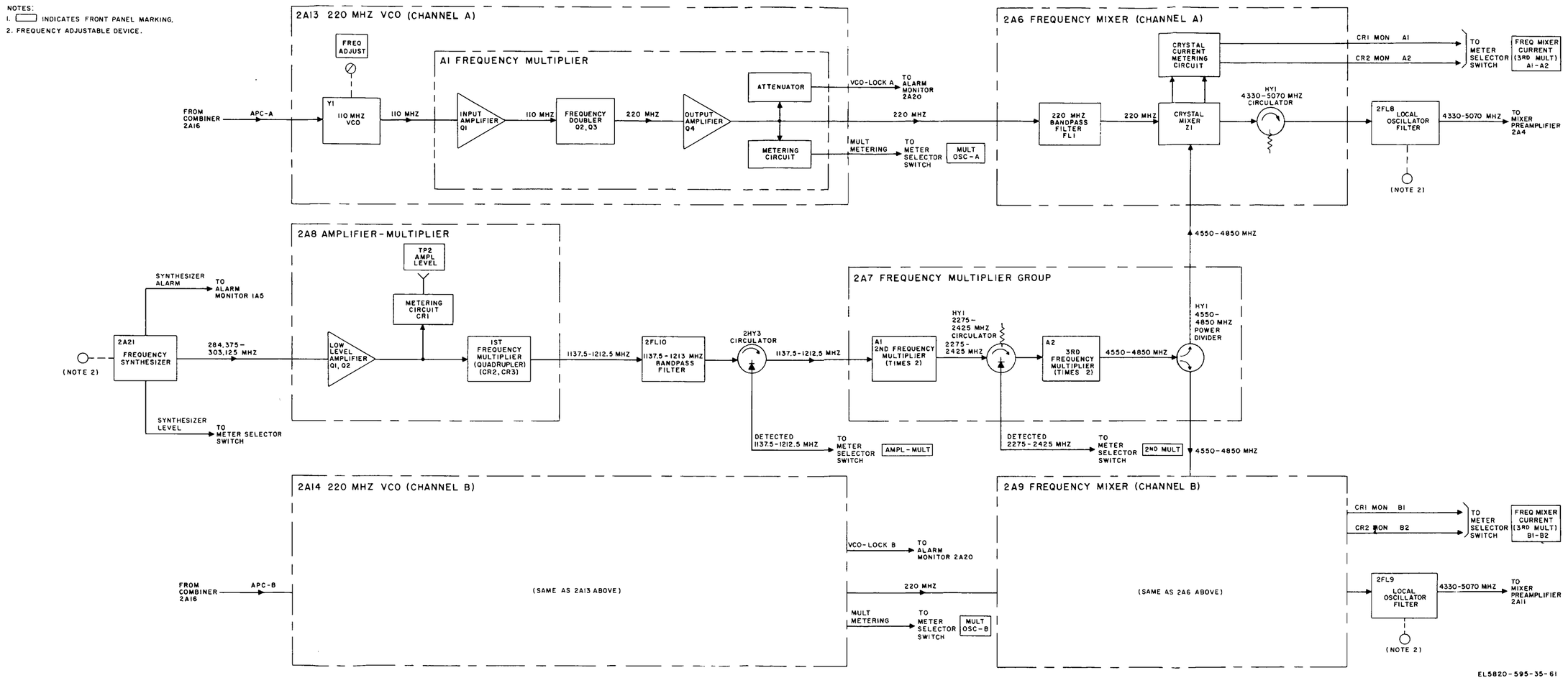


Figure 8-52. Receiver local oscillator circuits, block diagram.

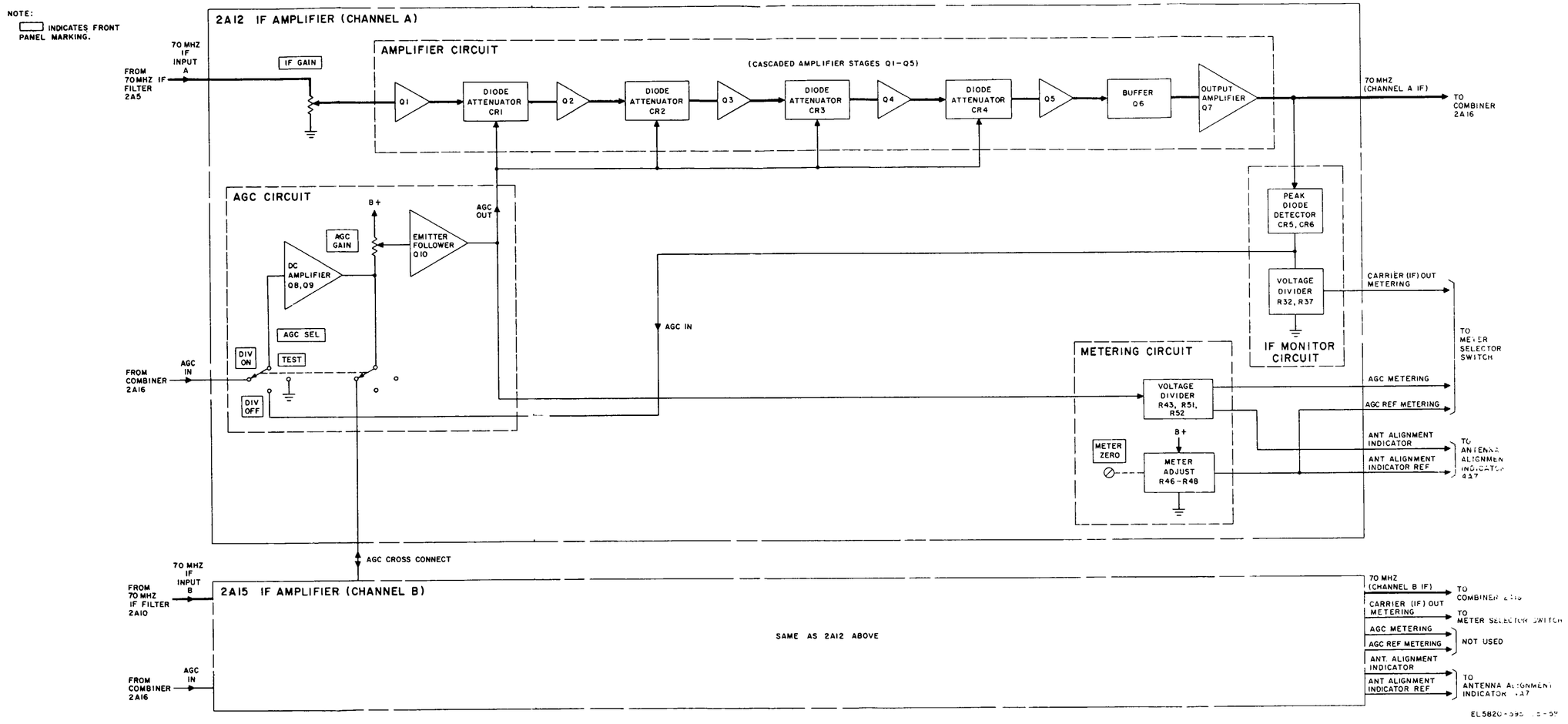


Figure 8-53. IF amplifiers 2A12 and 2A15, block diagram.

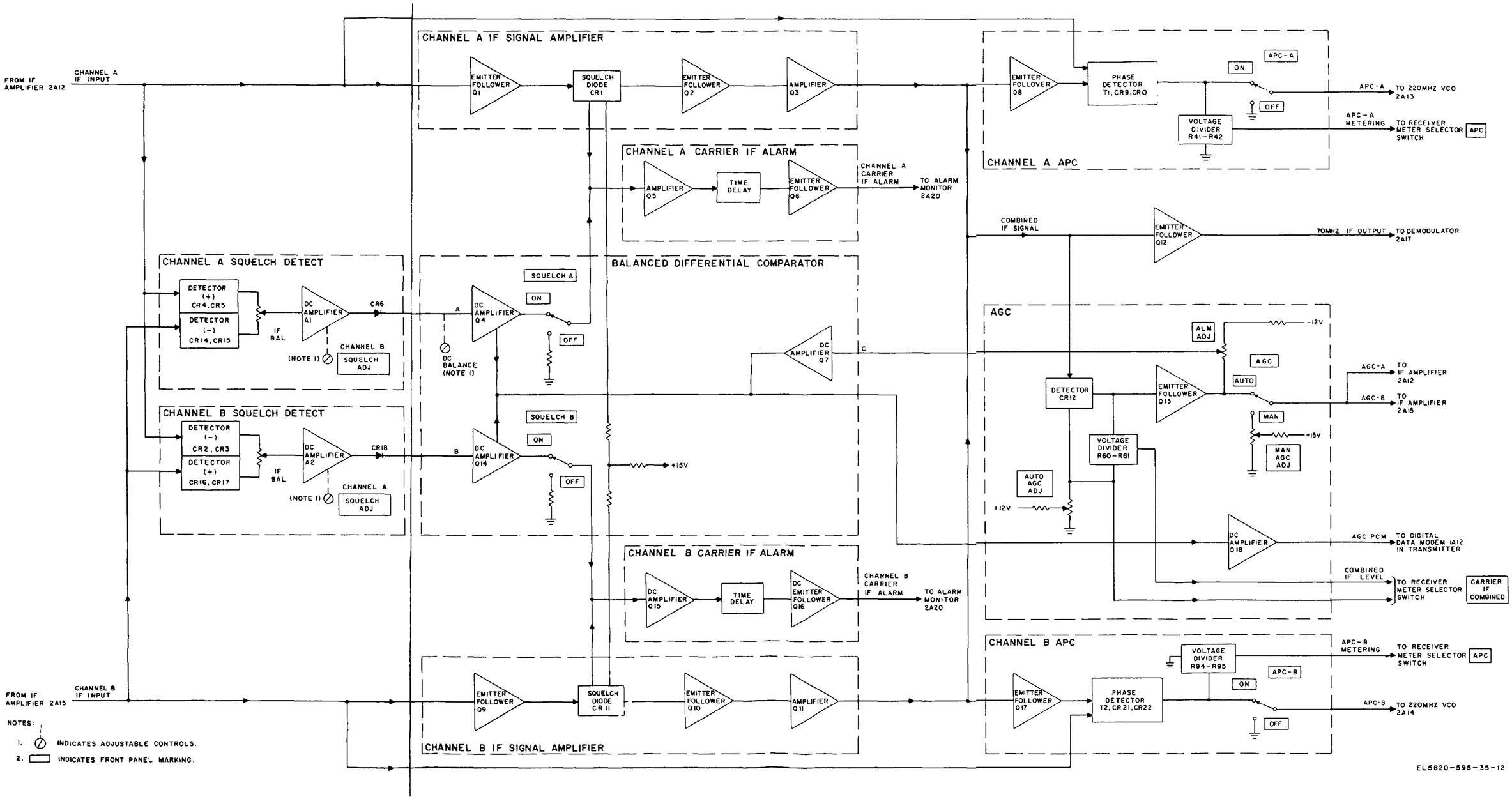


Figure 8-54. Combiner 2A16, block diagram.

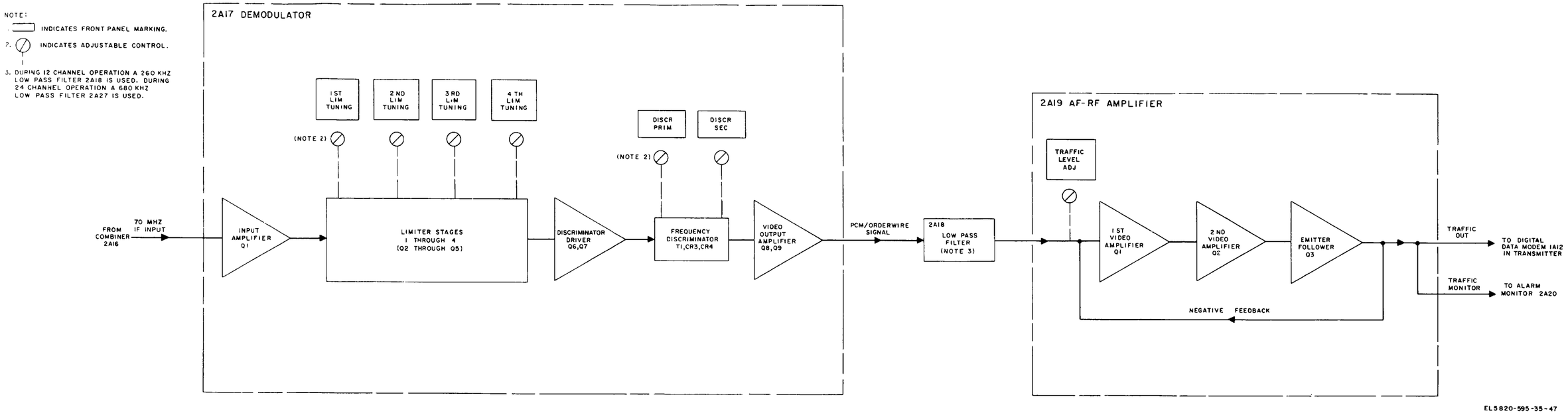


Figure 8-55. Receiver demodulator and amplifier circuits, block diagram.

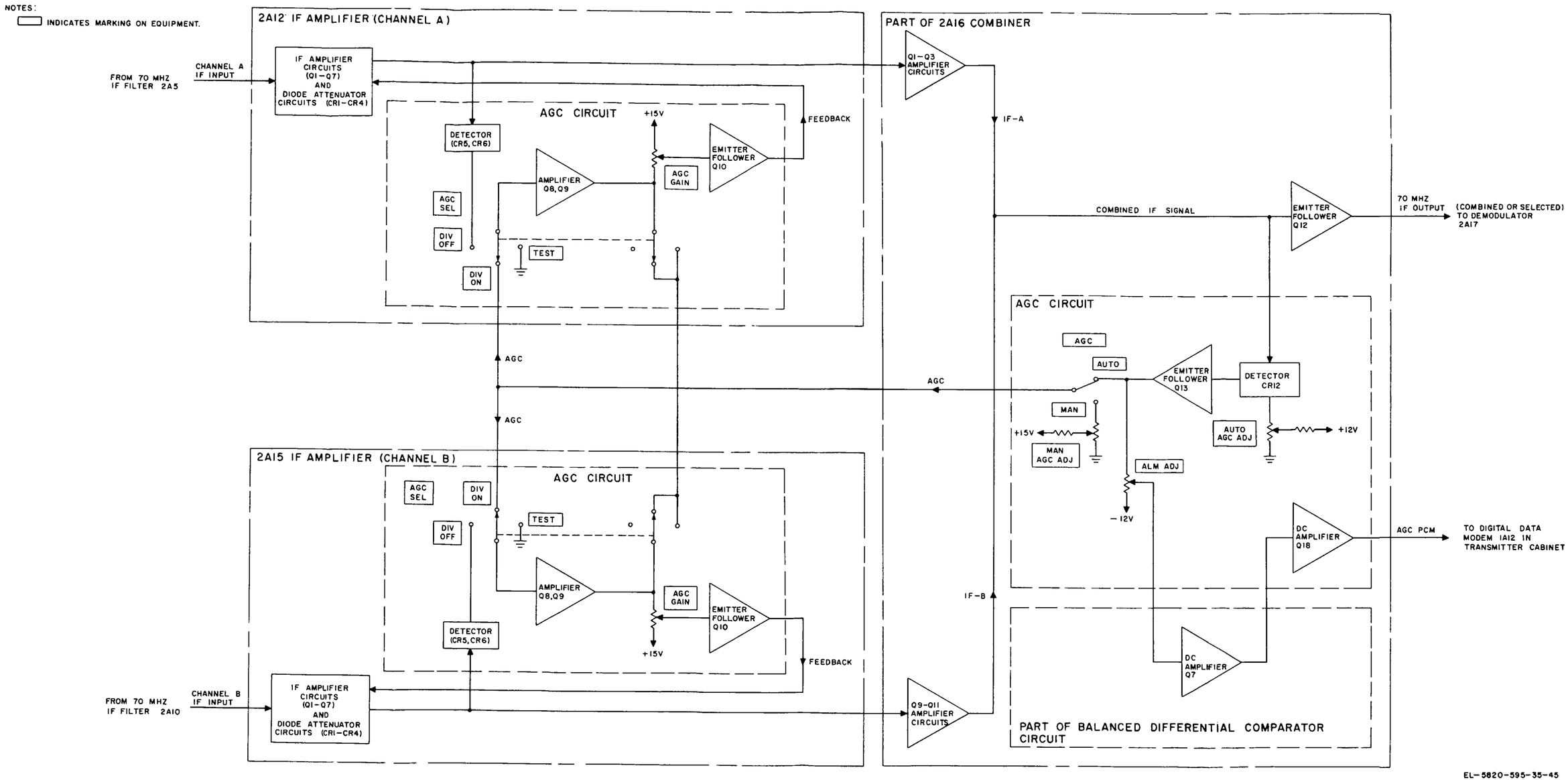


Figure 8-56. Receiver agc function, block diagram.

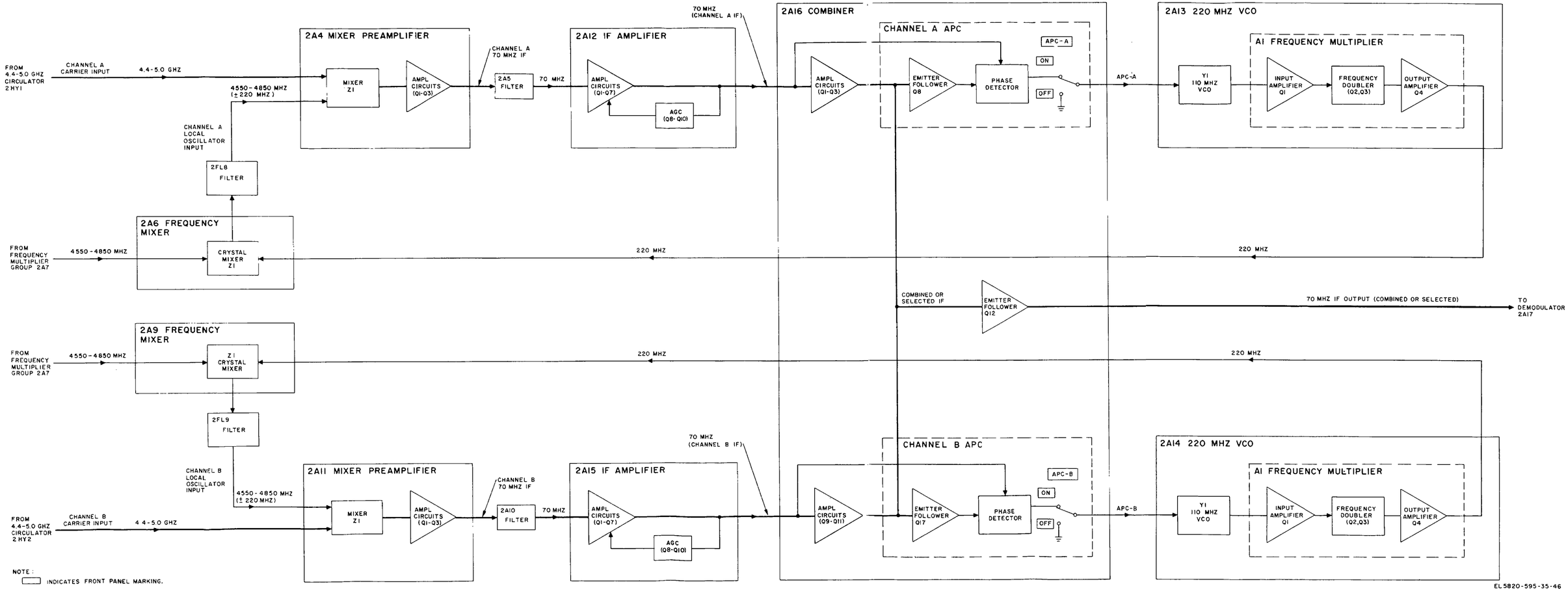


Figure 8-57. Receiver apc function, block diagram.

NOTES:

▭ INDICATES FRONT PANEL MARKING.

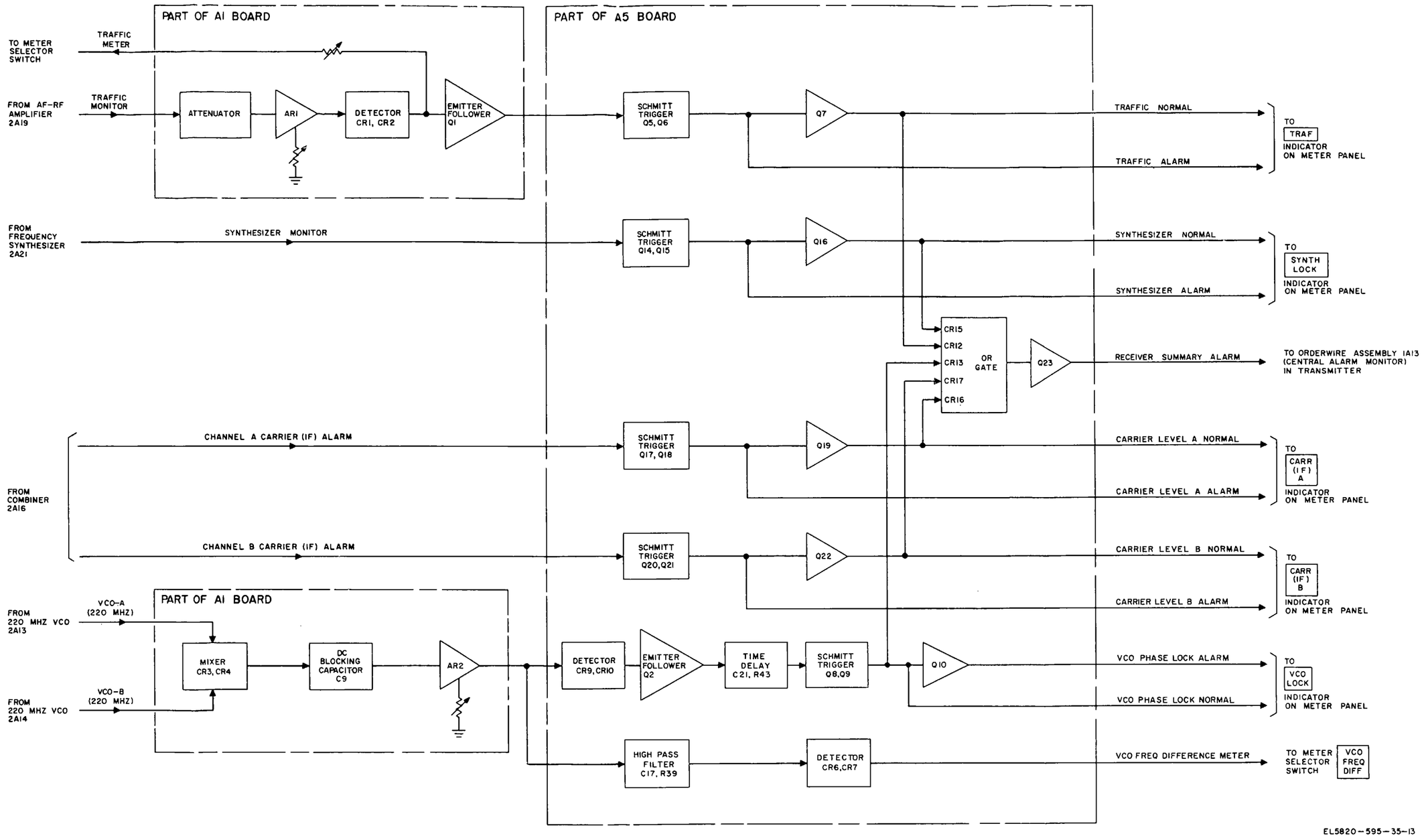


Figure 8-58. Alarm monitor 2A20, block diagram.

UNIT 2,
RECEIVER, RADIO R-1287/GRC-143

NOTES:

1 UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS.

2 CIRCUIT REFERENCES NOT SHOWN
2A22 CABINET, ELECTRICAL EQUIPMENT (143 DUAL RECEIVER).
2A24 PLATE ASSEMBLY, DUAL RECEIVER
2A22W1 WIRING HARNESS, BRANCHED (RCVR CAB).
2A24W1 WIRING HARNESS, BRANCHED (RCVR PLATE).

3 TERMINALS INDICATED ARE USED FOR INTERNAL MODULE CONNECTIONS DO NOT CONNECT EXTERNALLY.

4 UNLESS OTHERWISE SPECIFIED ALL WIRE SHALL BE STRANDED, TEFLON INSULATED, SIZES AS FOLLOWS:
NO 16 AWG FOR 115V AC POWER
NO 20 AWG FOR LOW VOLTAGE AC AND DC, AND GROUND.
NO 22 AWG FOR ALL OTHER WIRING.

5 CONTACT ARRANGEMENTS FOR VARIOUS CONNECTORS ARE SHOWN ON TABLE I.
PINS A1, A2, A3 ARE COAX CONTACTS.

6 USE FILTERS FOR 12 OR 24 CHANNEL OPERATION AS FOLLOWS.

OPERATION MODE	2A5 AND 2A10	2A18
12 CHANNEL	650525(8+750KHZ)	650519 (260KHZ)
24 CHANNEL	650538(8+1.5MHZ)	650537(680KHZ)

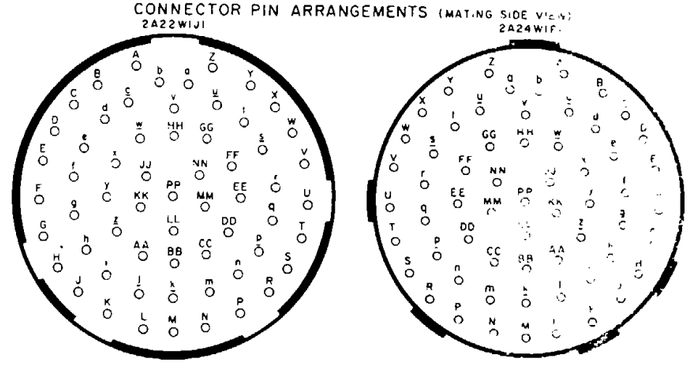
7 ▭ INDICATES MARKING ON EQUIPMENT

8 THE SYMBOL ⊸ P DENOTES TWISTED PAIR

9 SWITCH 2A22S1 IS VIEWED FROM END OPPOSITE CONTROL KNOB SECTION A IS CLOSEST TO KNOB

10 CONTROL, INDICATOR, AND SWITCH OUTLINES SHOWING TERMINAL LOCATIONS ARE PROVIDED BELOW ALL VIEWS ARE FROM WIRING SIDE

CONNECTOR PIN ARRANGEMENTS (MATING SIDE VIEW)



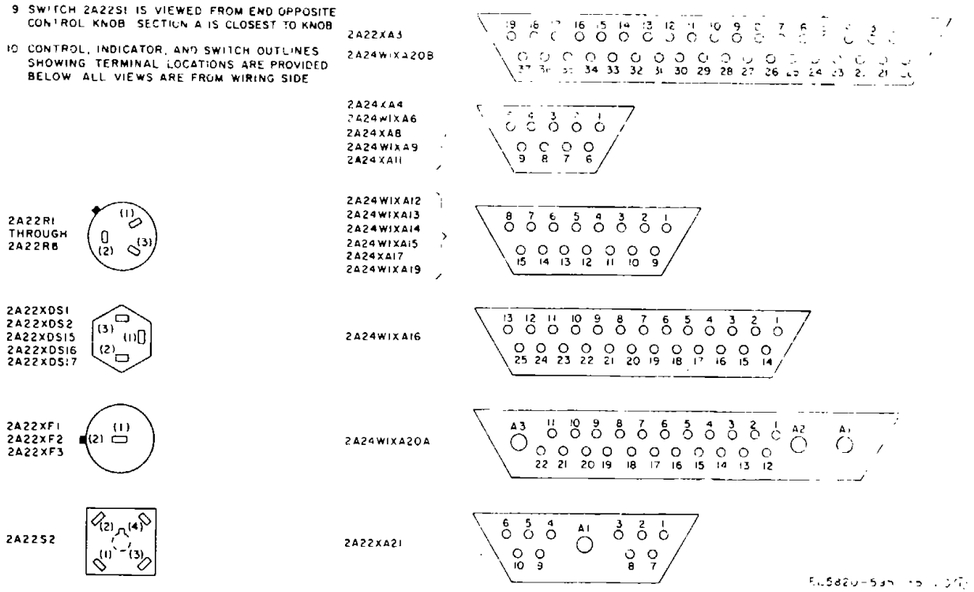


Figure 8-59 (1). Receiver (unit 2), interconnecting diagram (part 1 of 3).

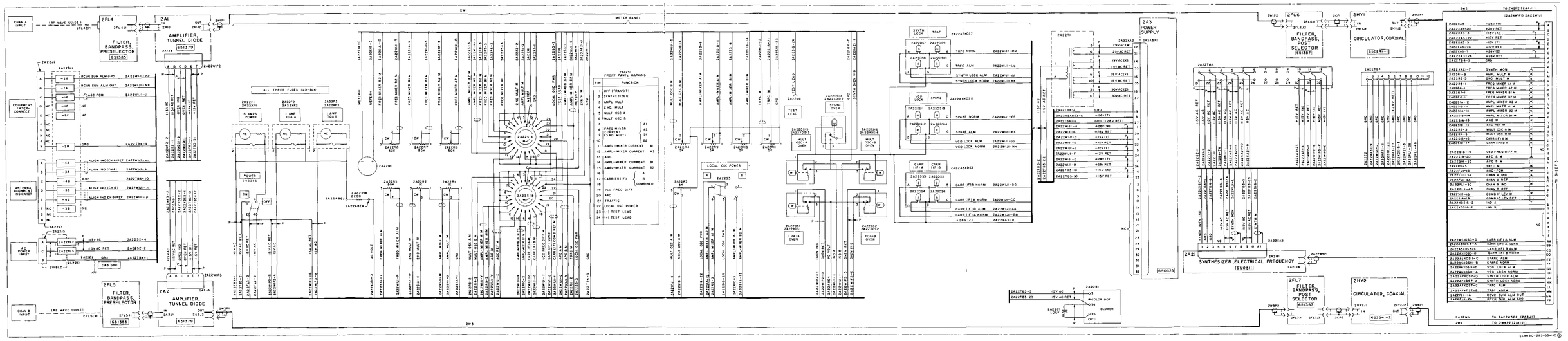


Figure 8-59 (2). Receiver (unit 2), interconnecting diagram (part 2 of 3)

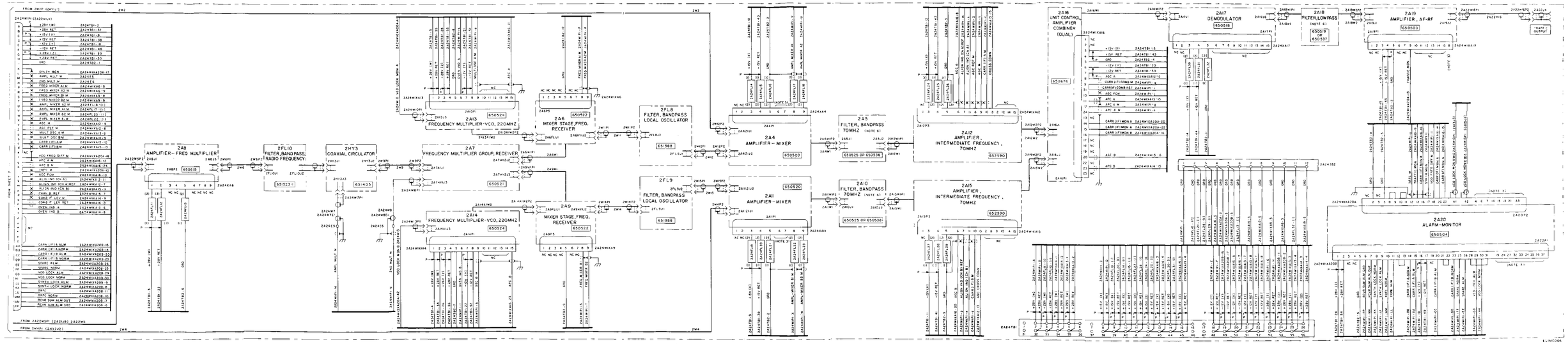


Figure 8-59 (3). Receiver (unit 2), interconnecting diagram (part 3 of 3)

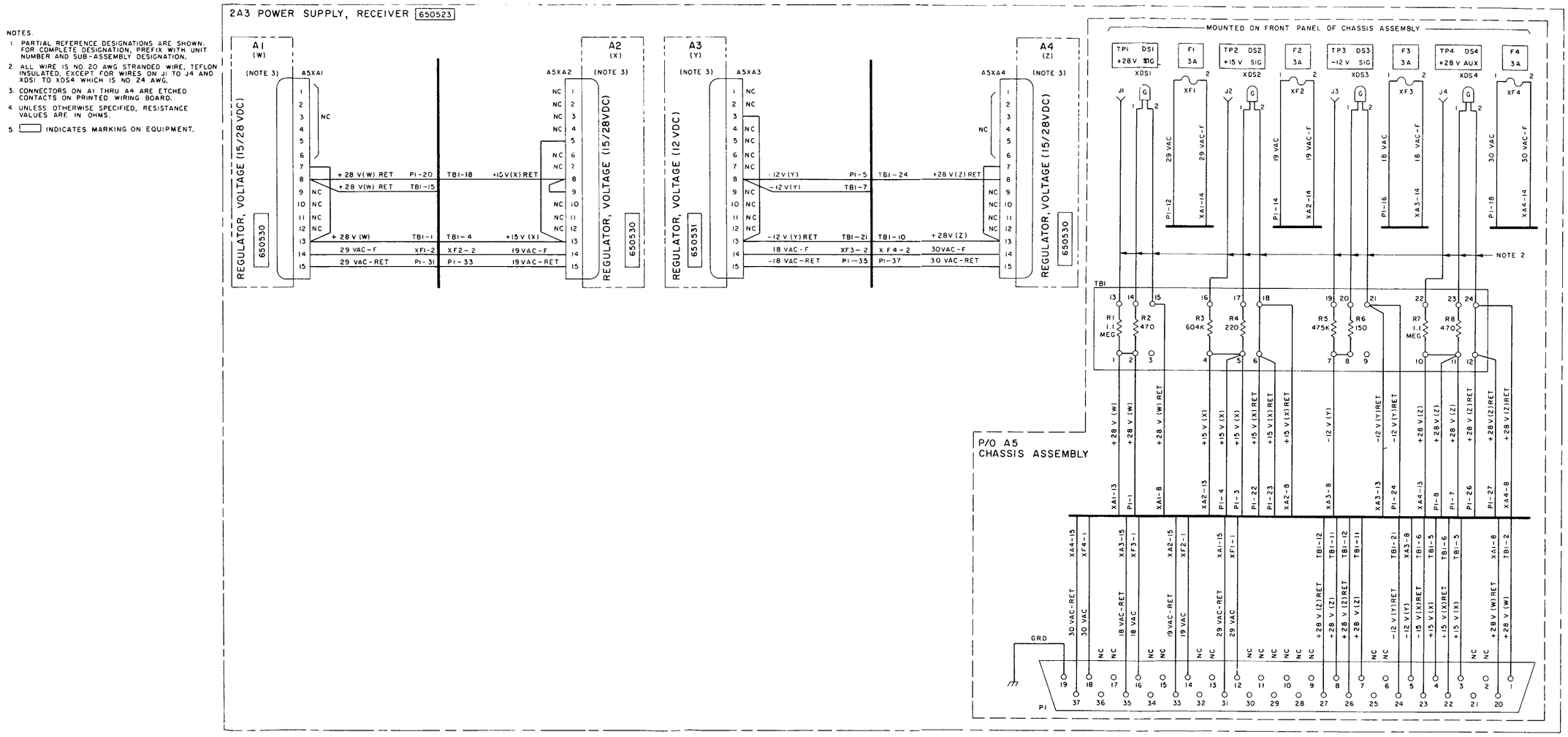


Figure 8-60. Power supply 2A3, interconnecting diagram.

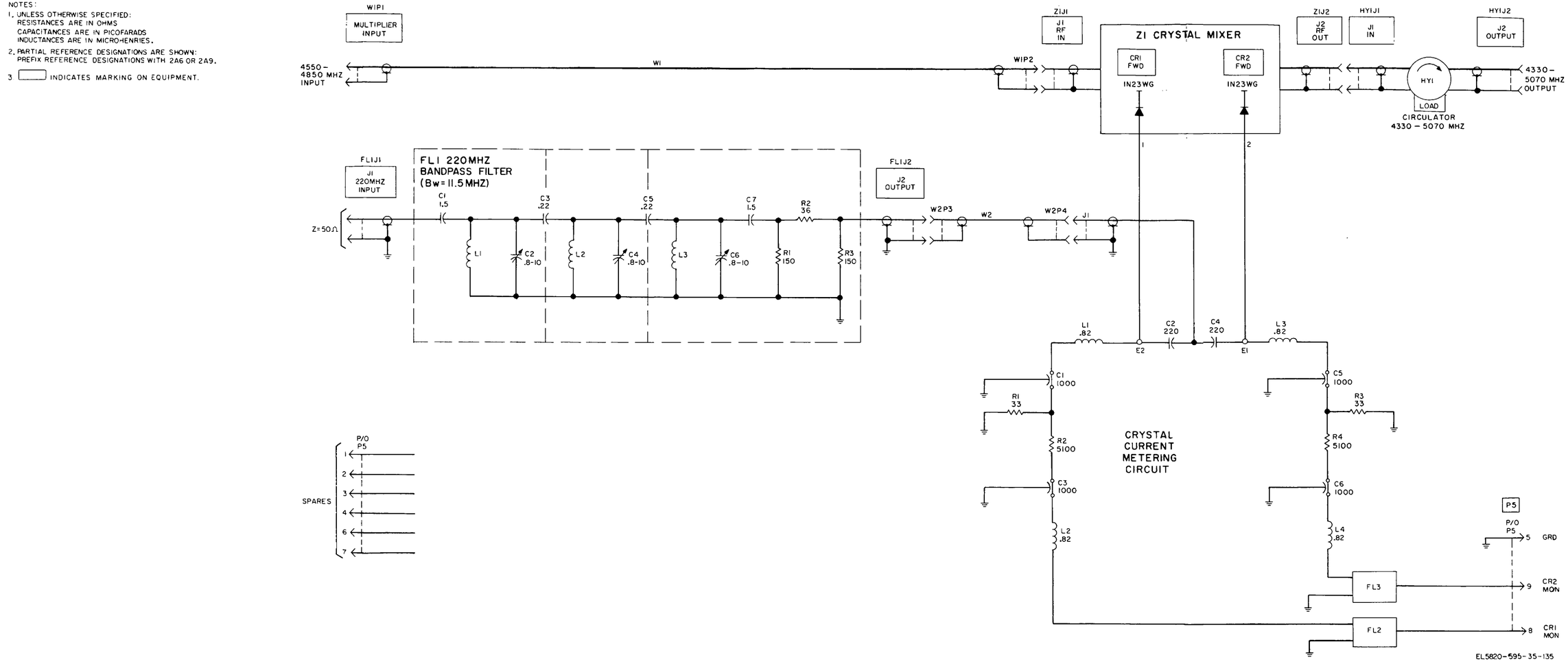
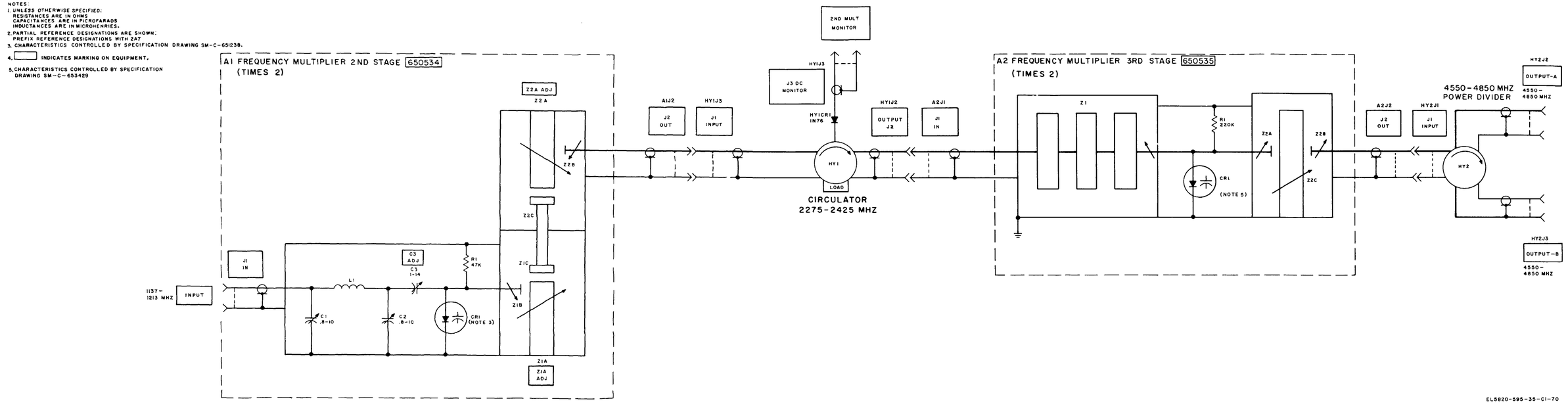
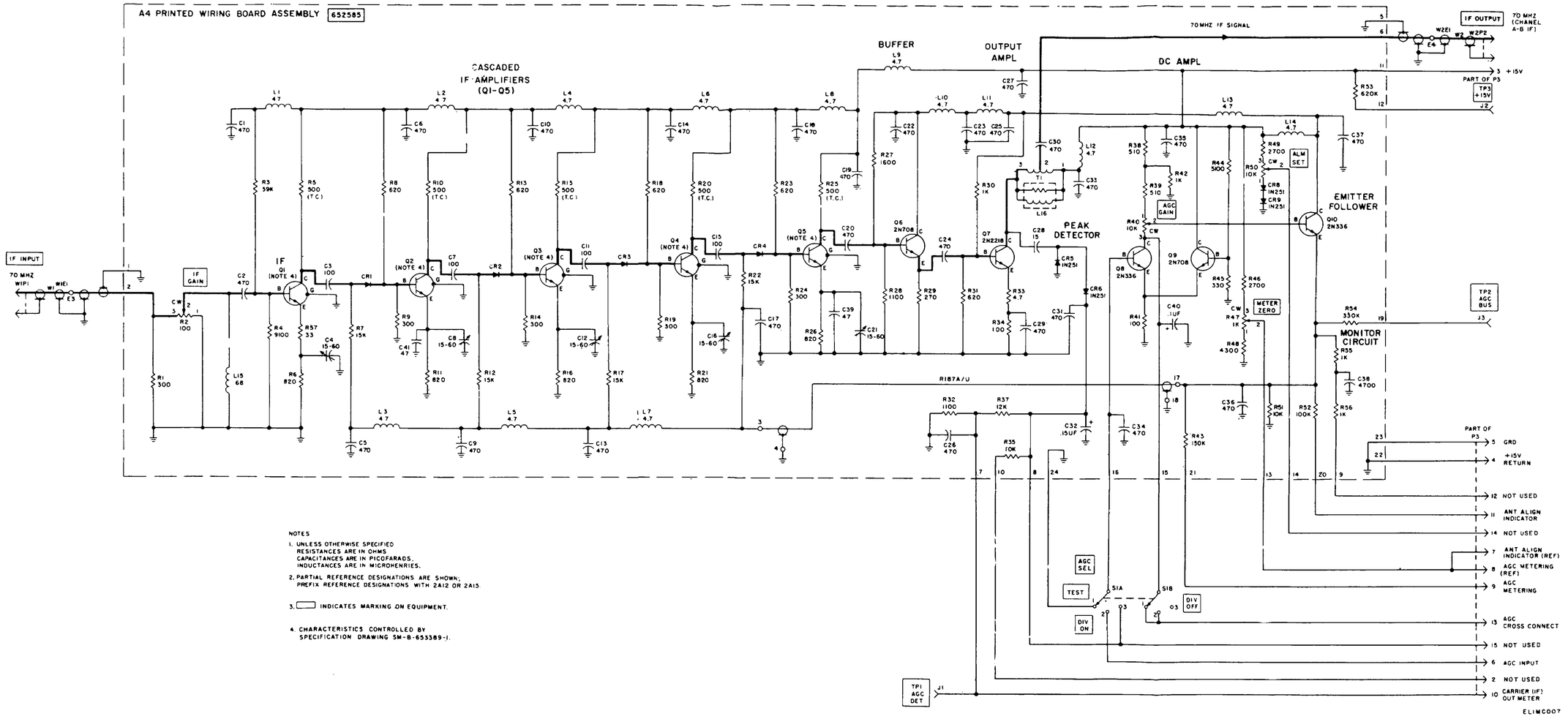


Figure 8-61. Frequency mixer 2A6/2A9, schematic diagram.



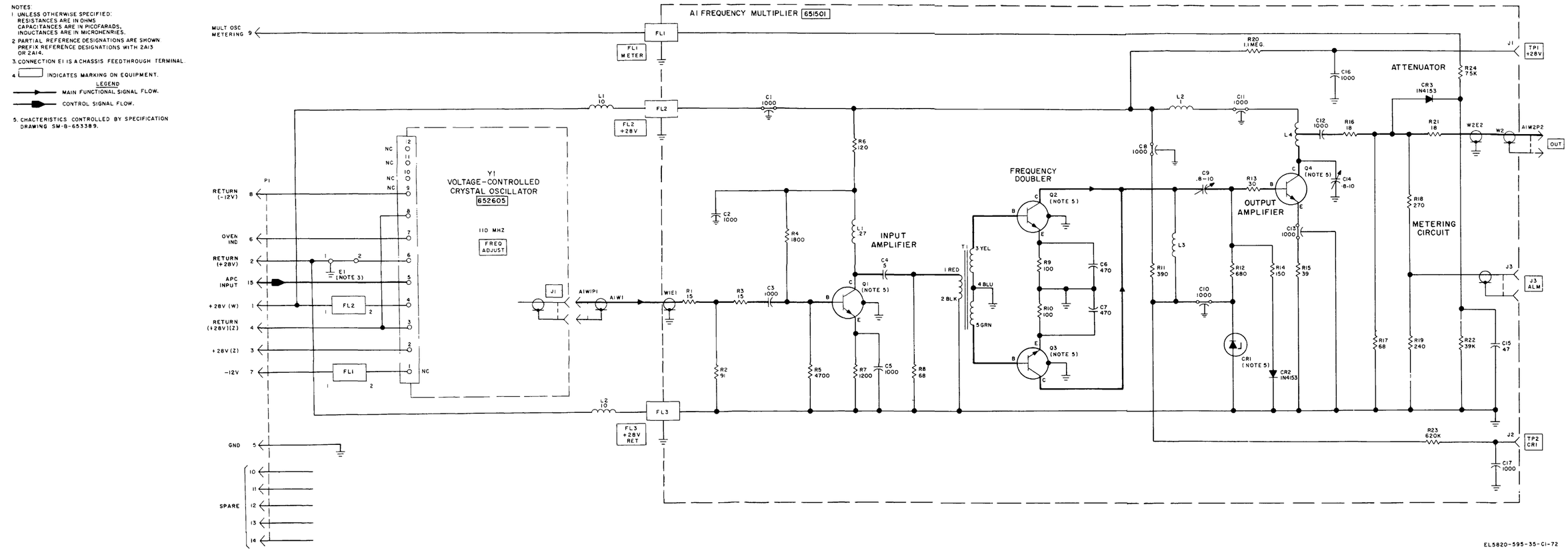
Change 1 **Figure 8-62. Frequency multiplier group 2A7, schematic diagram.**



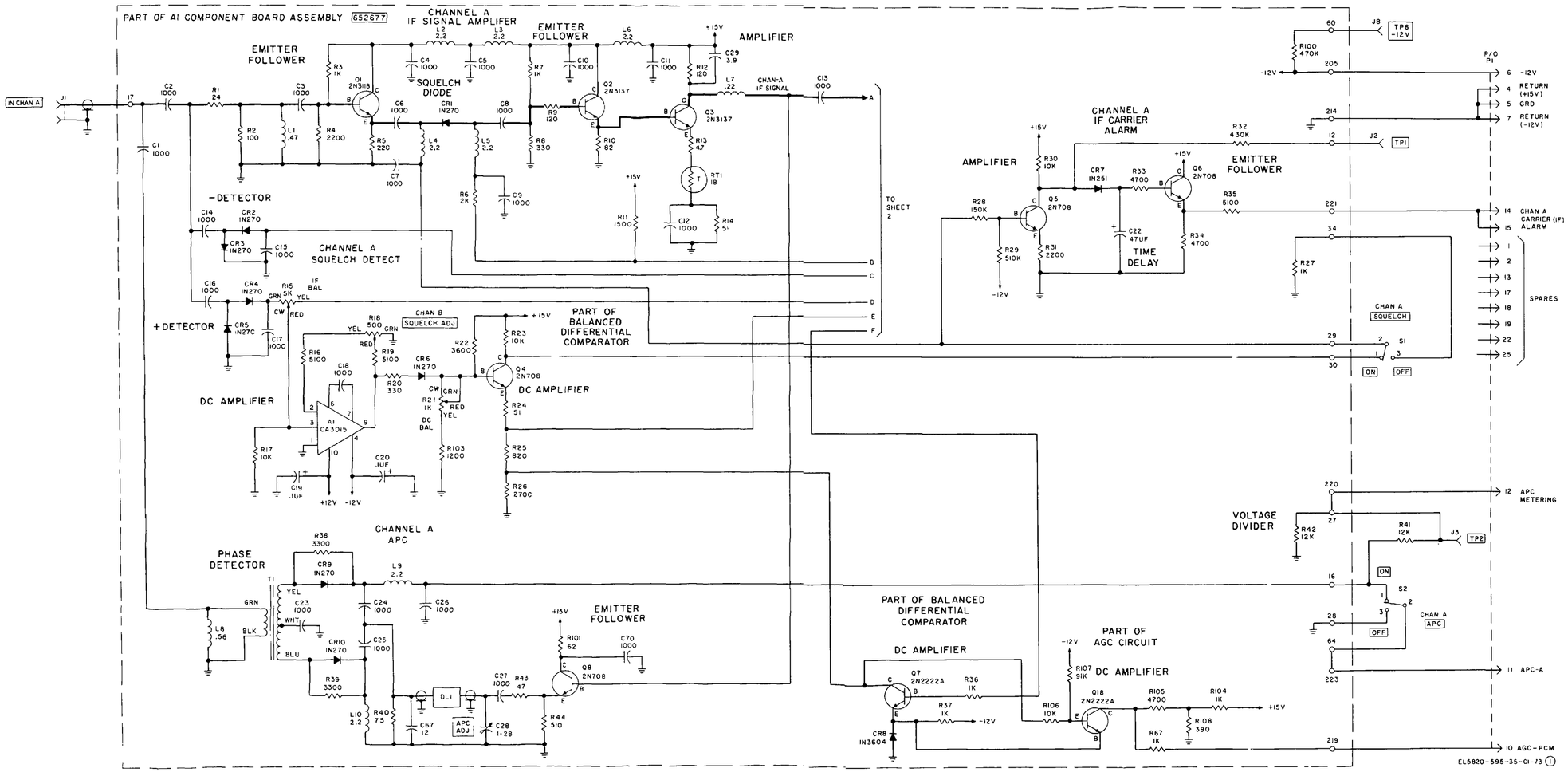
NOTES

1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN PICOFARADS. INDUCTANCES ARE IN MICROHENRIES.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; PREFIX REFERENCE DESIGNATIONS WITH 2A12 OR 2A15
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-653389-1.

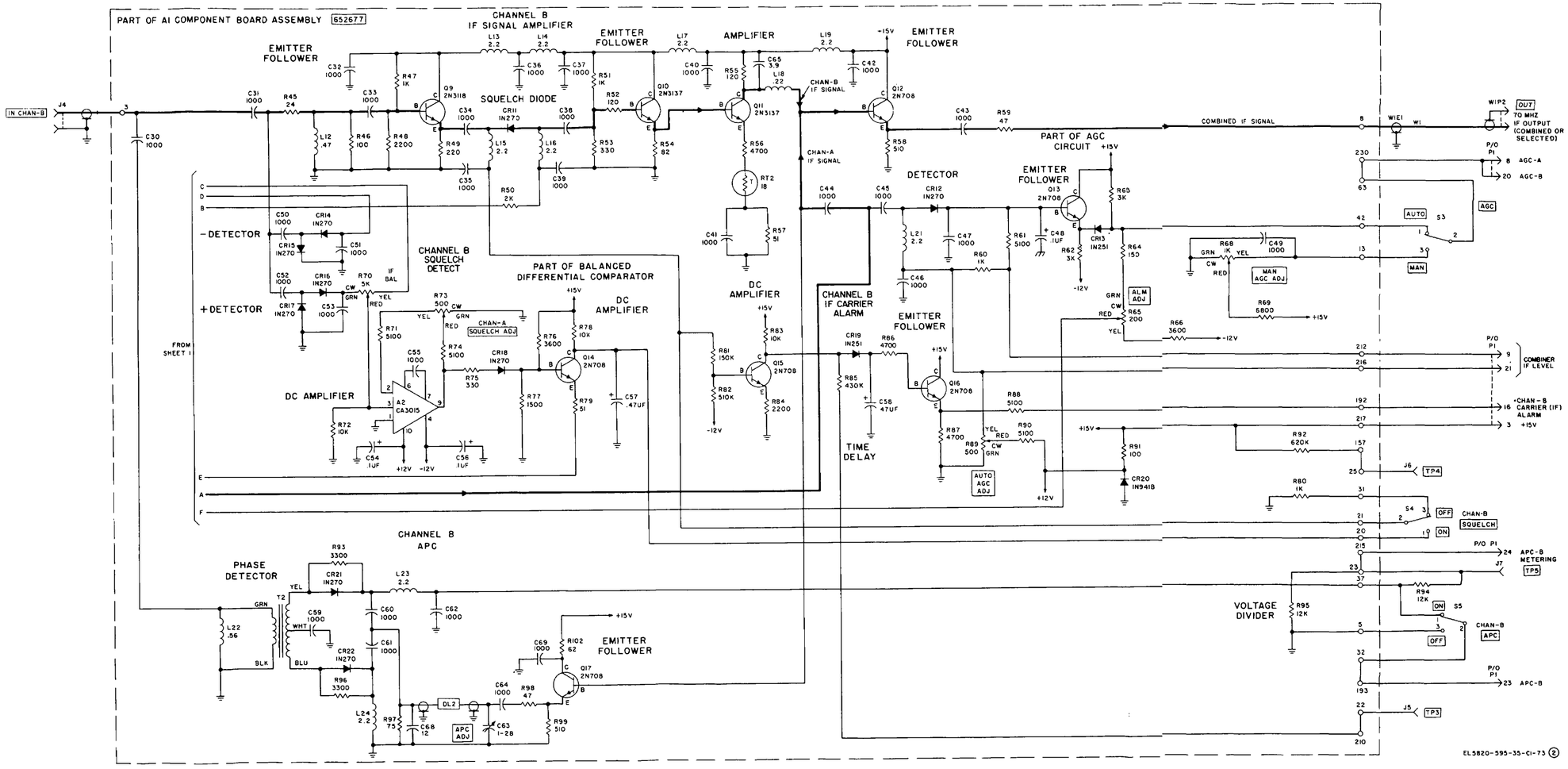
Change 2 **Figure 8-63. If amplifier 2A12/2A15, schematic diagram.**



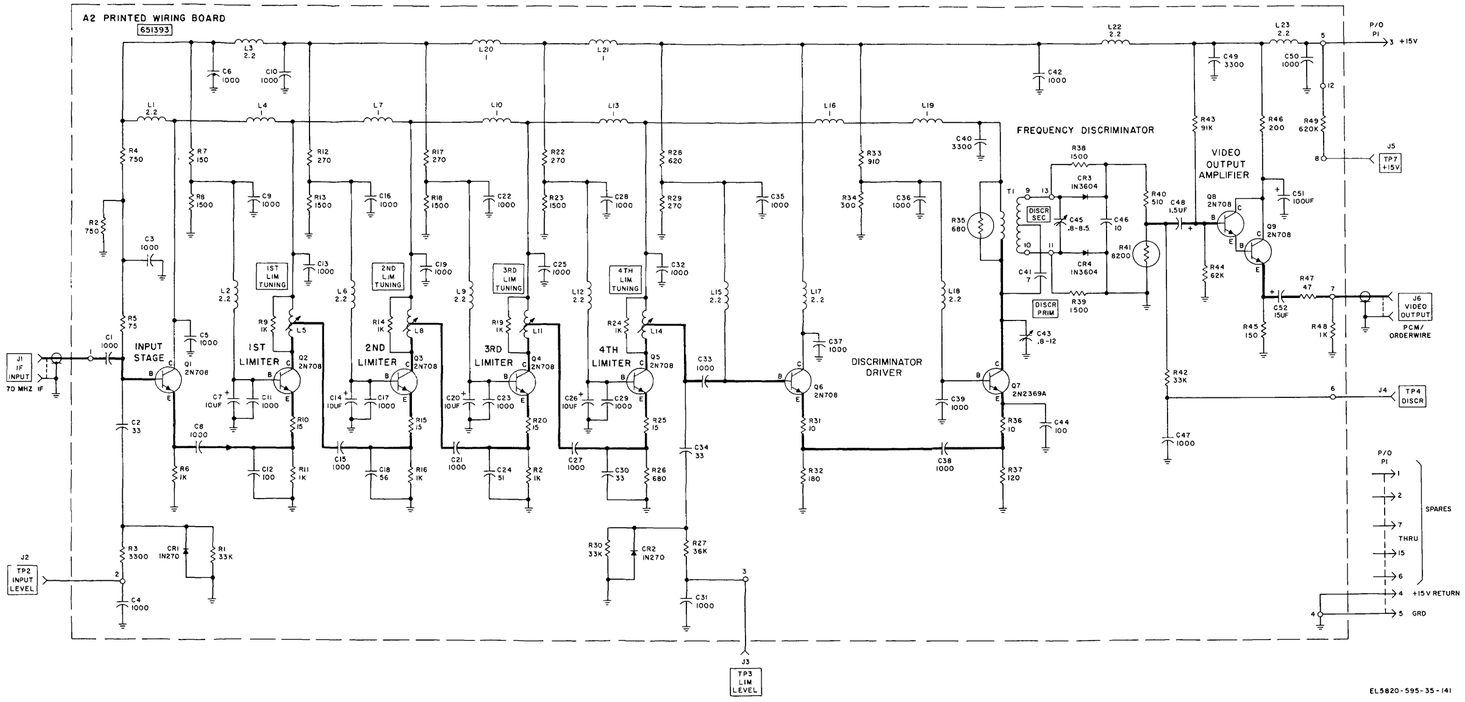
Change 1 Figure 8-64. 220 MHz vco 2A13/2A14, schematic diagram.



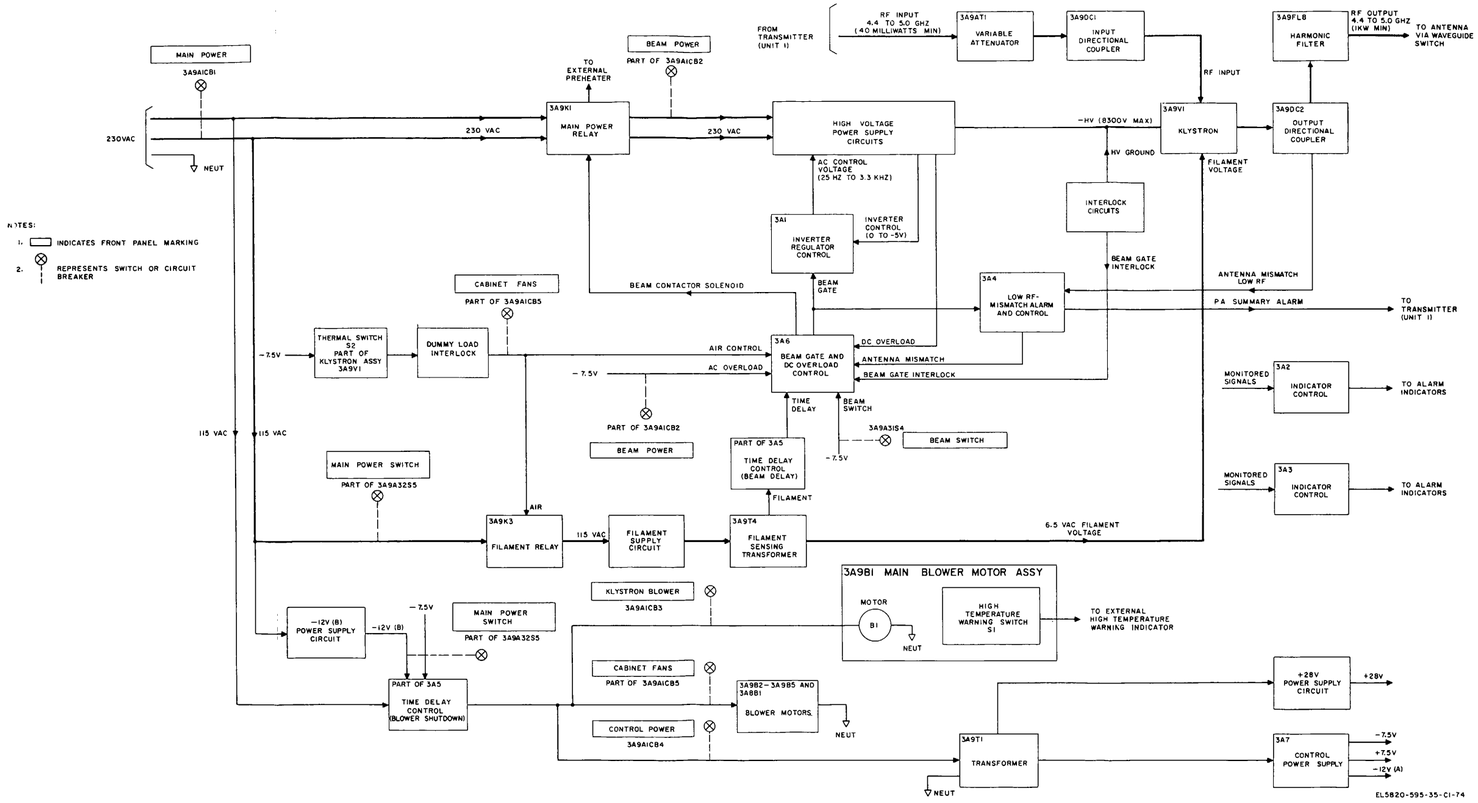
Change 1 **Figure 8-65 (1). Combiner 2A16, schematic diagram (part 1 of 2).**



Change 1 Figure 8-65 (2). Combiner 2A16, schematic diagram (part 2 of 2).

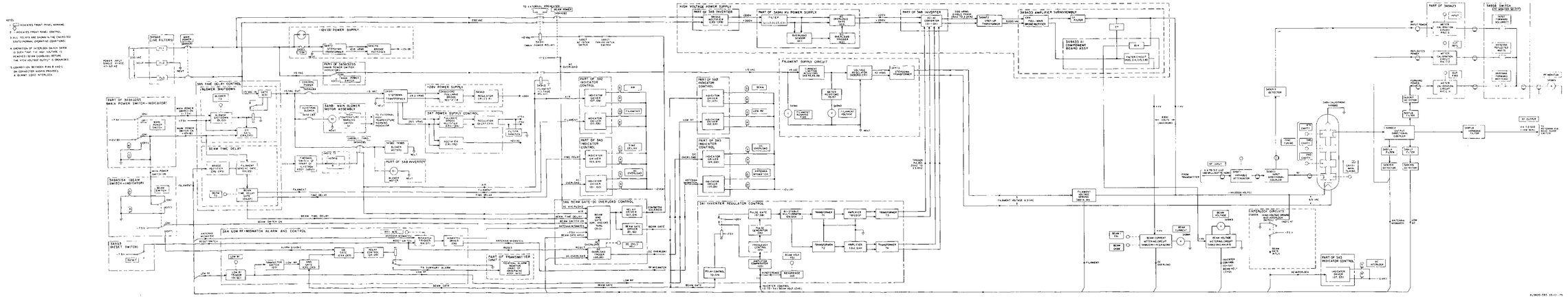


Change 1
Figure 8-66. Demodclator 2A17, schematic diagram



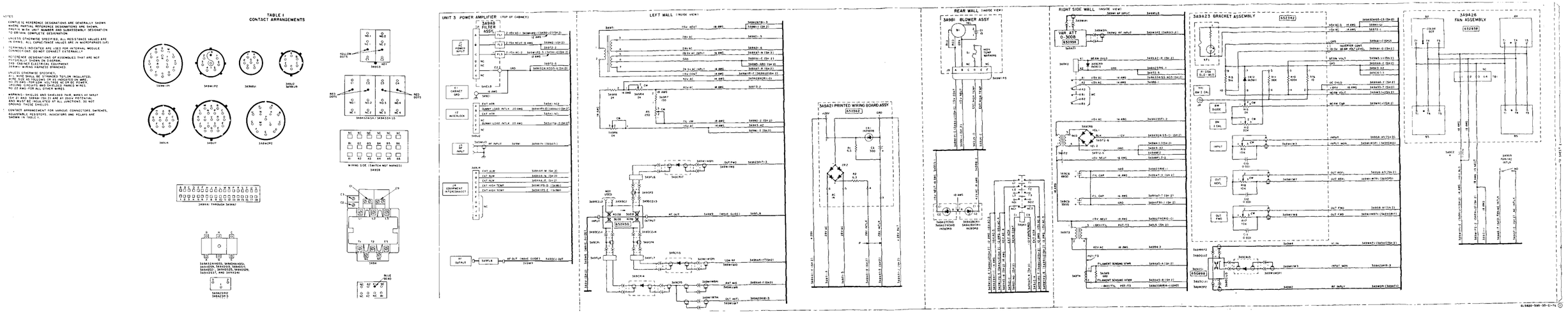
Change 1

Figure 8-67. Power amplifier block diagram



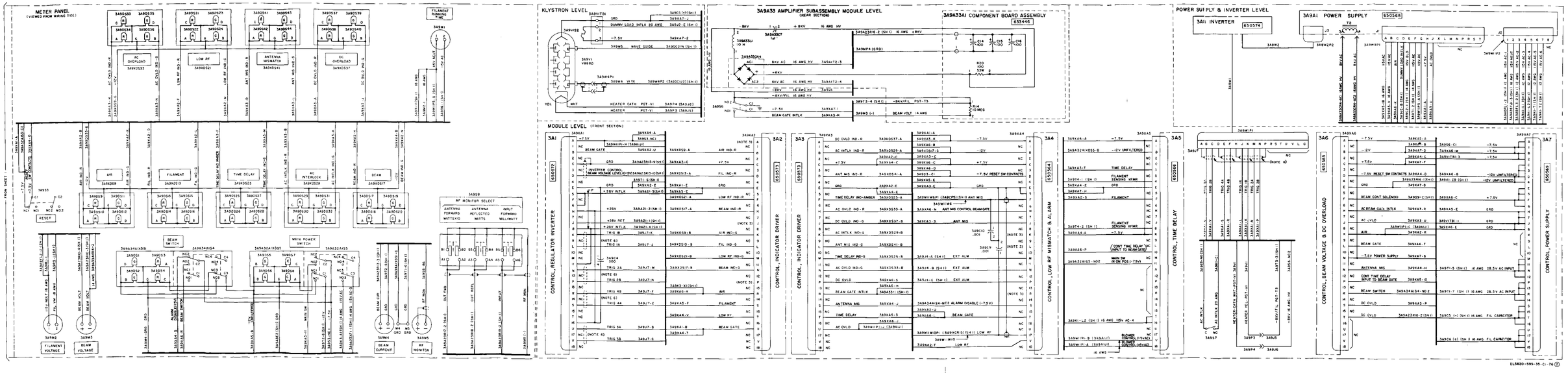
Change 1

Figure 8-68. Power amplifier module block diagram



Change 1

Figure 8-69 (1). Power amplifier (unit 3), interconnecting diagram (part 1 of 2).

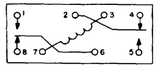


Change 1

Figure 8-69(2). Power amplifier (unit 3). Interconnecting diagram (part 2 of 2)

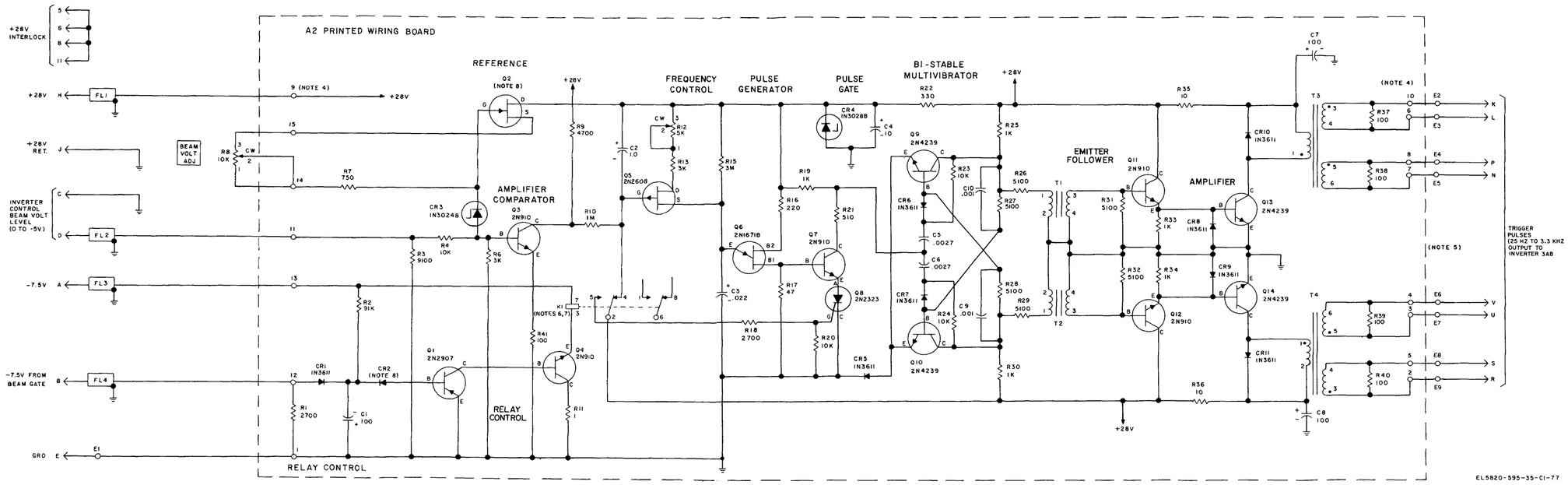
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS,
   CAPACITANCES ARE IN MICROFARDS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN;
   PREFIX REFERENCE DESIGNATIONS WITH 3A1.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. TERMINALS 1 TO 15 ARE ACTUALLY PADS ON PRINTED WIRING BOARD A2.
5. SPARE EXTERNAL CONTACTS (NOT SHOWN): 1, 2, 3, 4, 7, 9, 10, 12 TO 18, F, M, T.
6. PIN LOCATION DIAGRAM FOR K1, BLUE BEAD ON PIN 7.



7. RELAY K1 SHOWN DE-ENERGIZED.
8. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING.

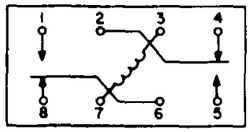
REFERENCE DESIGNATION	SPECIFICATION DRAWING
CR2	SM-C-651872
Q2	SM-B-653264



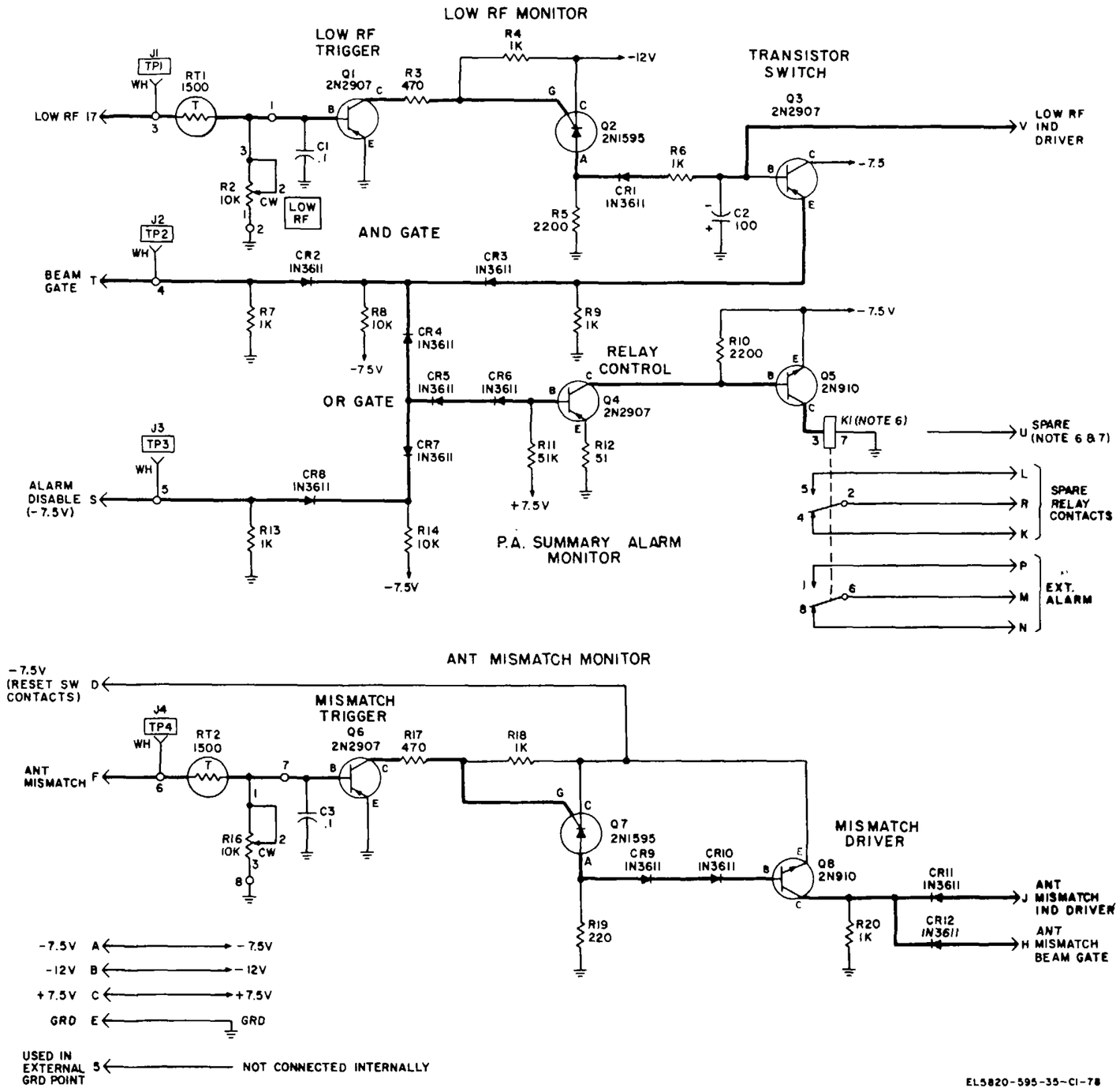
Change 1

Figure 8-70. Inverter regulator control 3A1, schematic diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS.
   CAPACITANCES ARE IN MICROFARADS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 3A4.
3. ▭ INDICATES MARKING ON EQUIPMENT.
4. TERMINALS 1 THRU 8 ARE TERMINAL PADS ON PRINTED WIRING BOARD A1.
5. SPARE CONTACTS: 1 THRU 4, 6 THRU 16, 18 & U.
6. PIN LOCATION DIAGRAM FOR K1
   BLUE BEAD ON PIN 7.



7. RELAY K1 SHOWN DE-ENERGIZED.

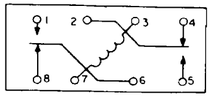


Change 1

Figure 8-71. Low RF-mismatch, alarm and control 3A4, schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCES ARE IN OHMS
   CAPACITANCES ARE IN MICROFARADS
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   PREFIX REFERENCE DESIGNATIONS WITH 3A5
3. ▭ INDICATES MARKING ON EQUIPMENT
4. PIN LOCATION DIAGRAM FOR K1:
   BLUE BEAD ON PIN 7



5. RELAY K1 SHOWN DE-ENERGIZED.
6. TERMINALS 1 THRU 9, A1, A2, G ARE TERMINAL PADS ON PRINTED WIRING BOARD A1.
7. PINS A AND K ARE EXTERNALLY JUMPERED.
8. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-653271.
9. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-650889.

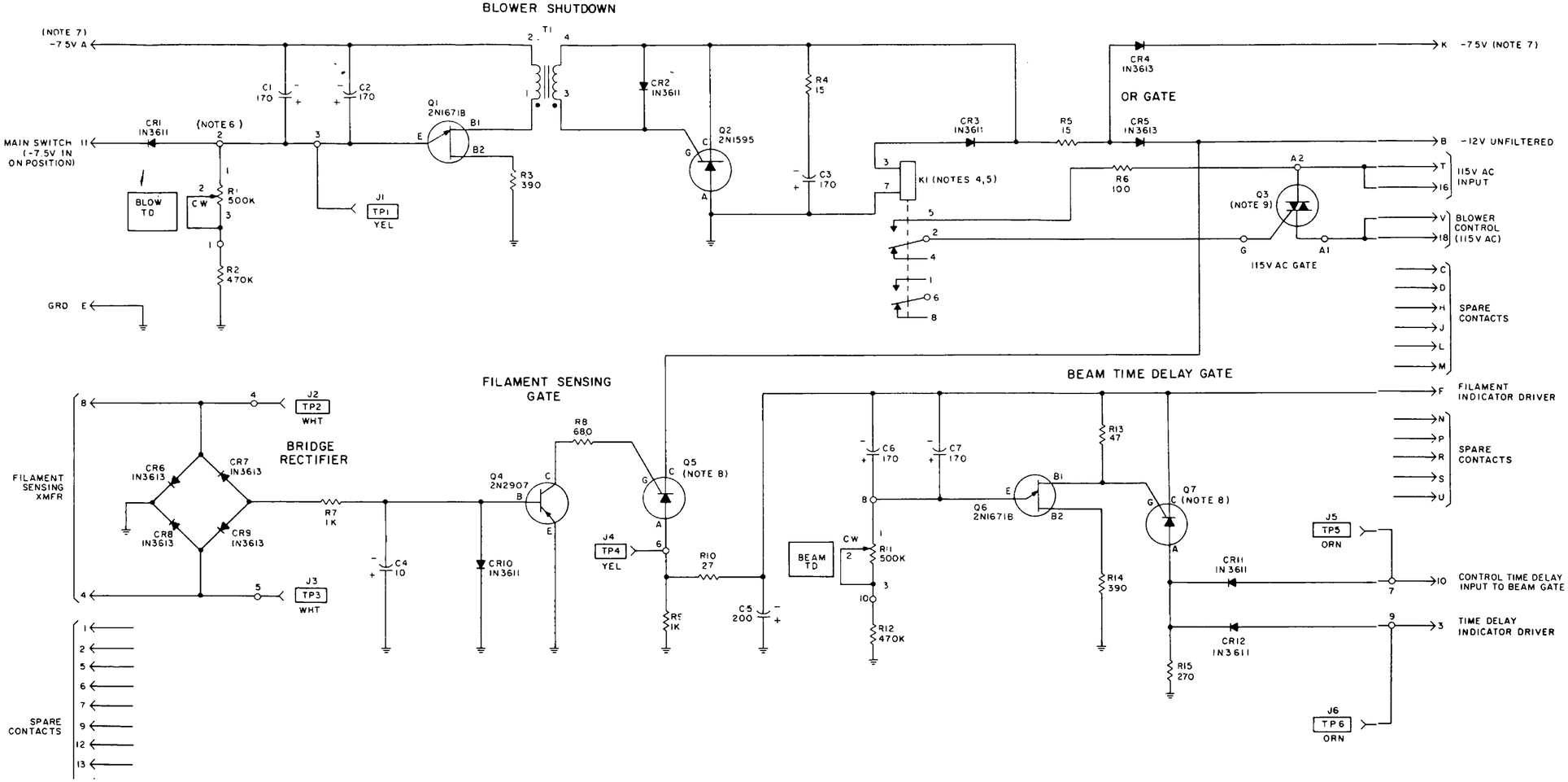
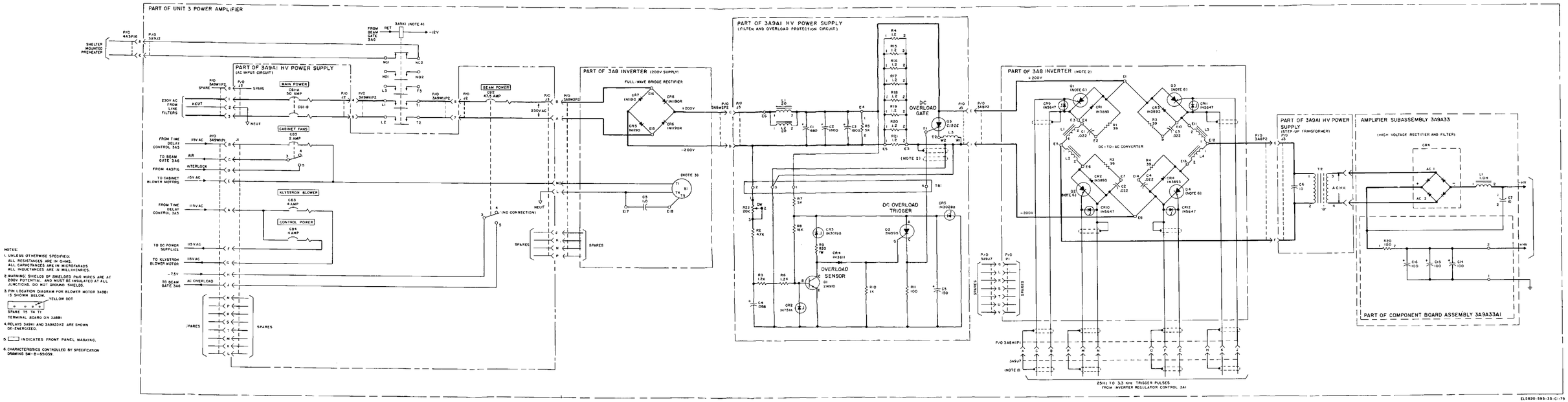


Figure 8-72. Time delay control 3A5, schematic diagram.



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN MICROFARADS
   ALL INDUCTANCES ARE IN MILLIHENRIES.
2. WARNING: SHIELDS OF SHIELDED PAIR WIRES ARE AT 200V POTENTIAL AND MUST BE INSULATED AT ALL JUNCTIONS. DO NOT GROUND SHIELDS.
3. PIN LOCATION DIAGRAM FOR BLOWER MOTOR 3A5B1 IS SHOWN BELOW.
   SPARE T5 to T1
   TERMINAL BOARD ON 3A5B1
4. RELAYS 3A9K1 AND 3A9A33K2 ARE SHOWN DE-ENERGIZED.
5. [ ] INDICATES FRONT PANEL MARKING.
6. CHARACTERISTICS CONTROLLED BY SPECIFICATION DRAWING SM-B-651059.

Change 1

Figure 8-73. High voltage power supply 3A9A1, schematic diagram.

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.

2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

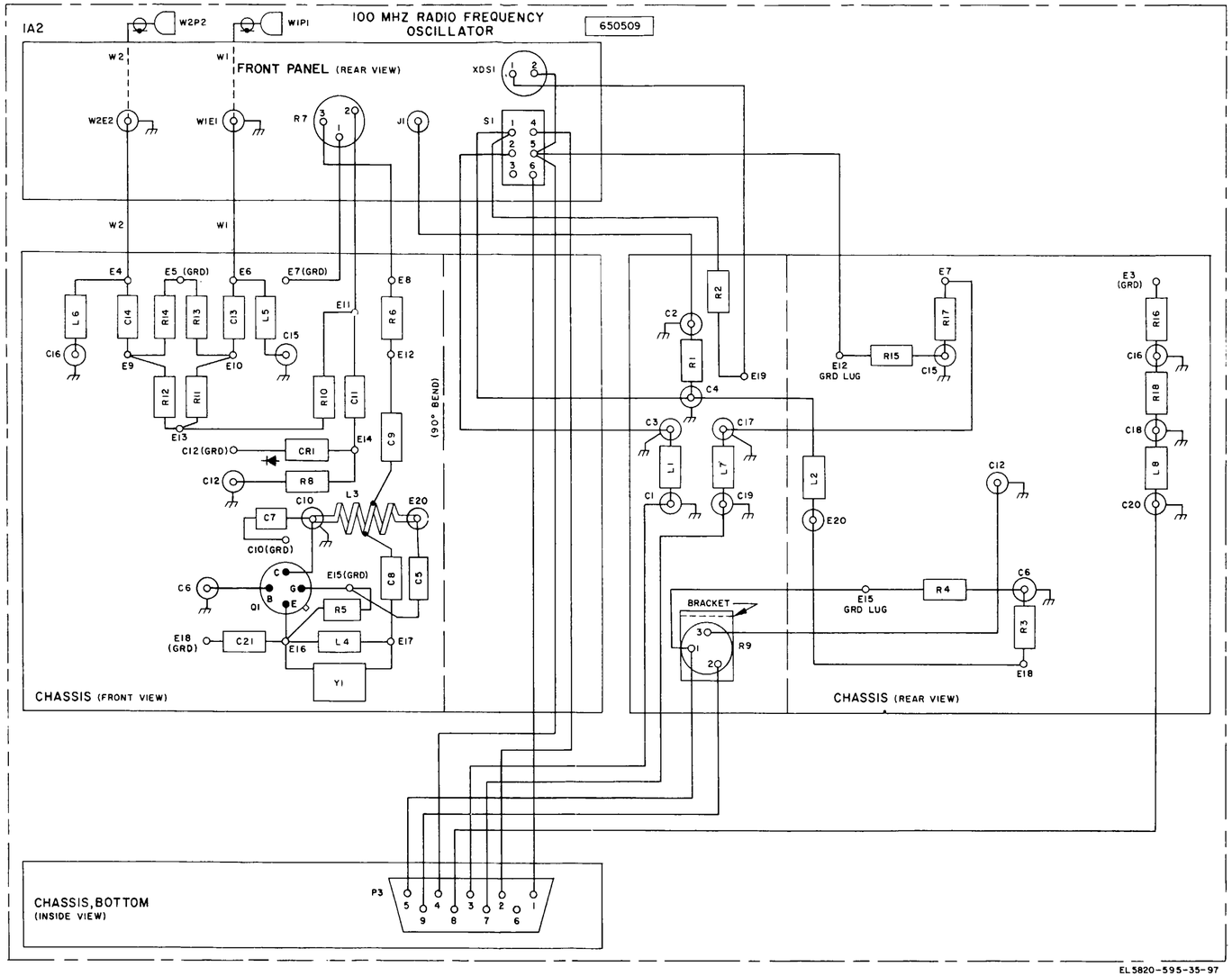
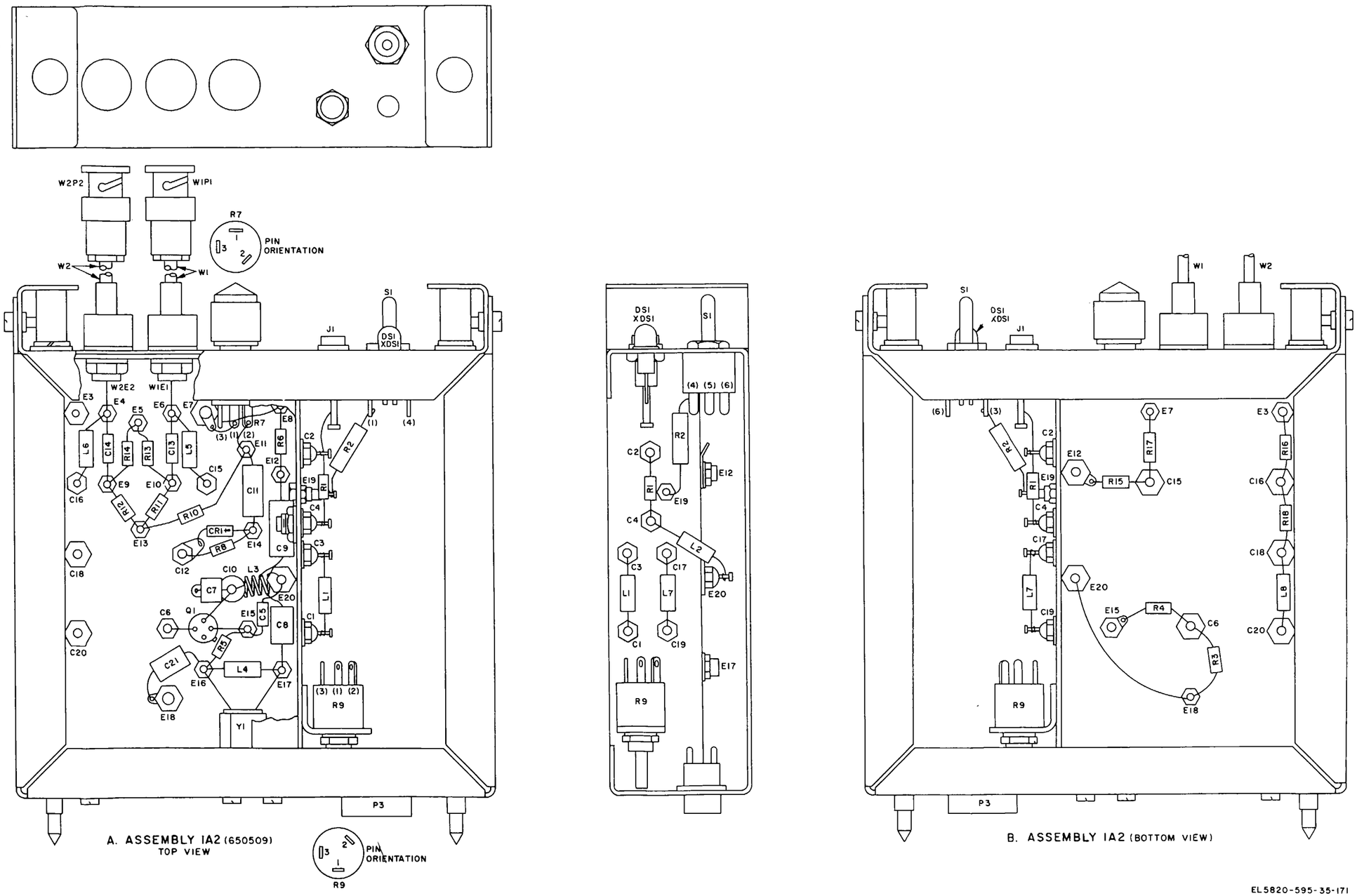


Figure 8-74. 100 MHz rf oscillator 1A2, wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A2.



EL5820-595-35-171

Figure 8-75. 100 MHz RF oscillator 1A2, parts location diagram.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB — ASSEMBLY DESIGNATION.

2. ALL WIRE IS NO. 26 AWG STRANDED TEFLON INSULATED, UNLESS SPECIFIED AS NO. 22 AWG.

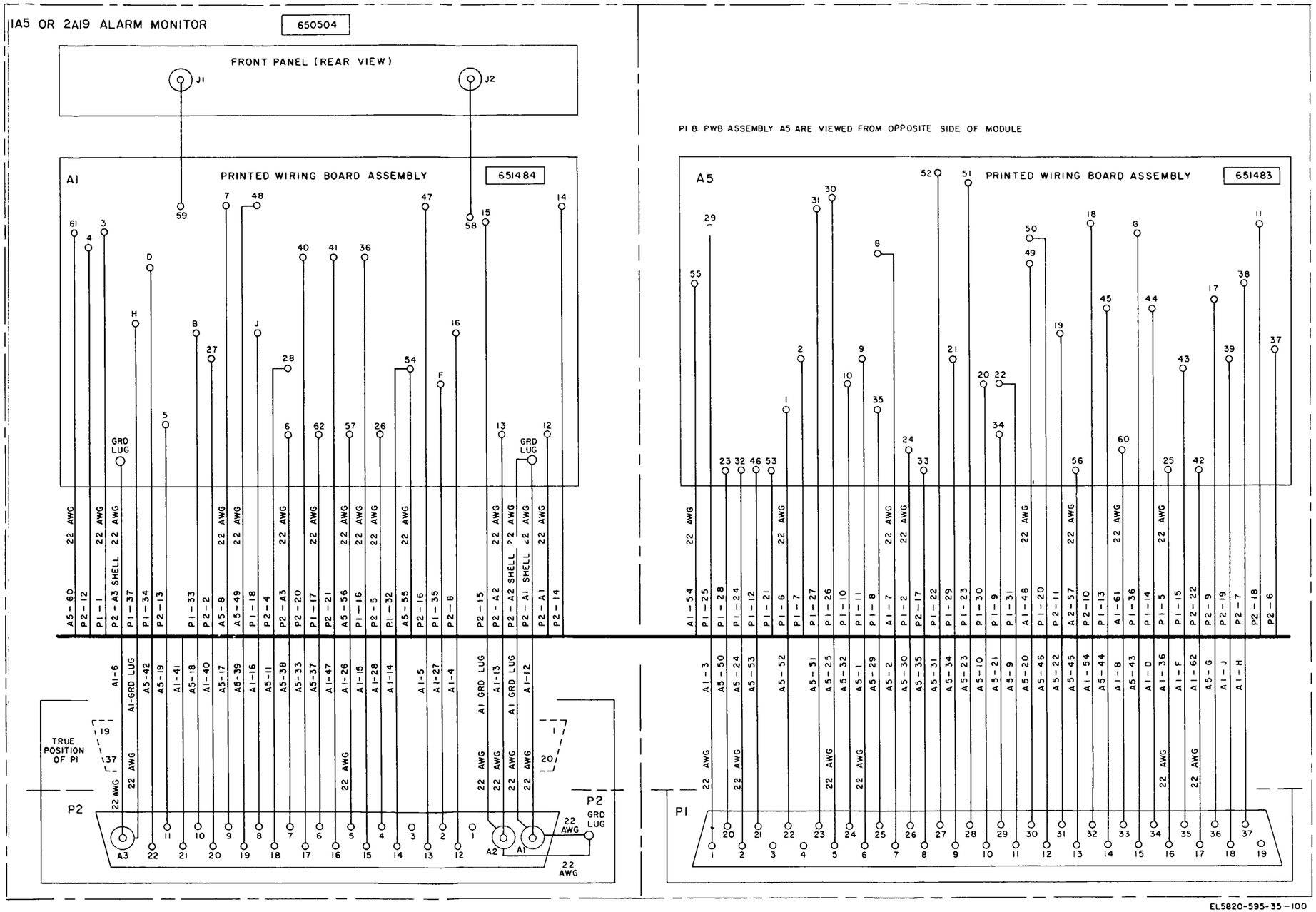


Figure 8-76. Alarm monitor 1A5/2A20, assembly wiring diagram.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A5 (TRANSMITTER) OR 2A20 (RECIVER).
2. COMPONENT SIDES OF BOARDS FACE OUTWARD.

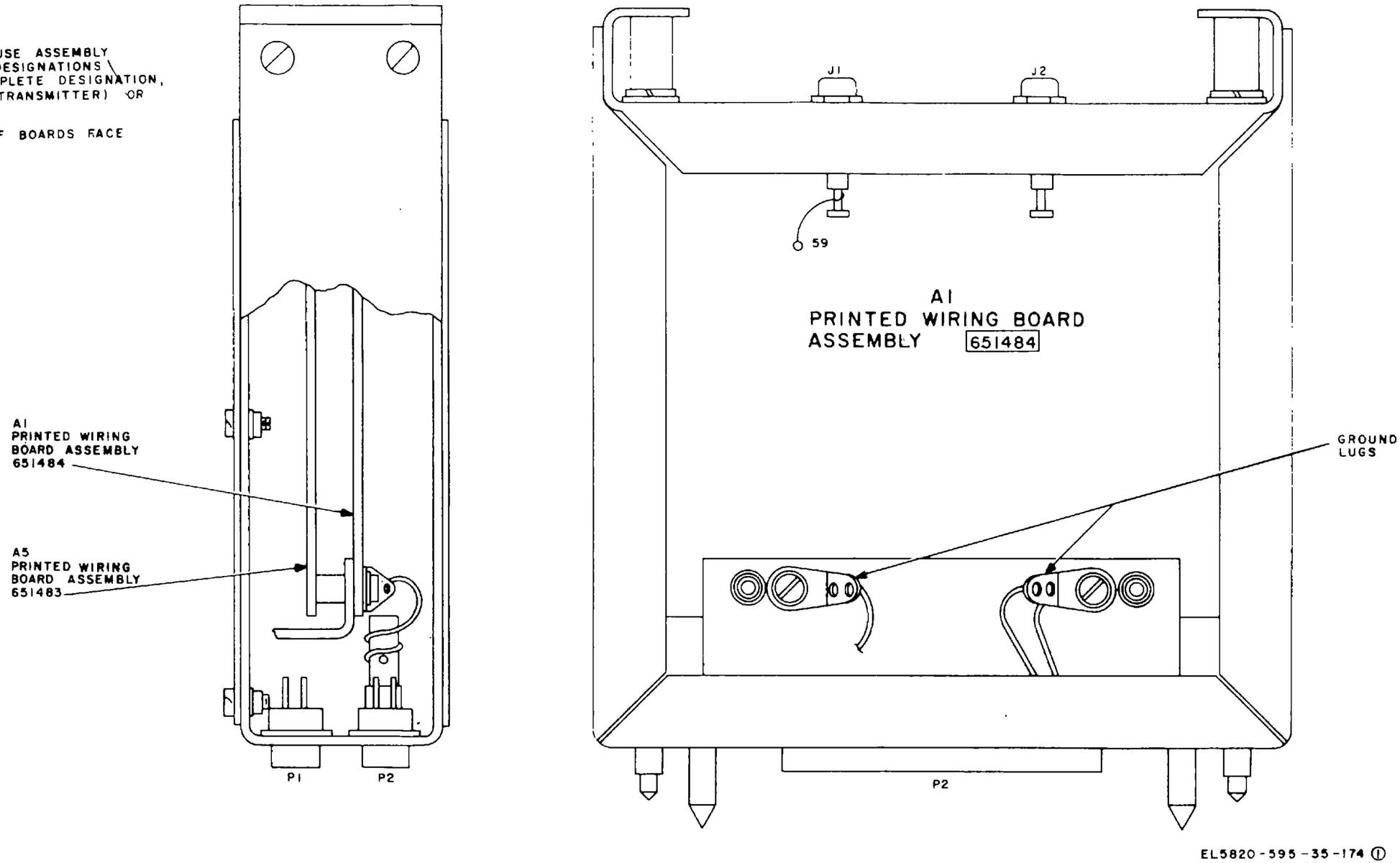
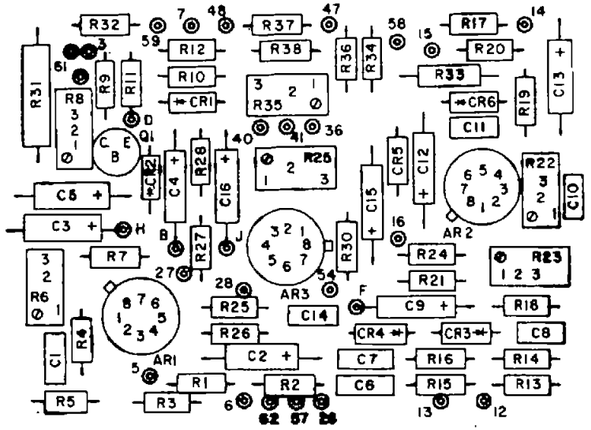
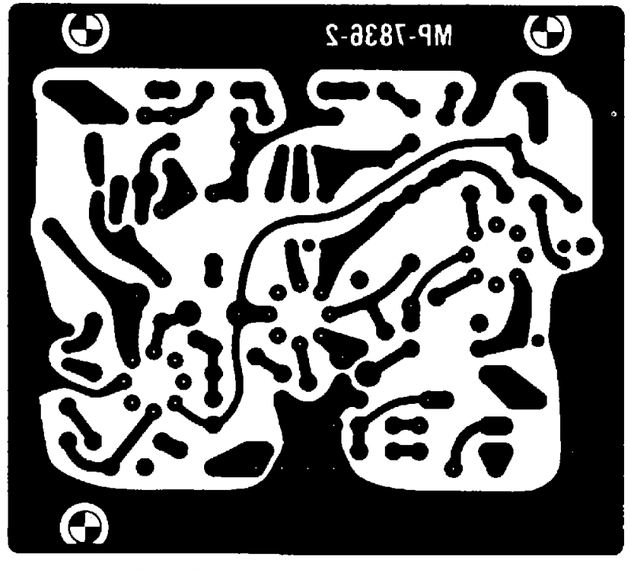


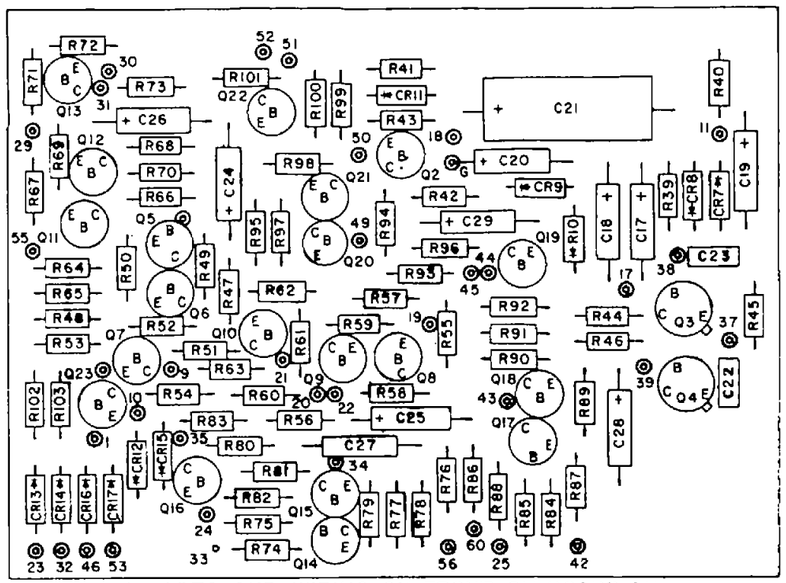
Figure 8-77(1). Alarm monitor 1A5/2A20, parts location and Printed wiring diagram (part 1 of 2)



A. PARTS AND WIRING ON FRONT OF BOARD A1.



B. WIRING ON BACK OF BOARD A1
(VIEWED THROUGH FRONT)



C. PARTS AND WIRING ON FRONT OF BOARD A5.

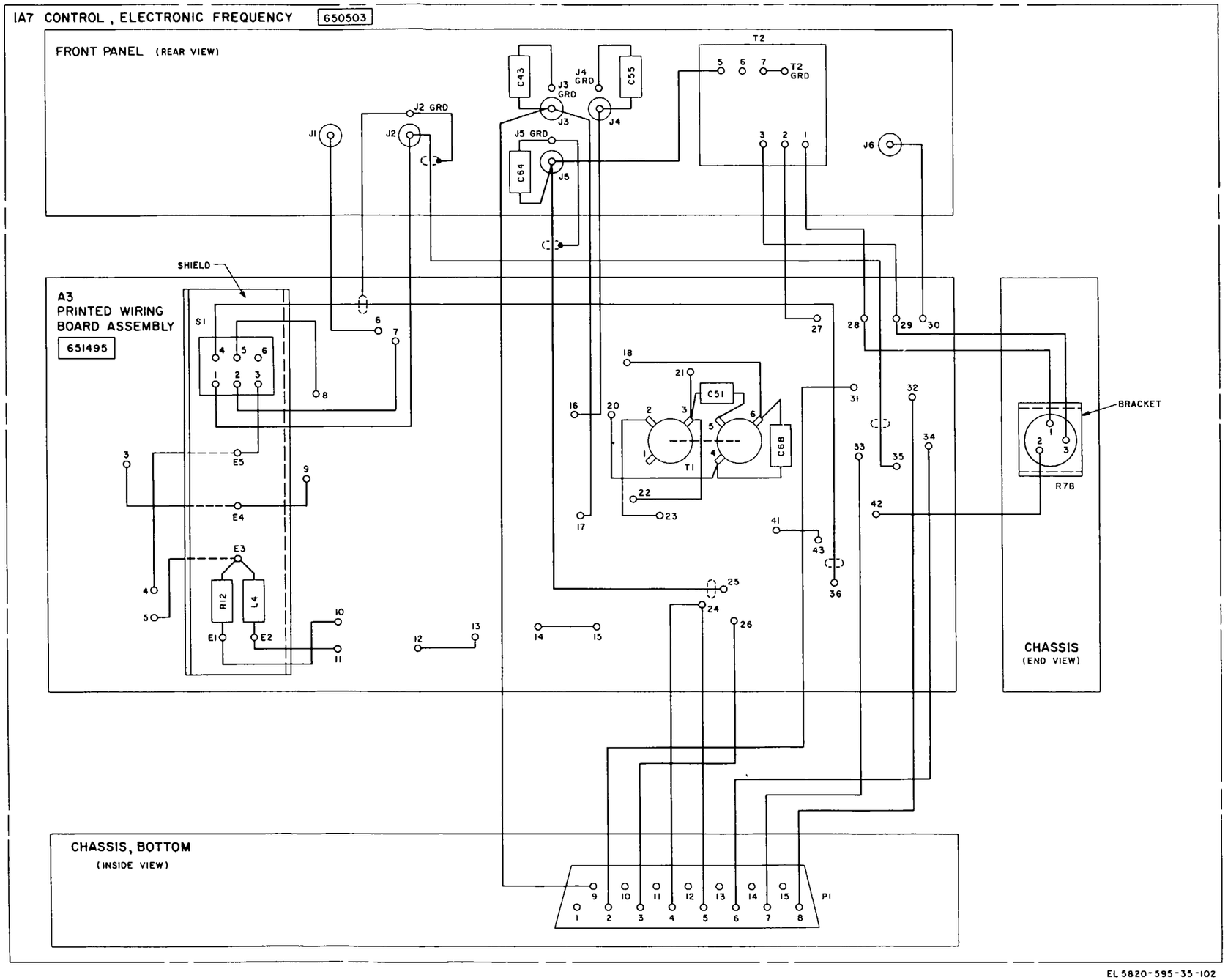
D. WIRING ON BACK OF BOARD A5
(VIEWED THROUGH FRONT).

EL5820-595-35-174 (2)

Figure 8-77(2). Alarm monitor 1A5/2A20, parts location and Printed wiring diagram (part 2 of 2)

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.



EL 5820-595-35-102

Figure 8-78. Electronic frequency control 1A7, assembly wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A7.

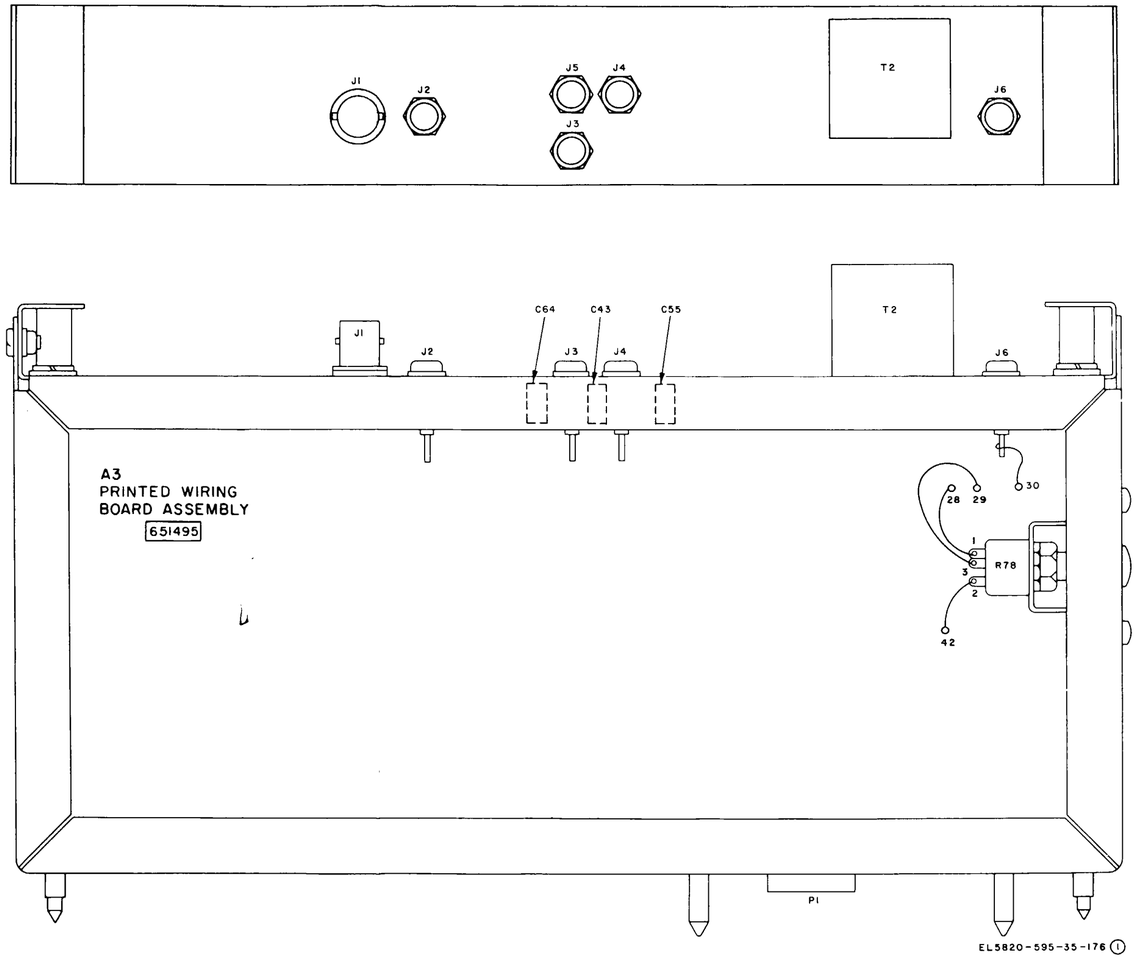


Figure 8-79 (1). Electronic frequency control 1A7, parts location and printed wiring diagram (part 1 of 2).

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A7.

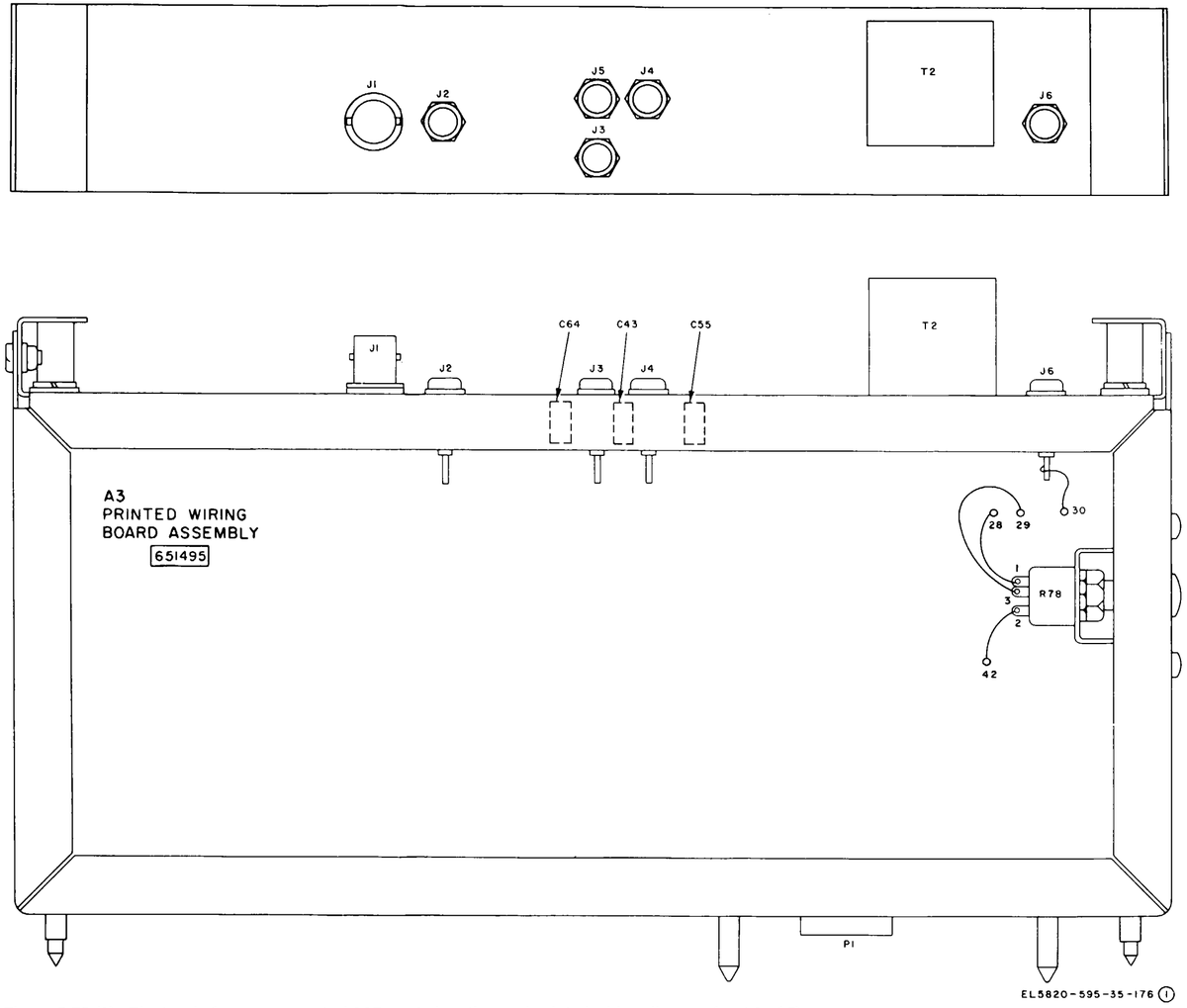


Figure 8-79 (1). Electronic frequency control 1A7, parts location and printed wiring diagram (part 1 of 2).

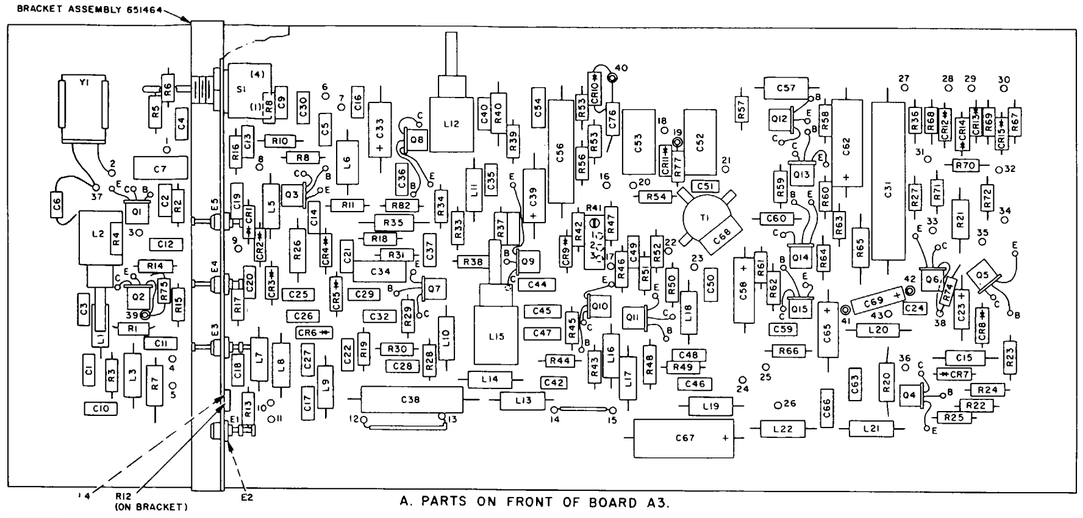


Figure 8-79 (2). Electronic frequency control 1A7, parts location and printed wiring diagram (part 2 of 2).

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO.22 AWG STRANDED, TEFLON INSULATED.
3. WIRING TIEPOINT TERMINAL NUMBERS (WT——) ARE ASSIGNED FOR IDENTIFICATION PURPOSES ONLY, THEY ARE NOT MARKED ON EQUIPMENT.
4. IN SOME COMPONENTS, RESISTOR R78 IS ADDED AND SWITCH S1 IS SPOT. IN THESE CASES RESISTOR R21 IS LOCATED ON THE ASSEMBLY BOTTOM.

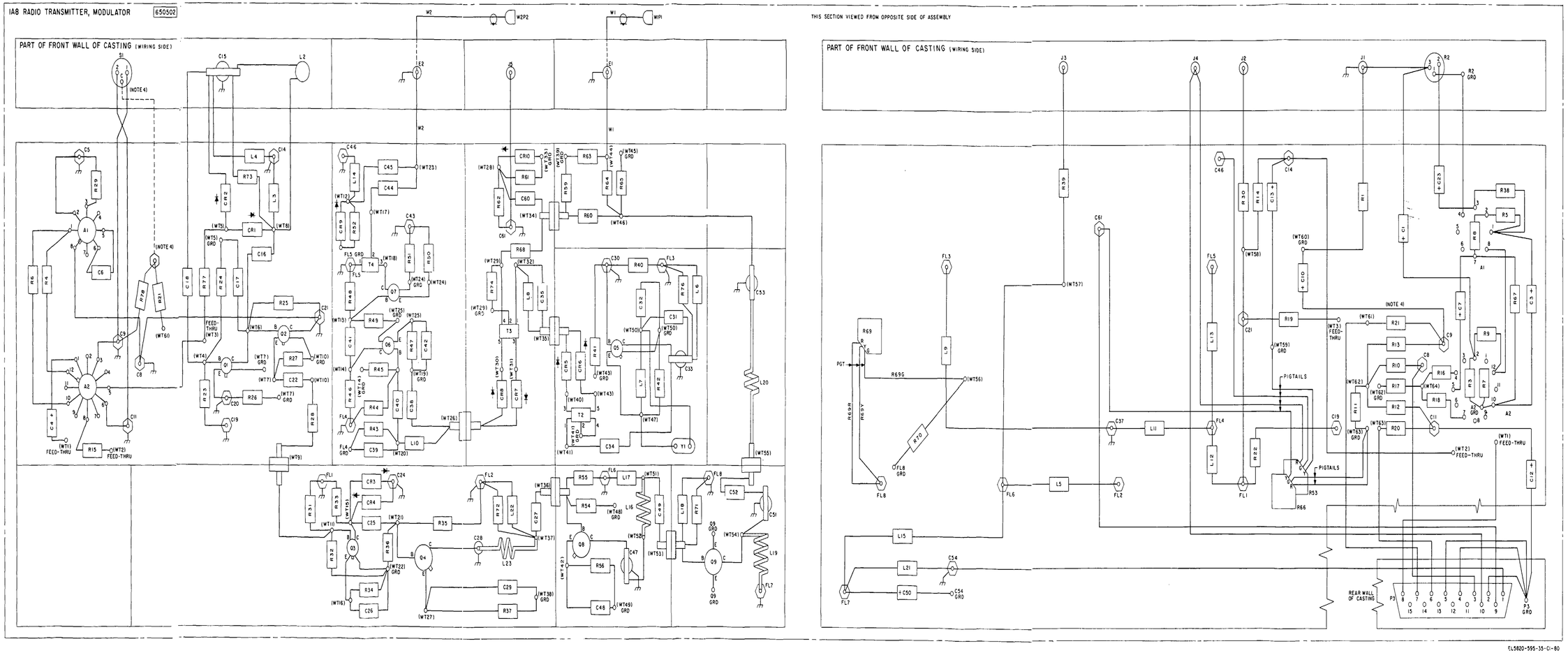


Figure 8-80. Modulator 1A8, wiring diagram.

Change 1

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A8.
2. IN SOME COMPONENTS, RESISTOR R78 IS ADDED AND SWITCH S1 IS SPDT. IN THESE CASES RESISTOR R21 IS LOCATED ON THE ASSEMBLY BOTTOM.

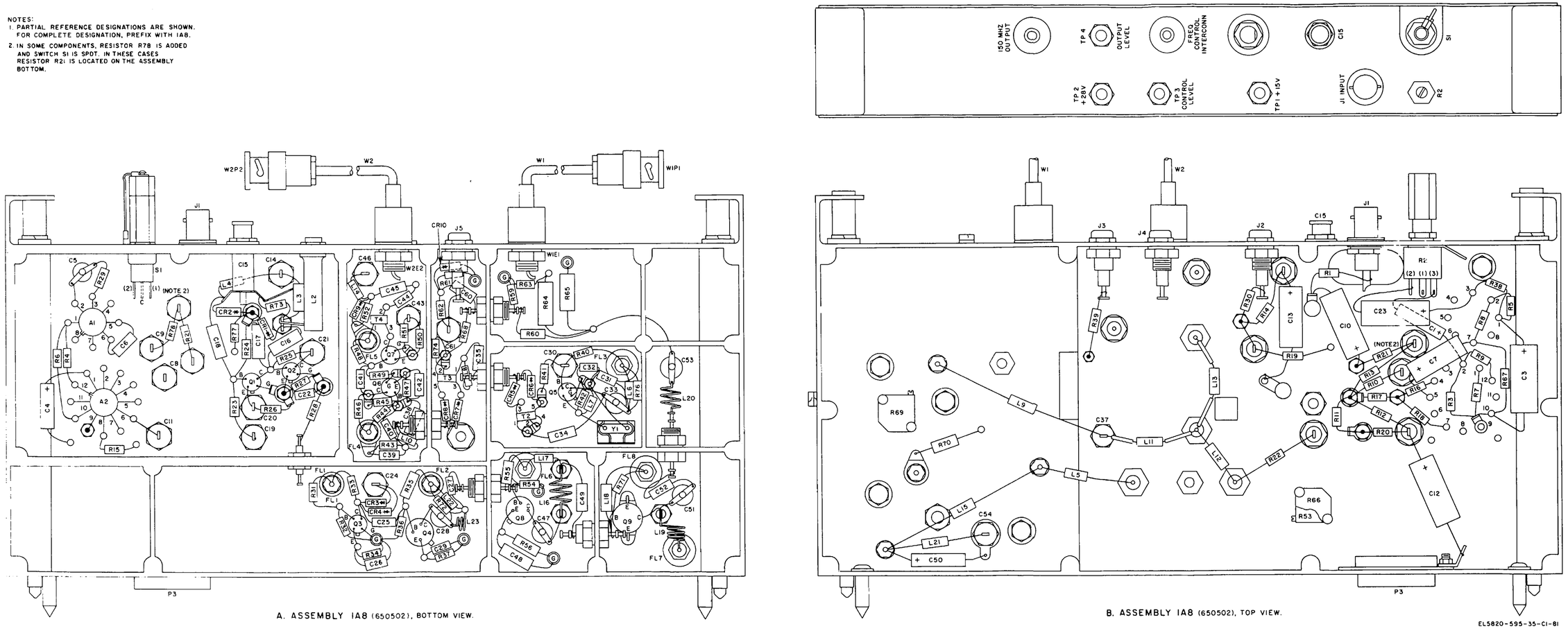


Figure 8-81. Modulator 1A8, parts location diagram.

Change 1

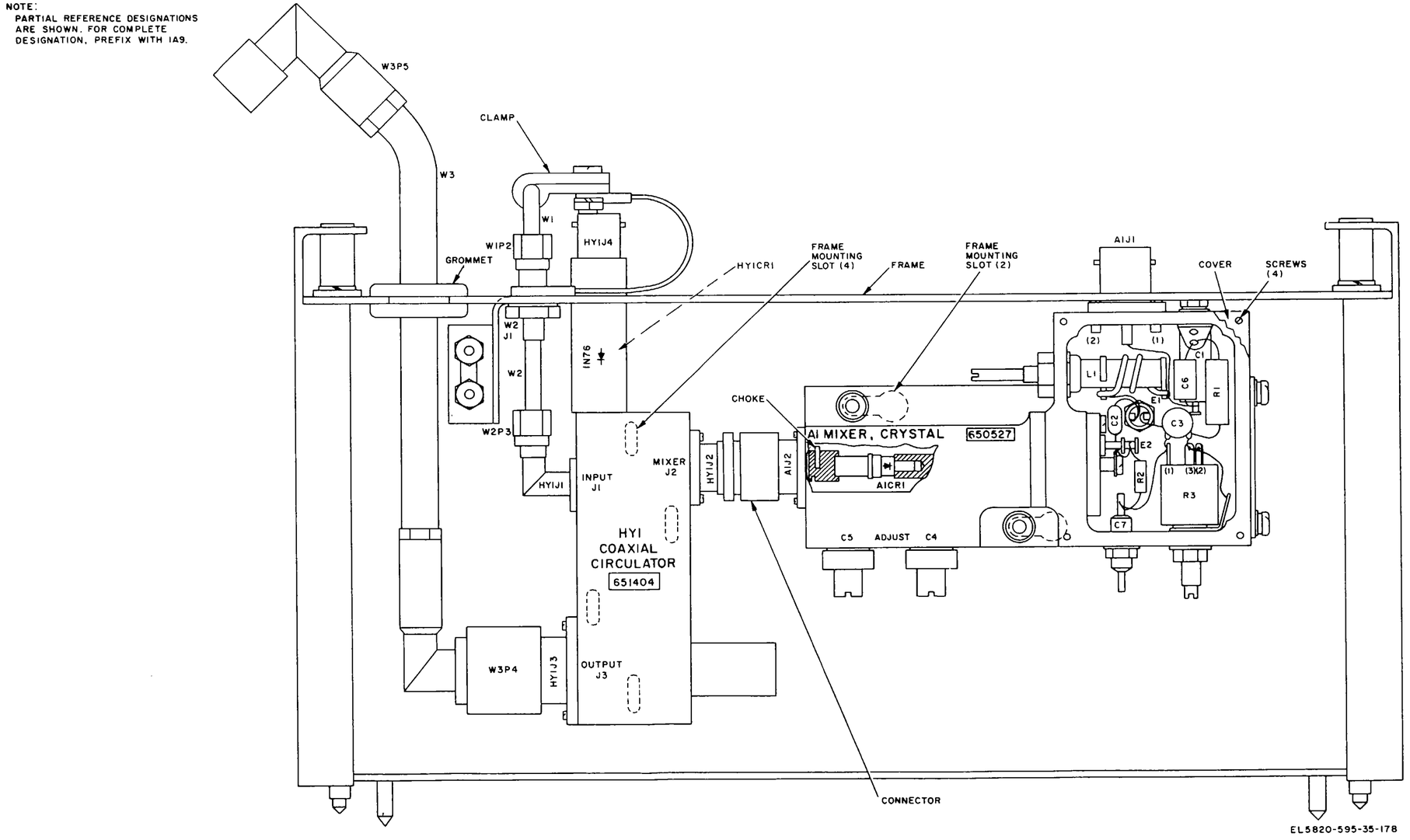


Figure 8-82. Frequency mixer 1A9, parts location diagram.

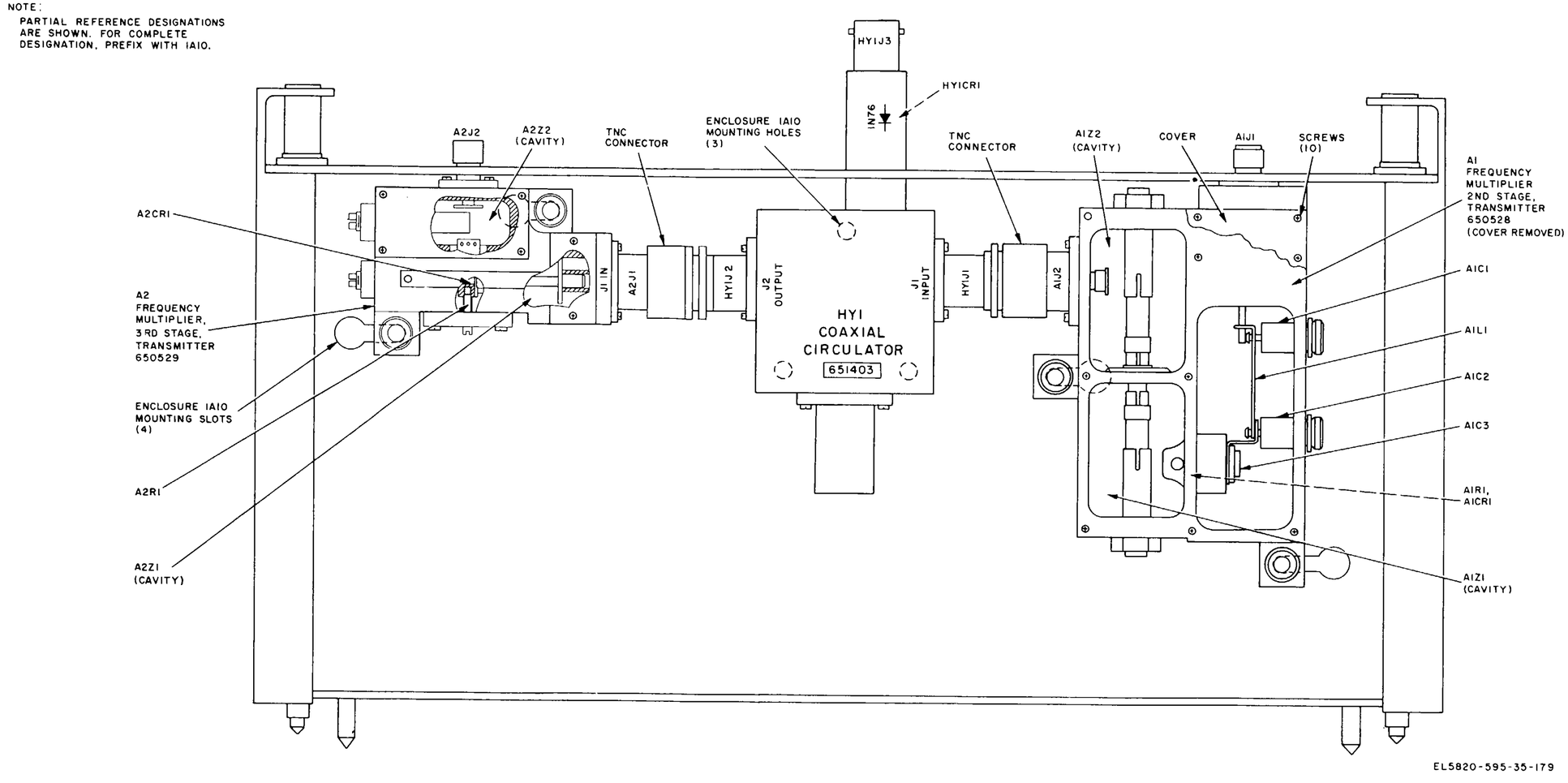
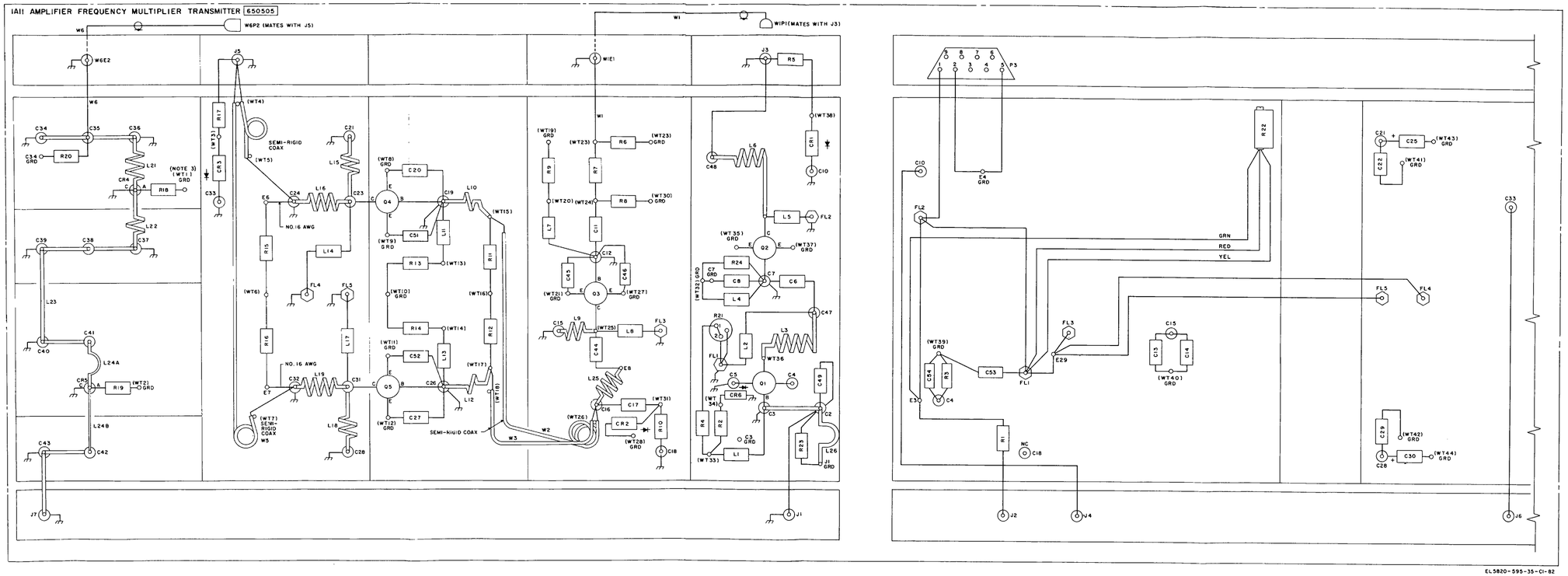


Figure 8-83. Frequency multiplier group 1A10, parts location diagram.

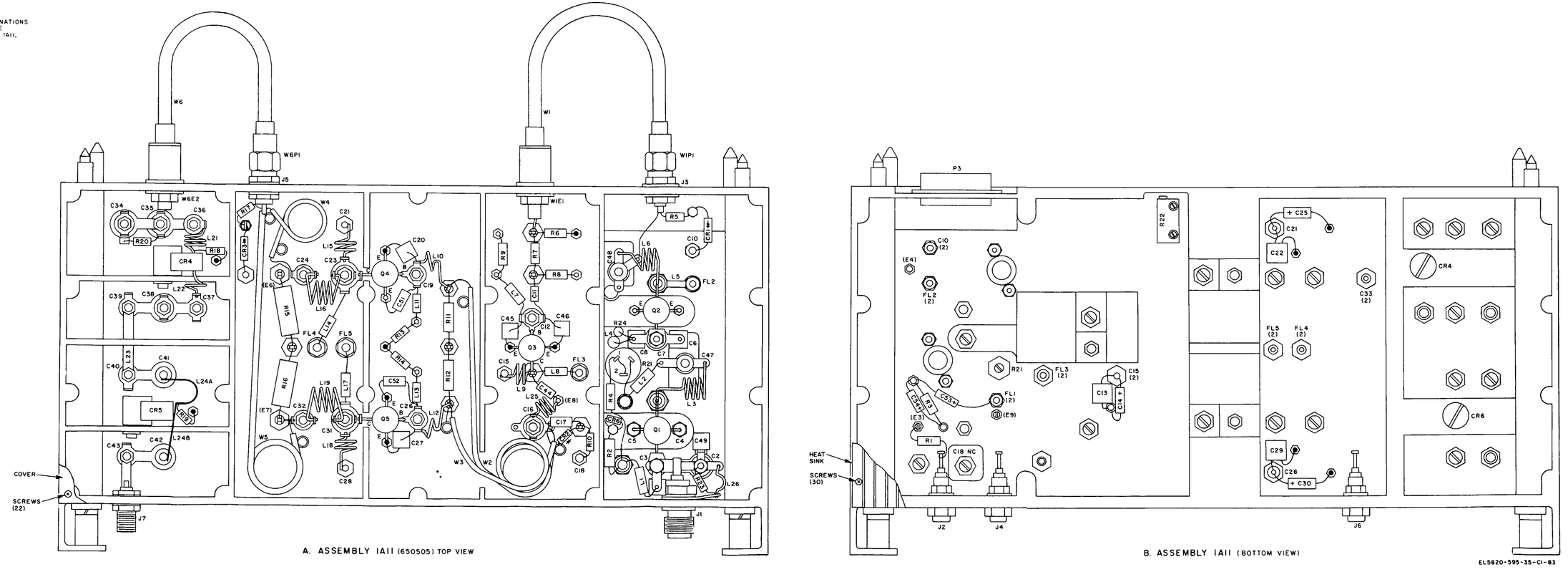
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER.
2. ALL WIRE IS NO.22 AWG STRANDED, TEFLON INSULATED; UNLESS OTHERWISE SPECIFIED.
3. WIRING TIEPOINT TERMINAL NUMBERS (WT—) ARE ASSIGNED FOR IDENTIFICATION PURPOSES ONLY; THEY ARE NOT MARKED ON EQUIPMENT.



Change 1

Figure 8-84. Amplifier-frequency multiplier 1A11, wiring diagram.

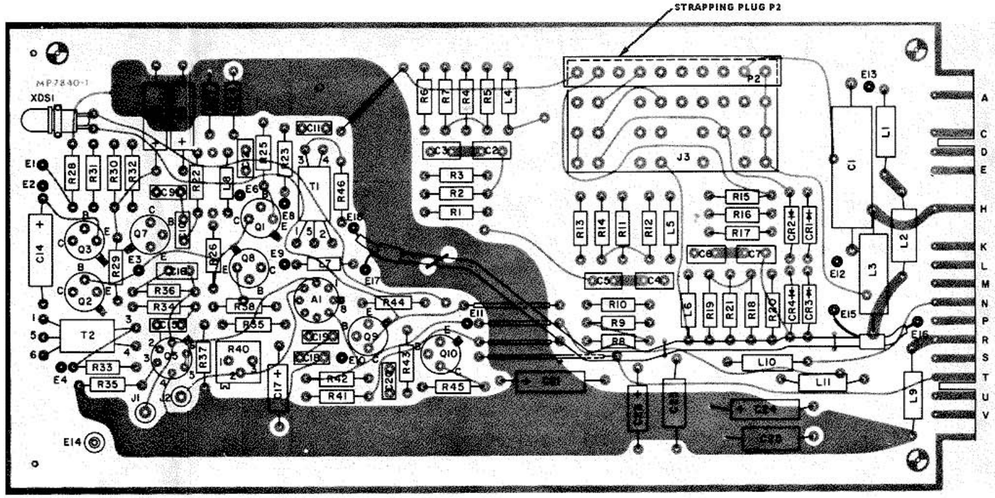
NOTE
PARTIAL REFERENSE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A11.



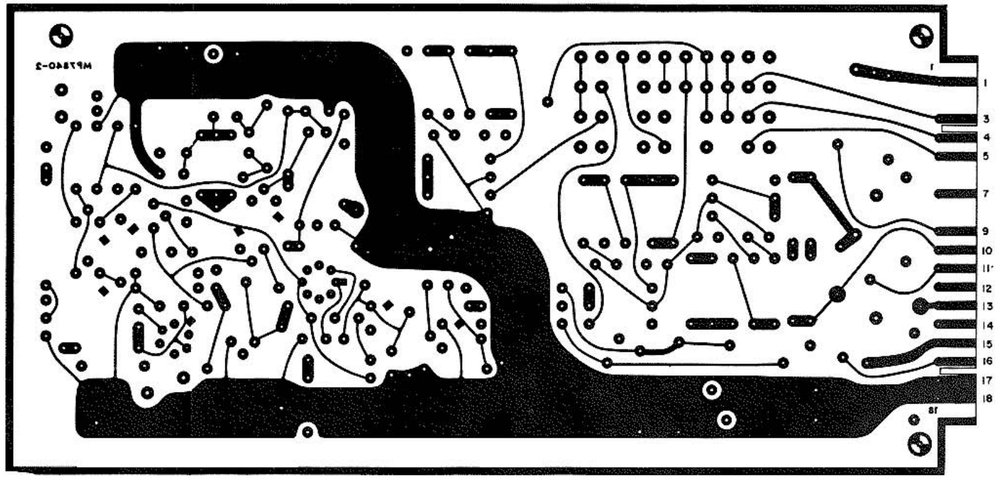
Change 1

Figure 8-85. Amplifier-frequency multiplier 1A11, parts location diagram.

NOTE: PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A121A.



A. PARTS AND WIRING ON FRONT OF BOARD A2 (650539).

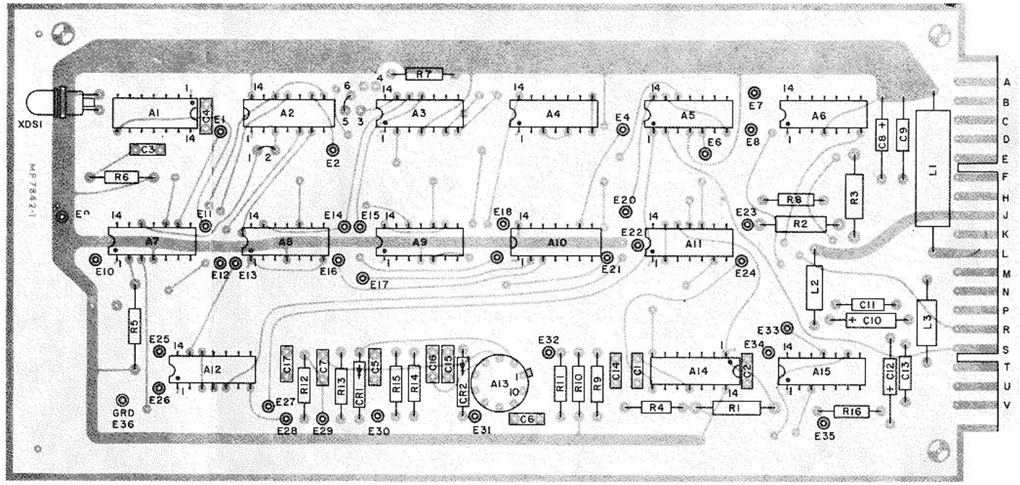


B. WIRING ON BACK OF BOARD A2 (VIEWED THROUGH FRONT).

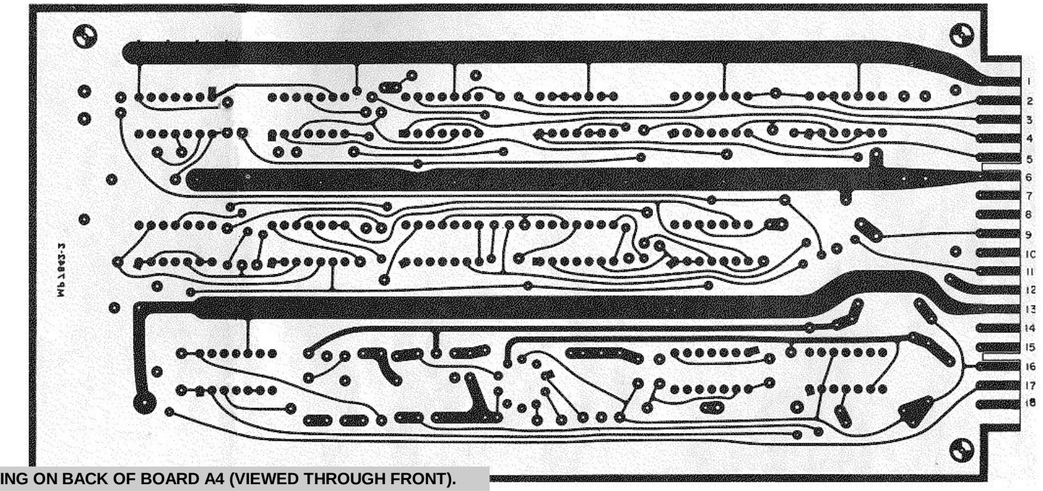
Figure 8-86. Cable digital regenerator 1A12A2, parts location and printed wiring diagram.

NOTE;

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A4



A. PARTS AND WIRING ON FRONT OF BOARD A4 (650542)

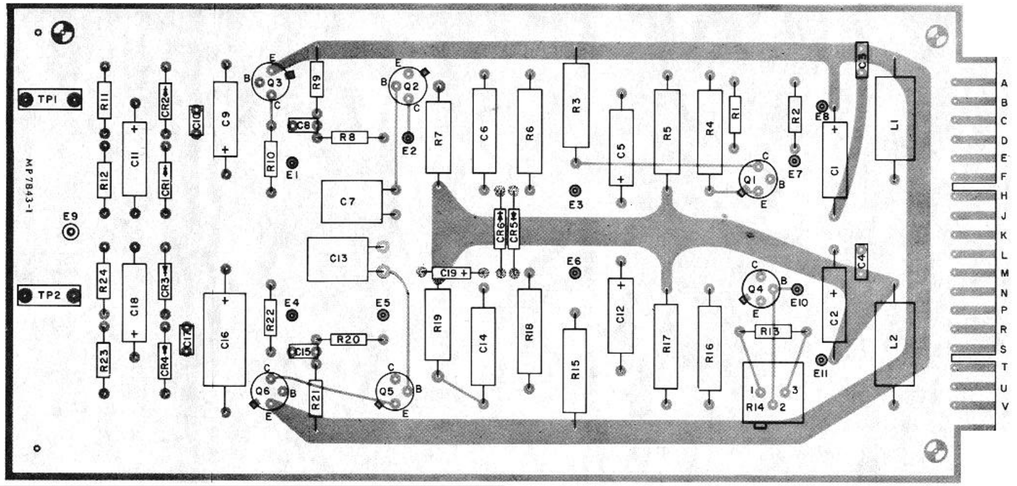


B. WIRING ON BACK OF BOARD A4 (VIEWED THROUGH FRONT).

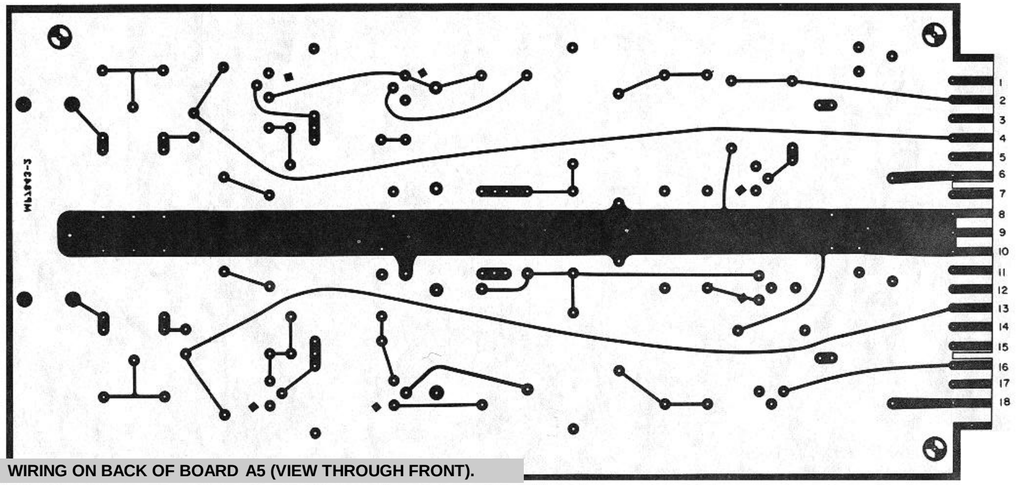
Figure 8-88. Cable digital processor 1A12A4 parts location and printed wiring diagram.

NOTE;

PARTIAL REFERENCE DESIGNATIONS A RE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A12A5



A. PARTS AND WIRING ON FRONT OF BOARD A5 (650543).

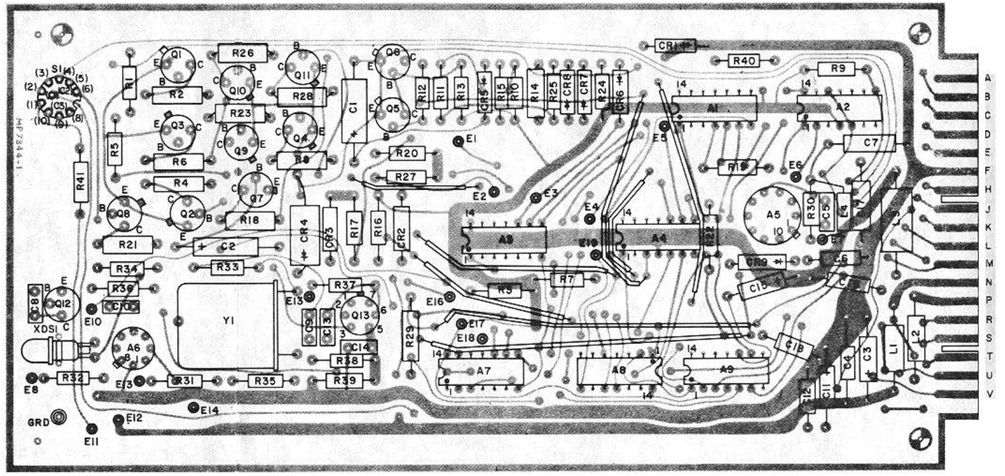


b. WIRING ON BACK OF BOARD A5 (VIEW THROUGH FRONT).

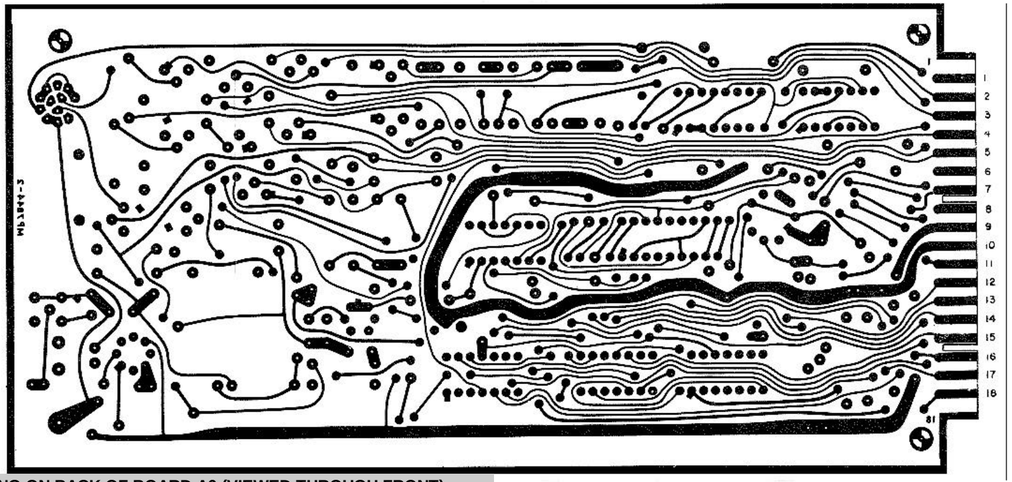
Figure 8-89. AF amplifier 1A12A5, parts location and printed wiring diagram.

NOTE;

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A12A6.



A. PARTS AND WIRING ON FRONT OF BOARD (650545)/

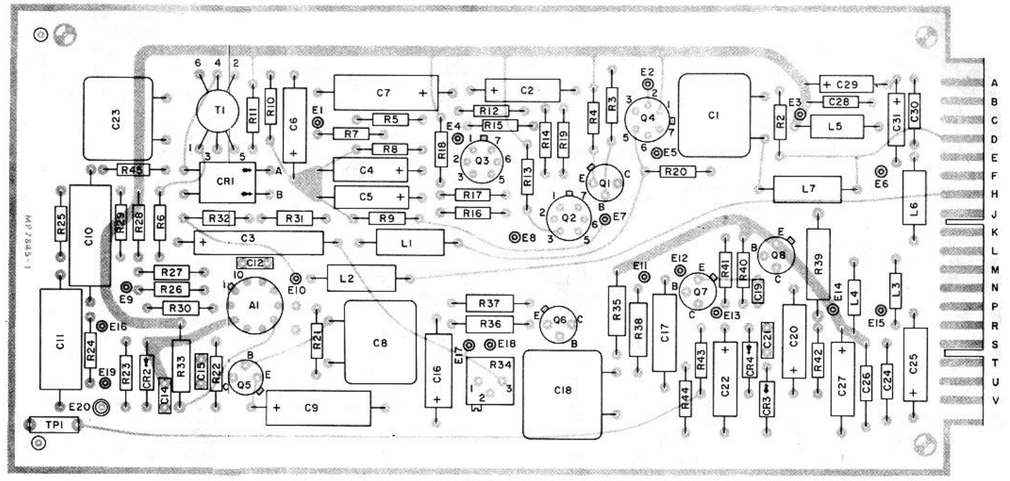


B. WIRING ON BACK OF BOARD A6 (VIEWED THROUGH FRONT).

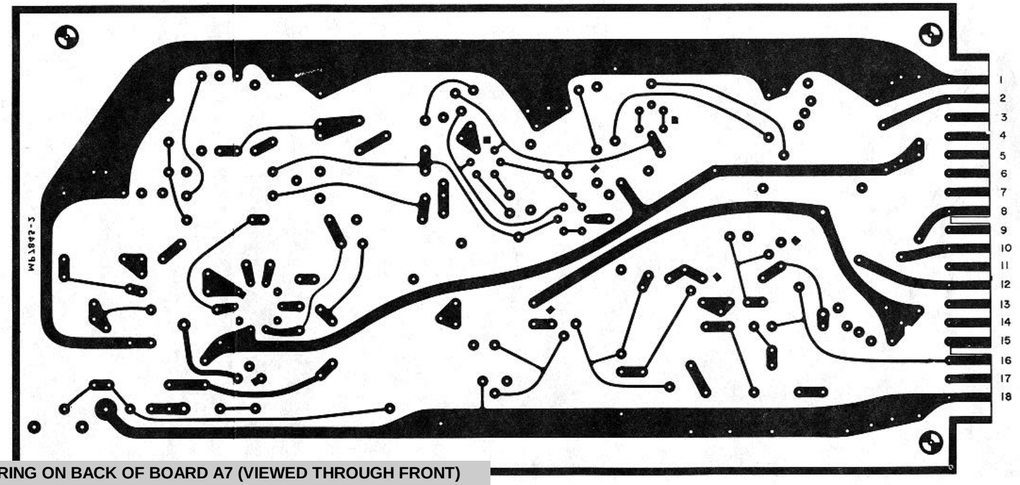
Figure 8-90. Alarm monitor 1A12A6, parts location and printed wiring diagram.

NOTE;

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A12A7.



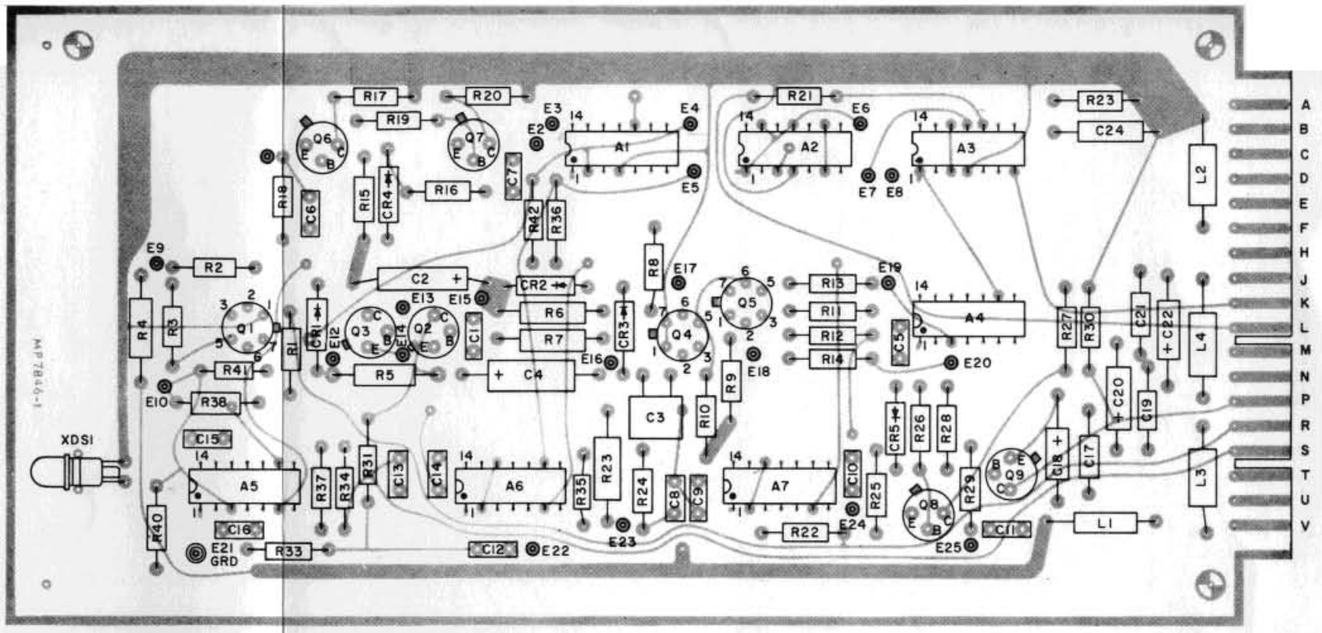
A. PARTS AND WIRING ON FRONT OF BOARD A7 (650547)



B. WIRING ON BACK OF BOARD A7 (VIEWED THROUGH FRONT)

Figure 8-91. Amplifier-detector 1A12A7, parts location and printed wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A8.



A. PARTS AND WIRING ON FRONT OF BOARD A8 (650575)

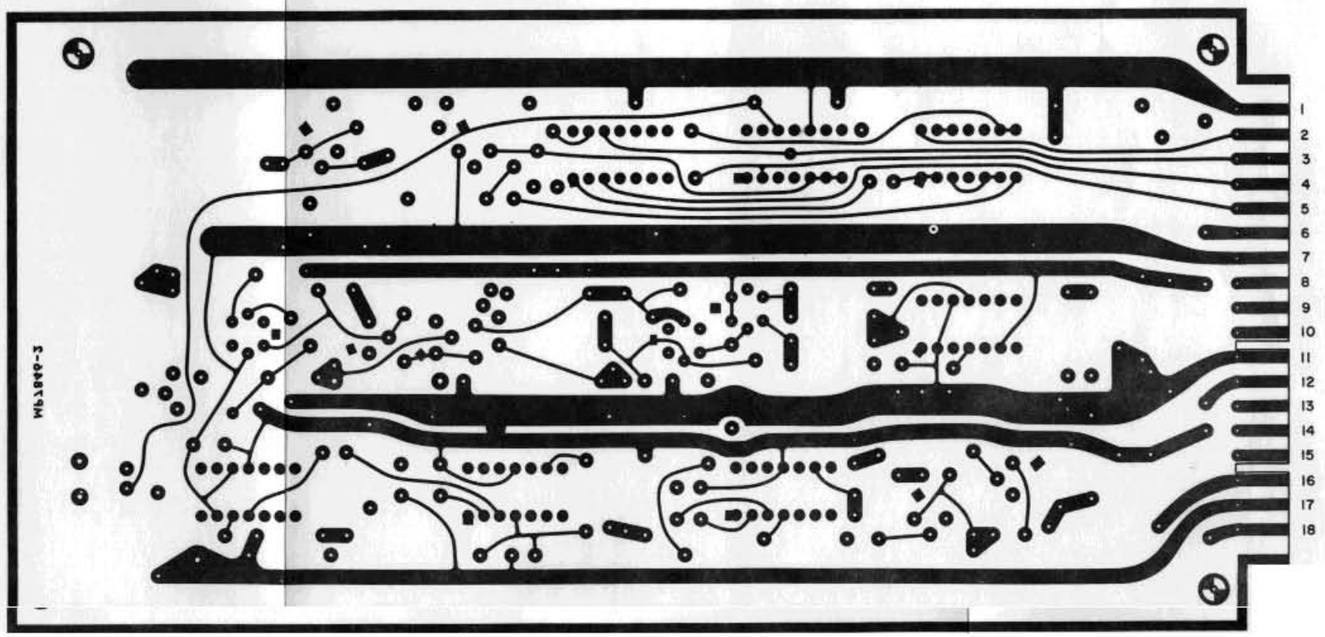
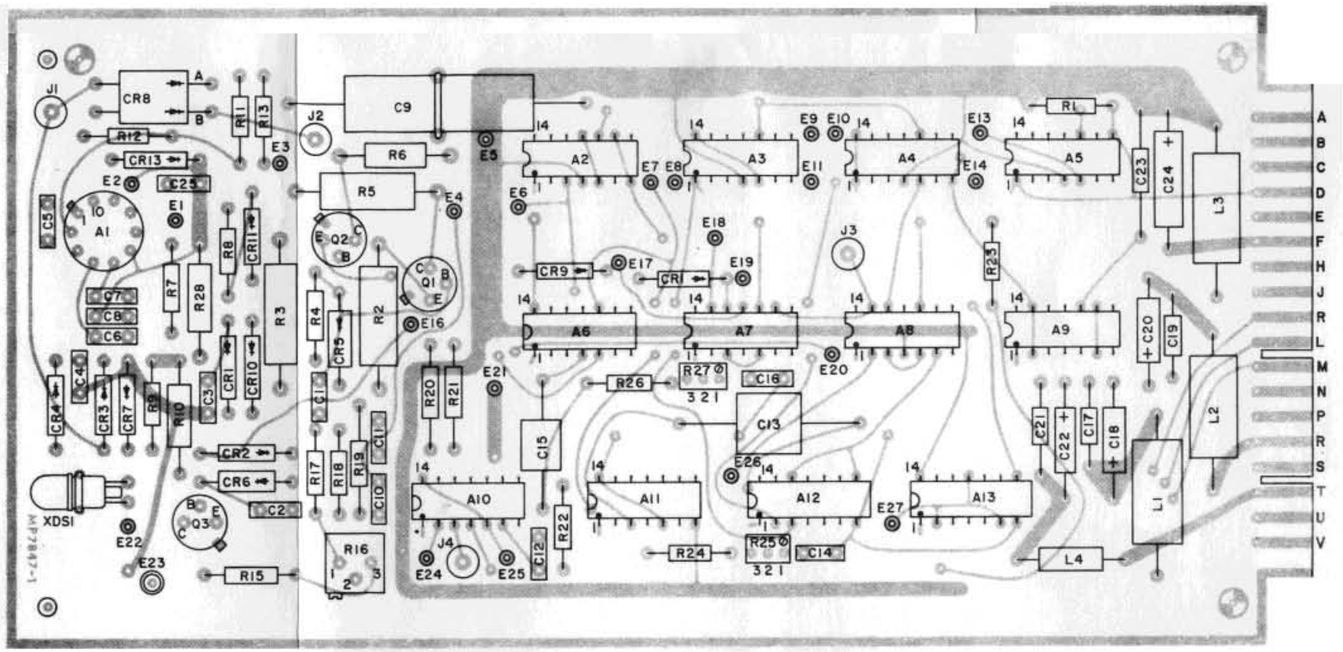


Figure 8-92. Radio digital regenerator 1A12A8, parts location and printed wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A9.



A. PARTS AND WIRING ON FRONT OF BOARD A9 (650576)

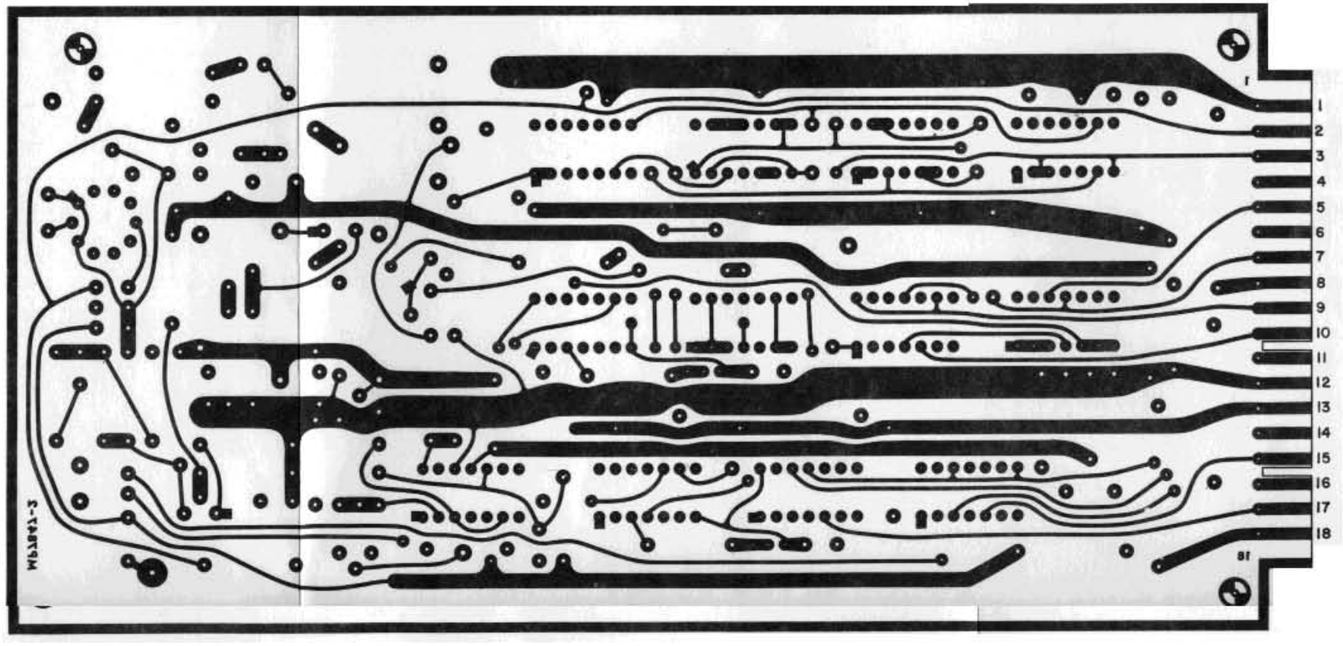
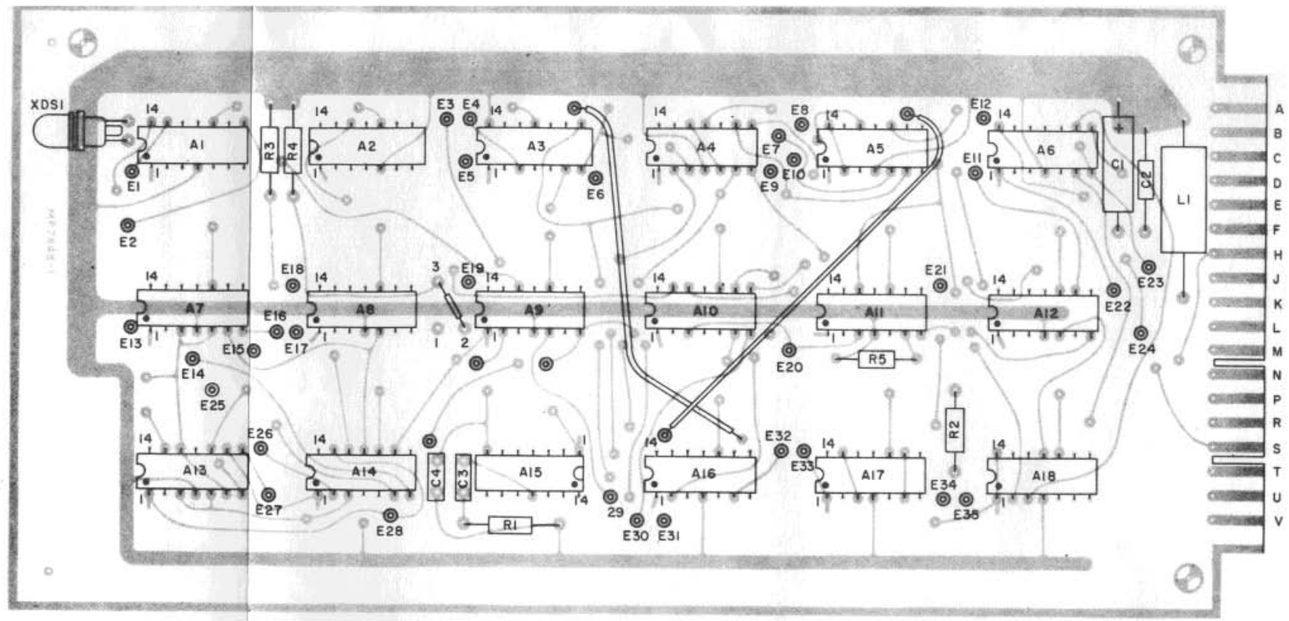


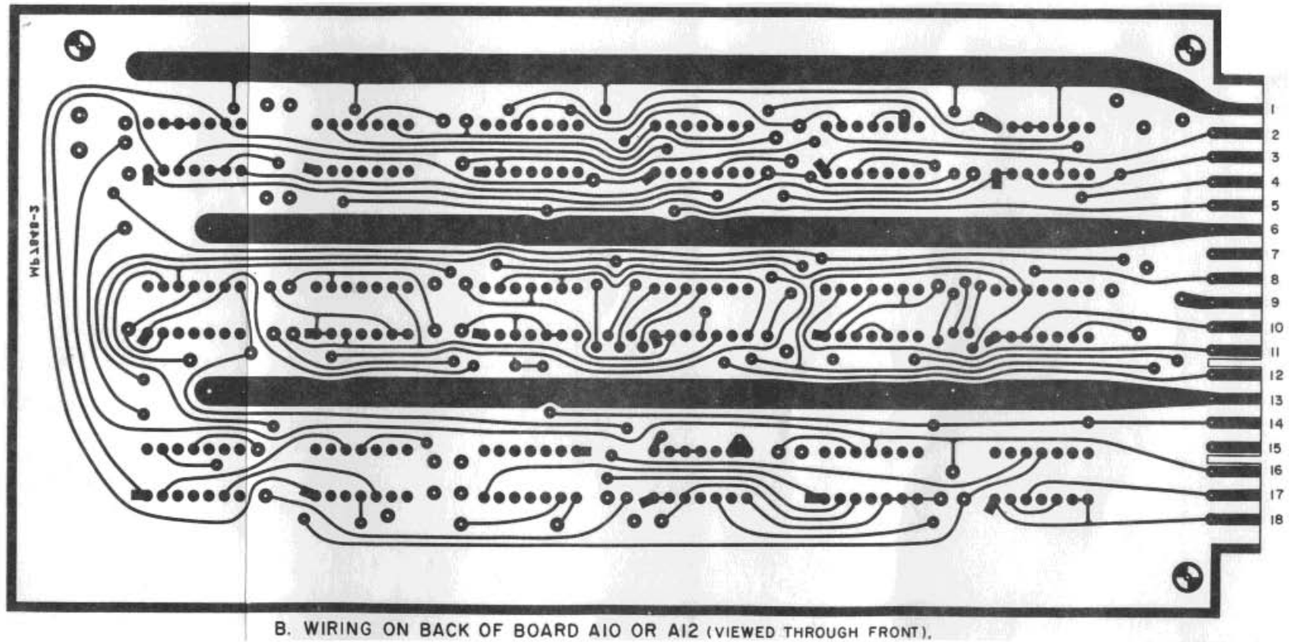
Figure 8-93. Radio digital regenerator 1A12A8, parts location and printed wiring diagram.

NOTE:

THIS IS A MULTIPLE USE ASSEMBLY.
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH
1A12A10 OR 1A12A12.



A. PARTS AND WIRING ON FRONT OF BOARD A10 OR A12 (650577).



B. WIRING ON BACK OF BOARD A10 OR A12 (VIEWED THROUGH FRONT).

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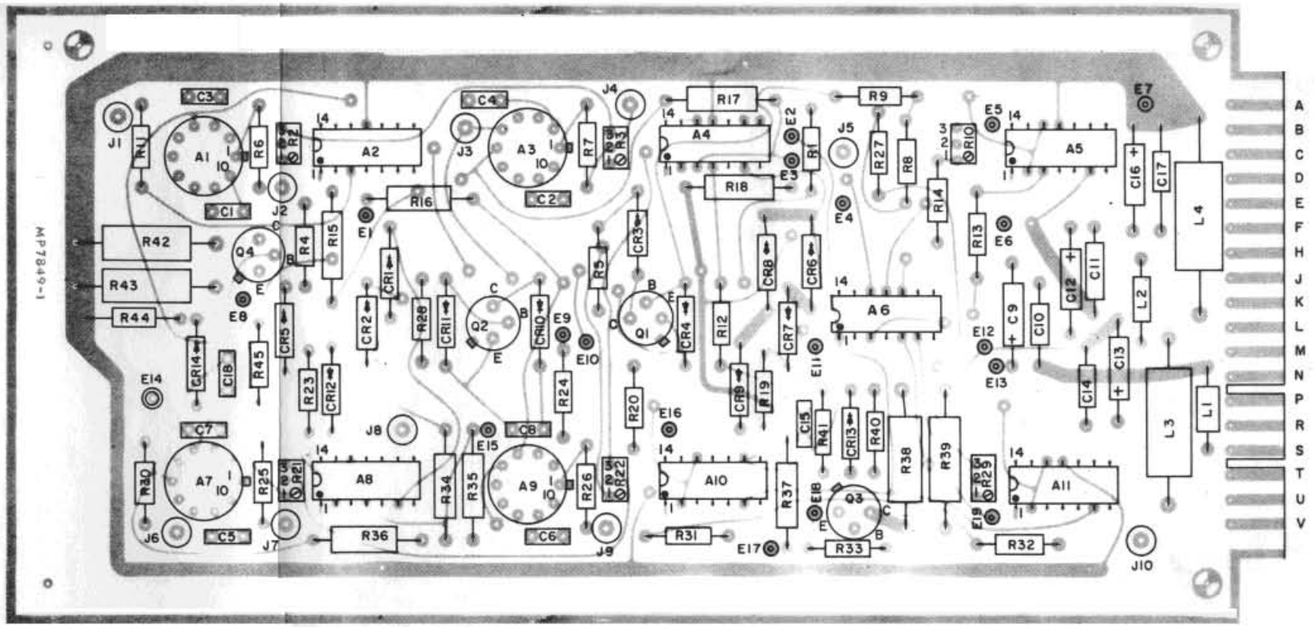
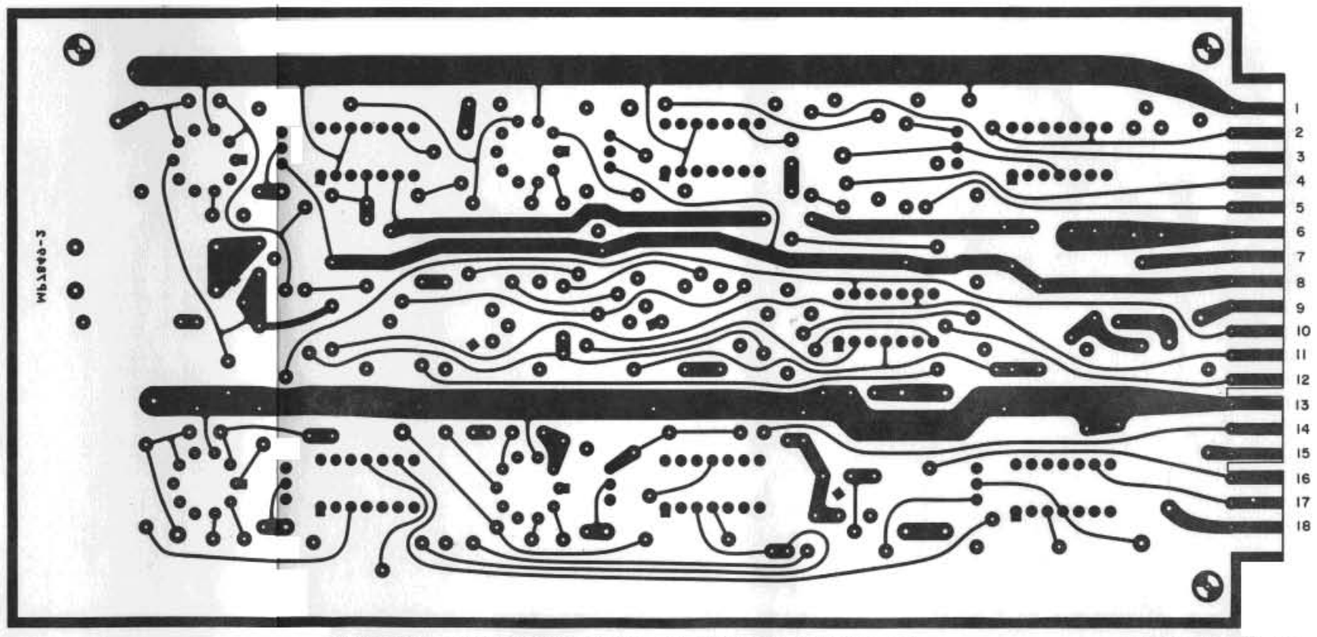
Figure 8-94. Control processor No. 1, 1A12A10 and No. 2, 1A12A12, parts location and printed wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A11.



A. PARTS AND WIRING ON FRONT OF BOARD A11 (650578)

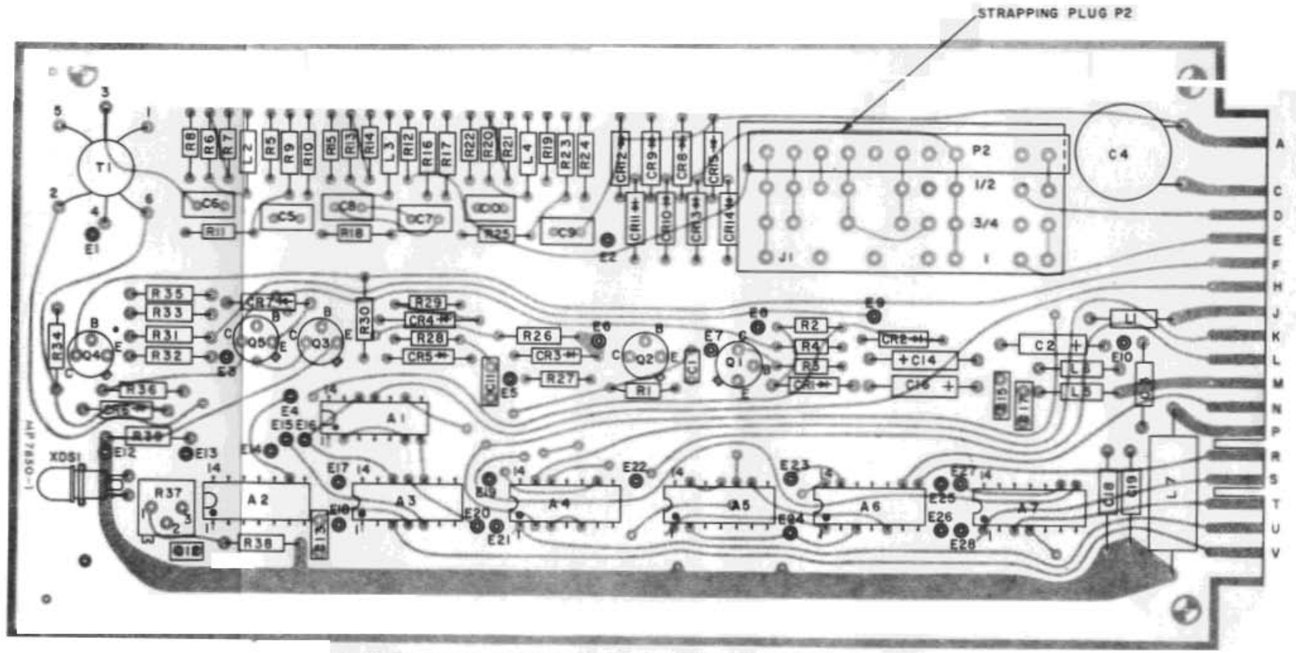


B. WIRING ON BACK OF BOARD A11 (VIEWED THROUGH FRONT) EL5820-595-35-190

Figure 8-95. Pulse decoder 1A12A11, parts location and printed wiring diagram.

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A12A13.



A. PARTS AND WIRING ON FRONT OF BOARD A13 (650579).

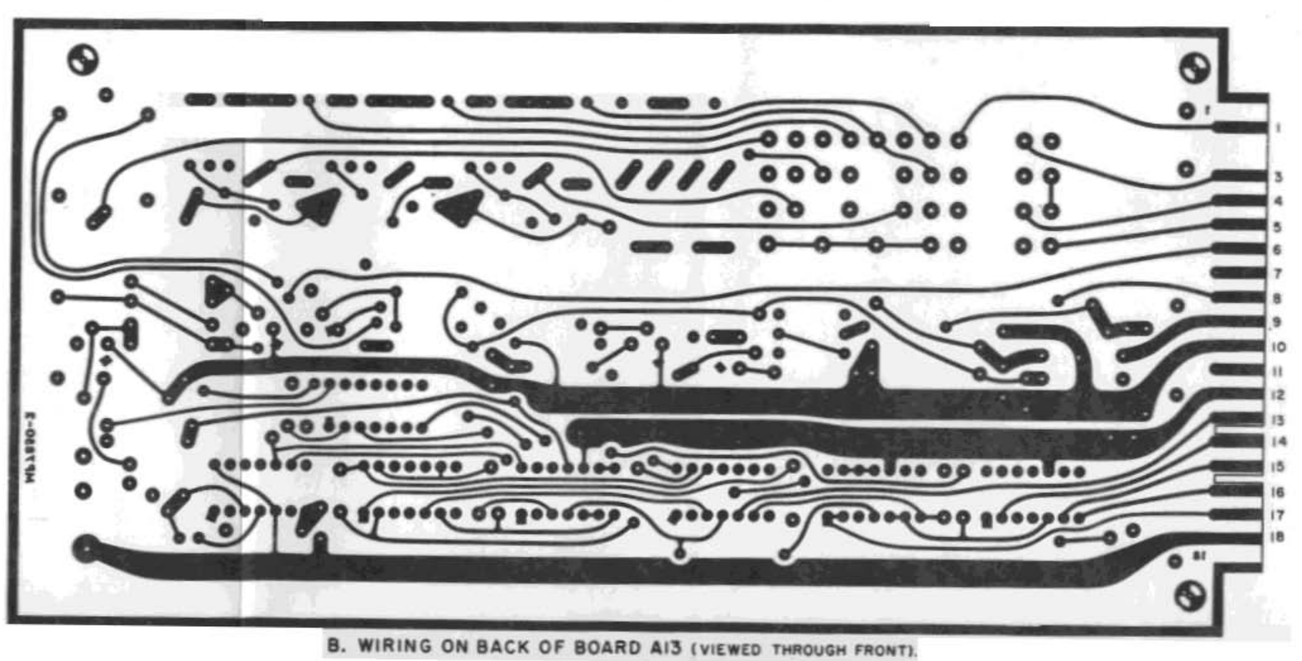
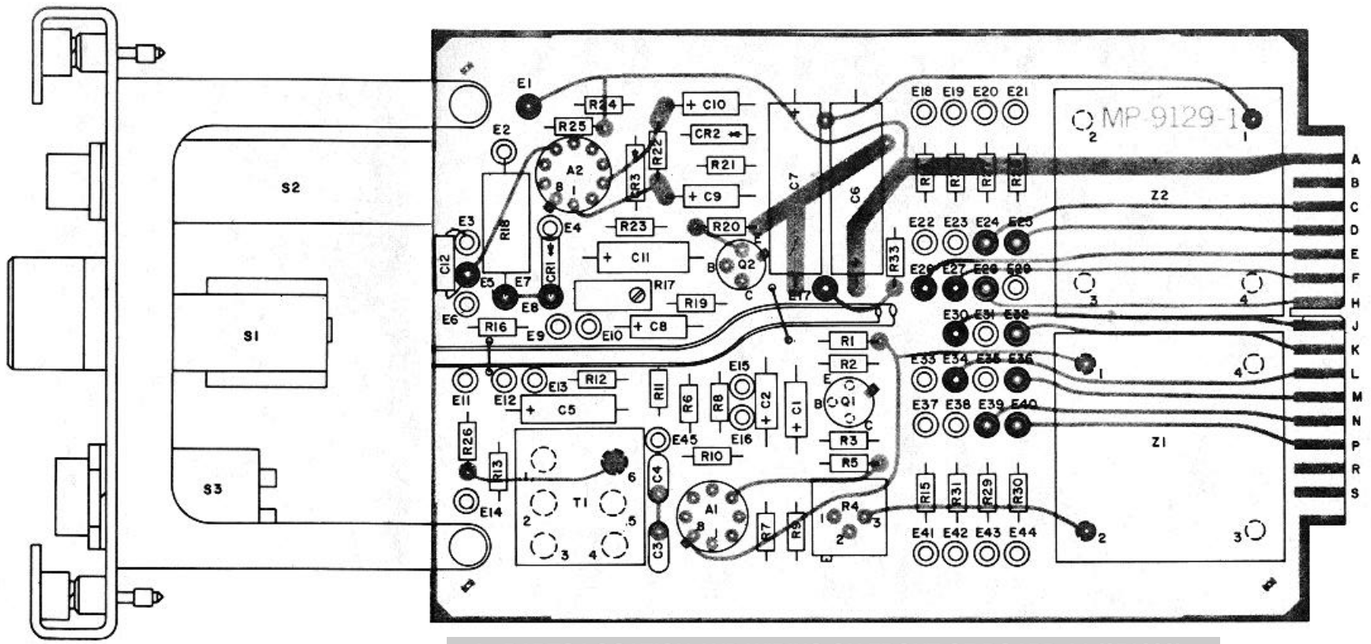
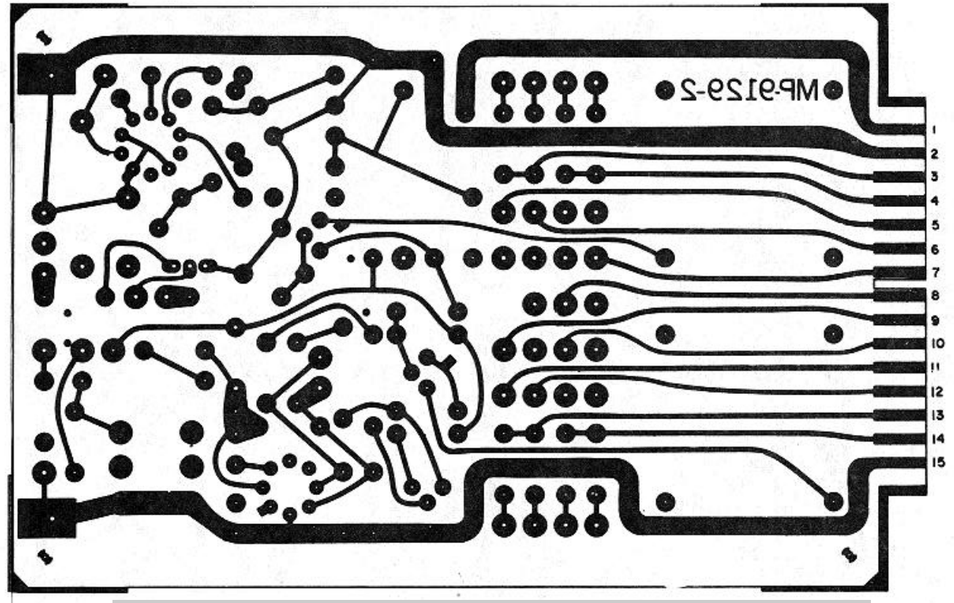


Figure 8-96. Radio digital processor 1A12A13, parts location and printed wiring diagram.



A. PARTS LOCATION AND WIRING ON FRONT OF BOARD A1 (651609).



B. WIRING N BACK OF BOARD A1 (VIEWED THROUGH FRONT).

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A1.

Figure 8-97. Board No. 1, 1A13A1, parts location and printed wiring diagram.
Change 1

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 24 AWG STRANDED, TEFLON INSULATED.
3. SWITCH IS VIEWED FROM END OPPOSITE CONTROL KNOB. SECTION A IS CLOSEST TO KNOB.

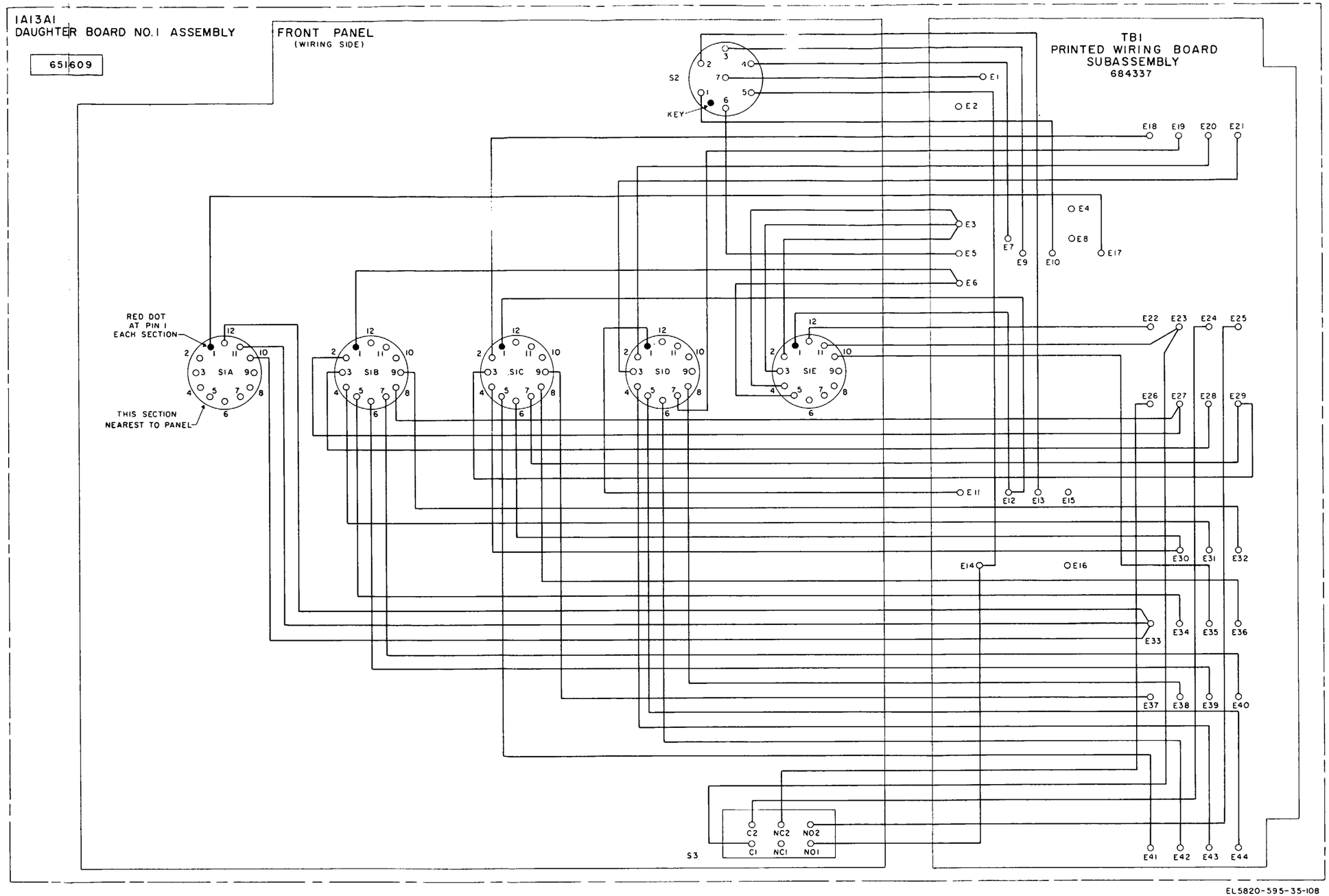
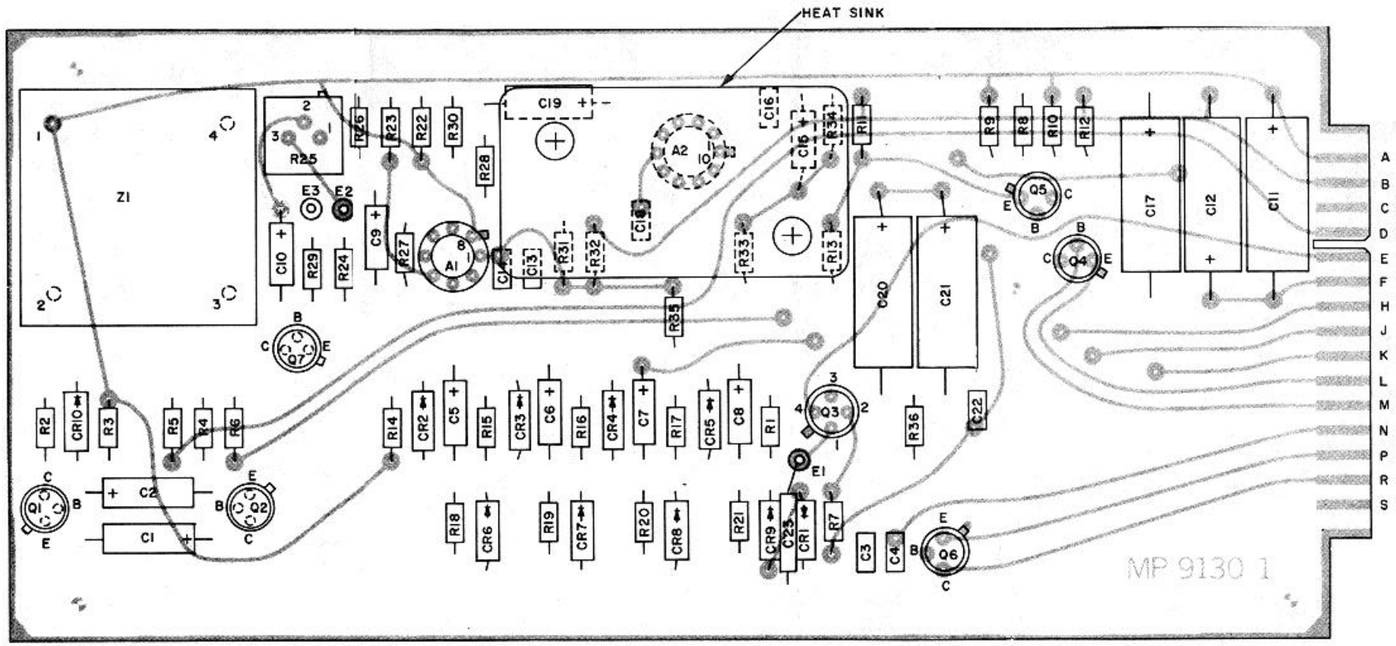


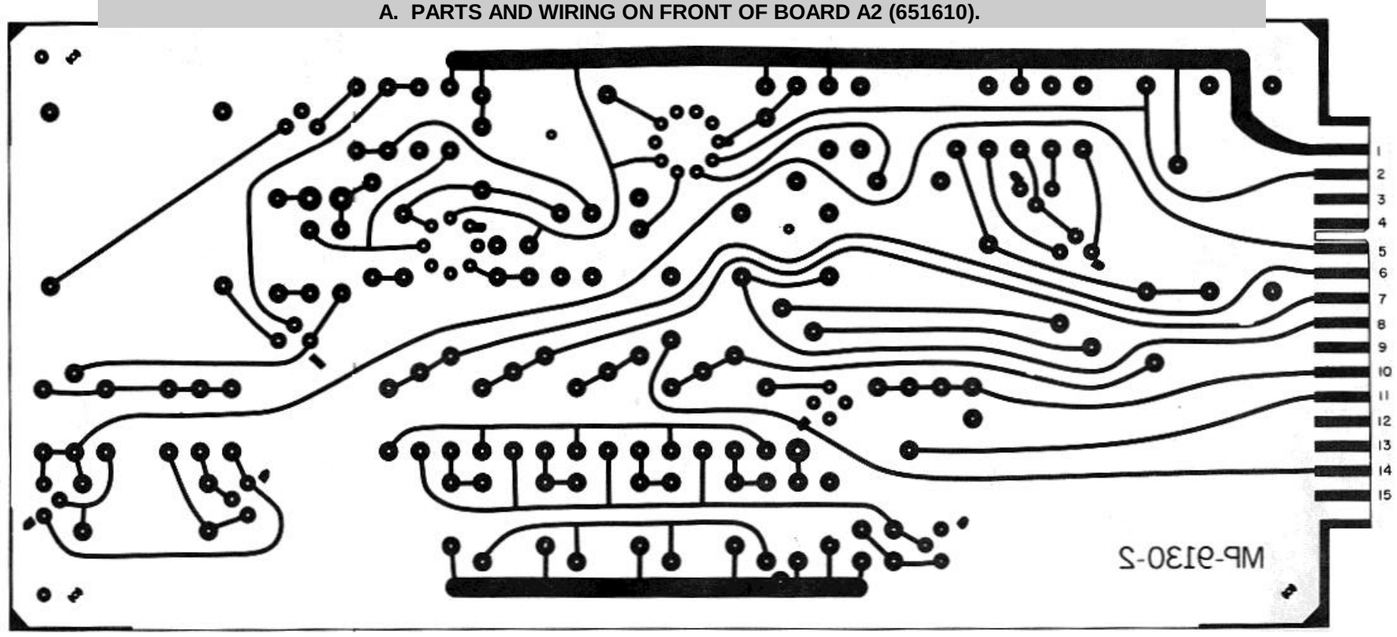
Figure 8-98. Board No. 1, 1A13A1, wiring diagram.

NOTE:

PARTIAL REFERENCE DESIG-NATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A2.



A. PARTS AND WIRING ON FRONT OF BOARD A2 (651610).

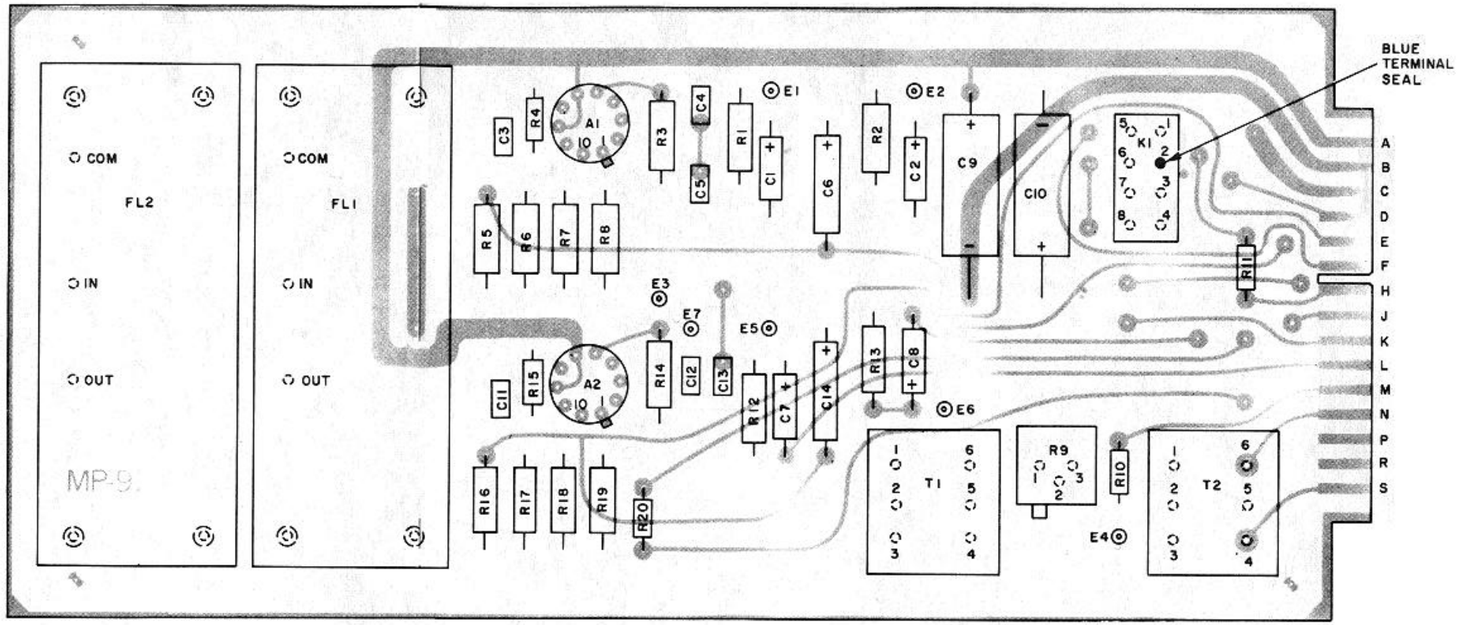


B. WIRING ON BACK OF BOARD A2 (viewed through front).

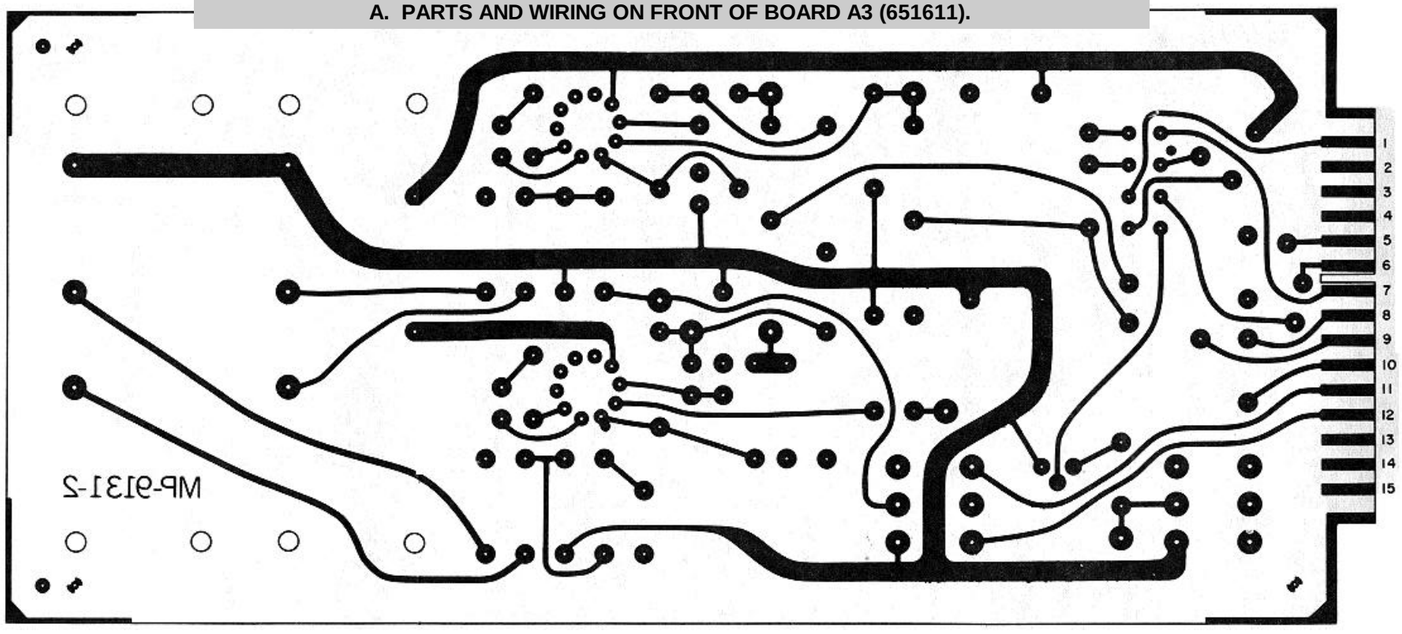
Figure 8-99. Board No. 2, 1A13A2, parts location and printed wiring diagram.

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A3.



A. PARTS AND WIRING ON FRONT OF BOARD A3 (651611).

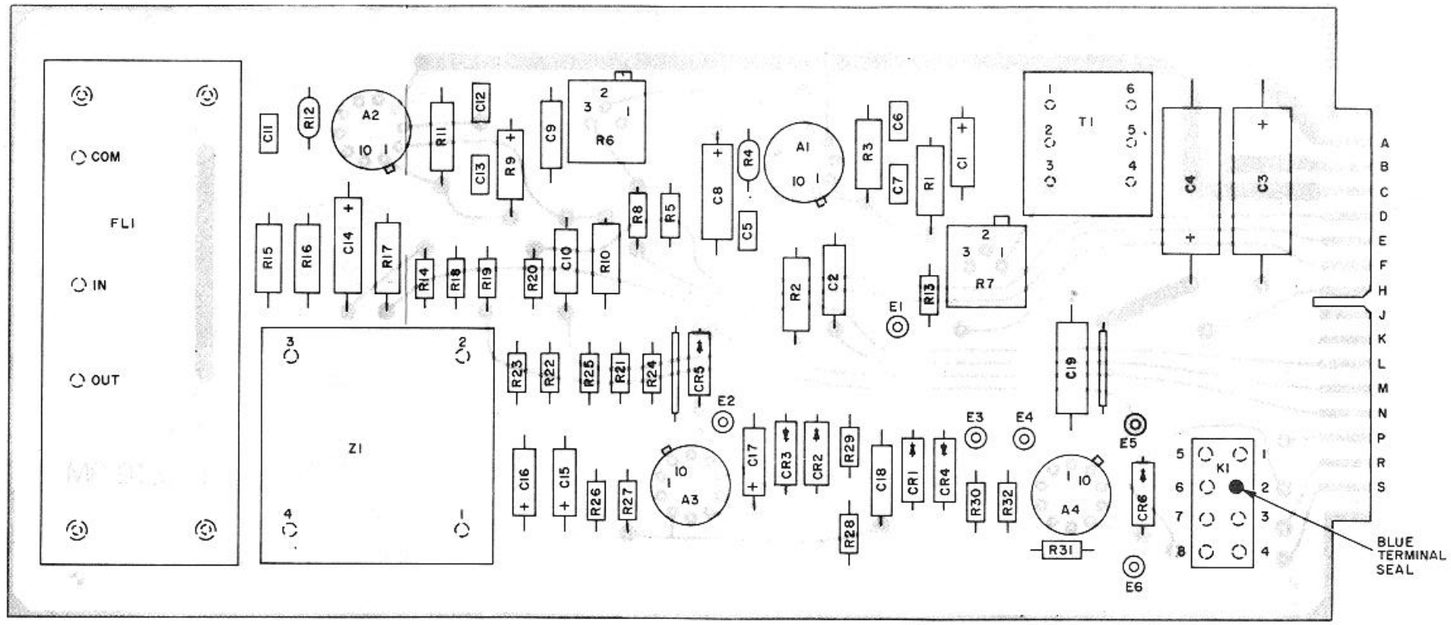


B. WIRING ON BACK OF BOARD A3 (VIEWED THROUGH FRONT).

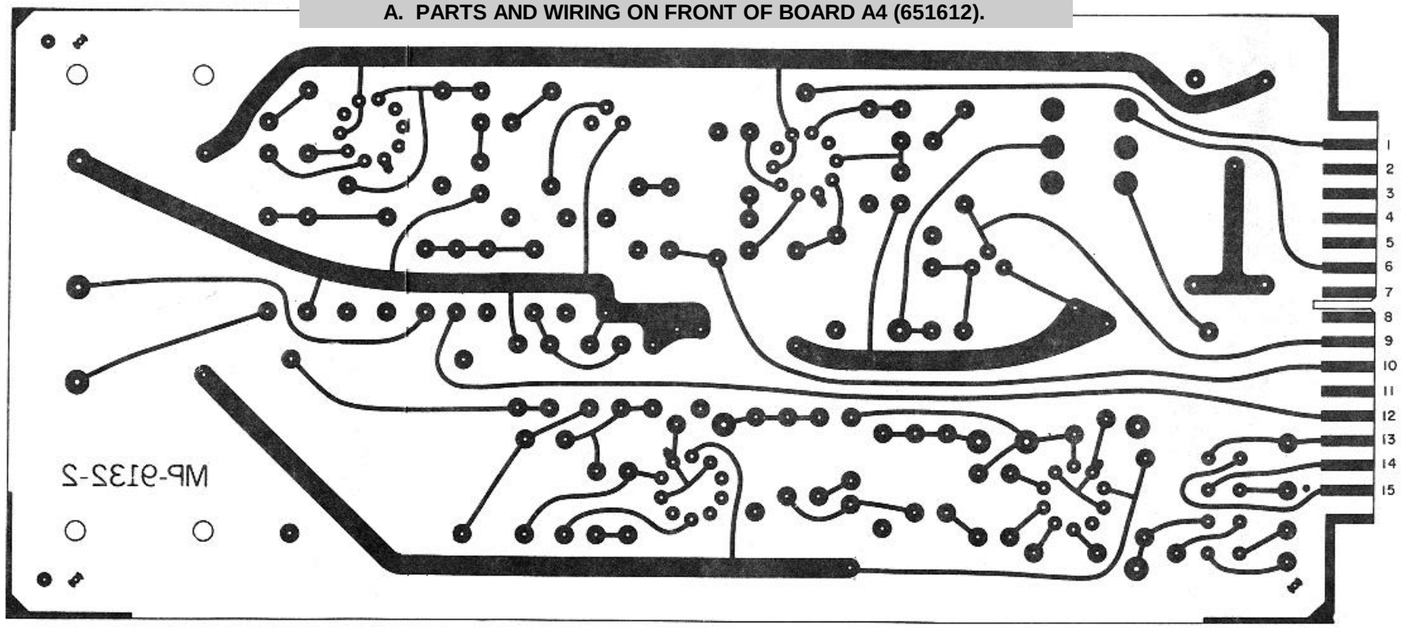
Figure 8-100. Board No. 3, 1A13A3, parts location and printed wiring diagram.

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A4.



A. PARTS AND WIRING ON FRONT OF BOARD A4 (651612).

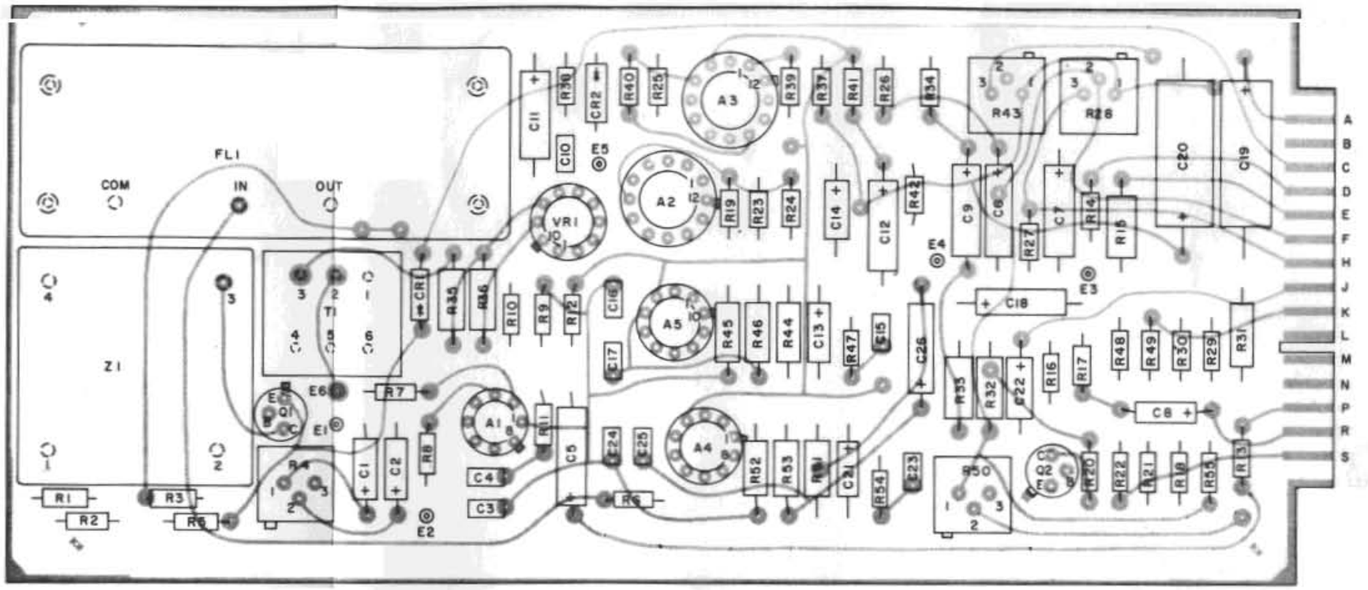


B. WIRING ON BACK OF BOARD A4 (VIEWED THROUGH FRONT).

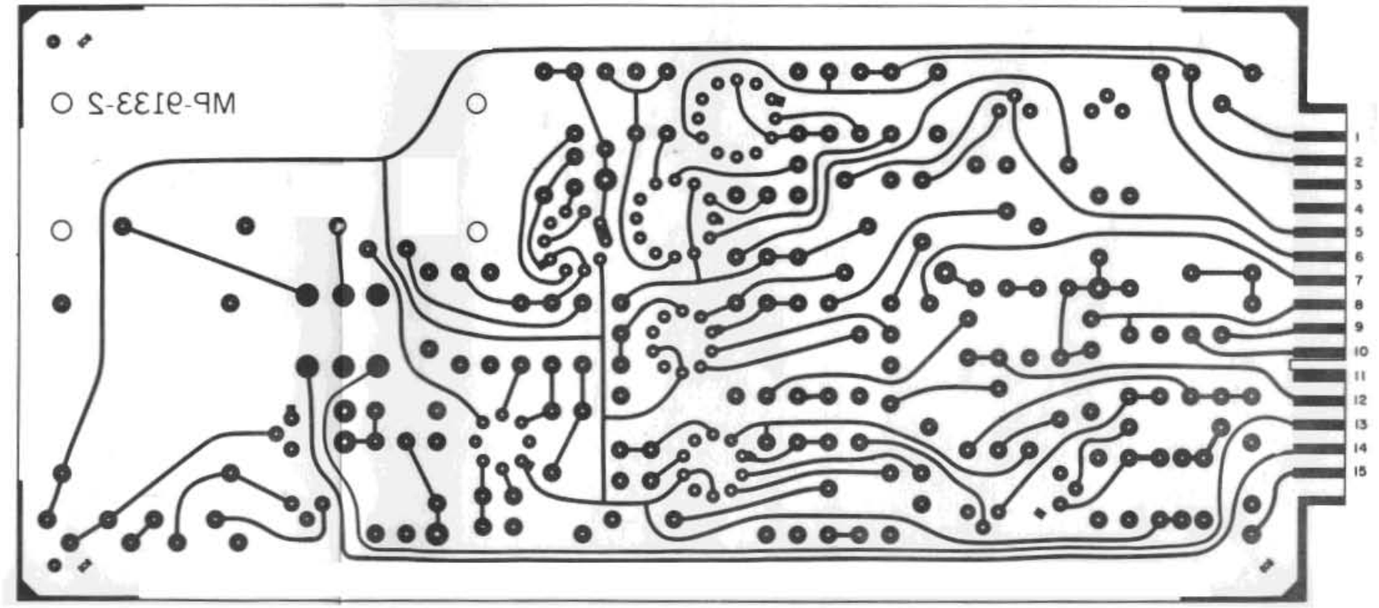
Figure 8-101. Board No. 4, 1A13A14, parts location and printed wiring diagram.

NOTE:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A13A5.



A. PARTS AND WIRING ON FRONT OF BOARD A5 (651613).



B. WIRING ON BACK OF BOARD A5 (VIEWED THROUGH FRONT).

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Figure 8-102. Board No. 5,1a13a5, parts location and printed wiring diagram.
Change 1

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED.

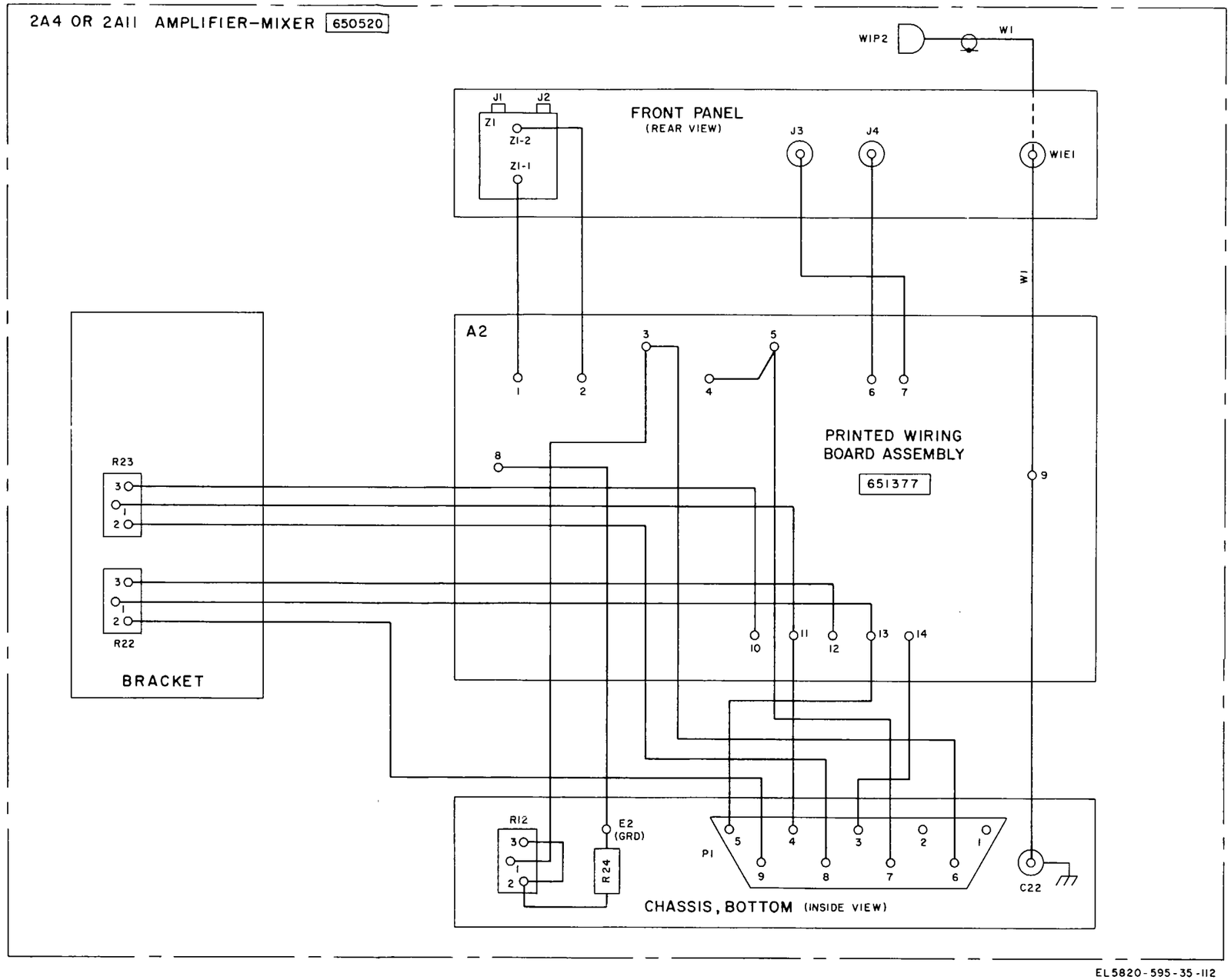
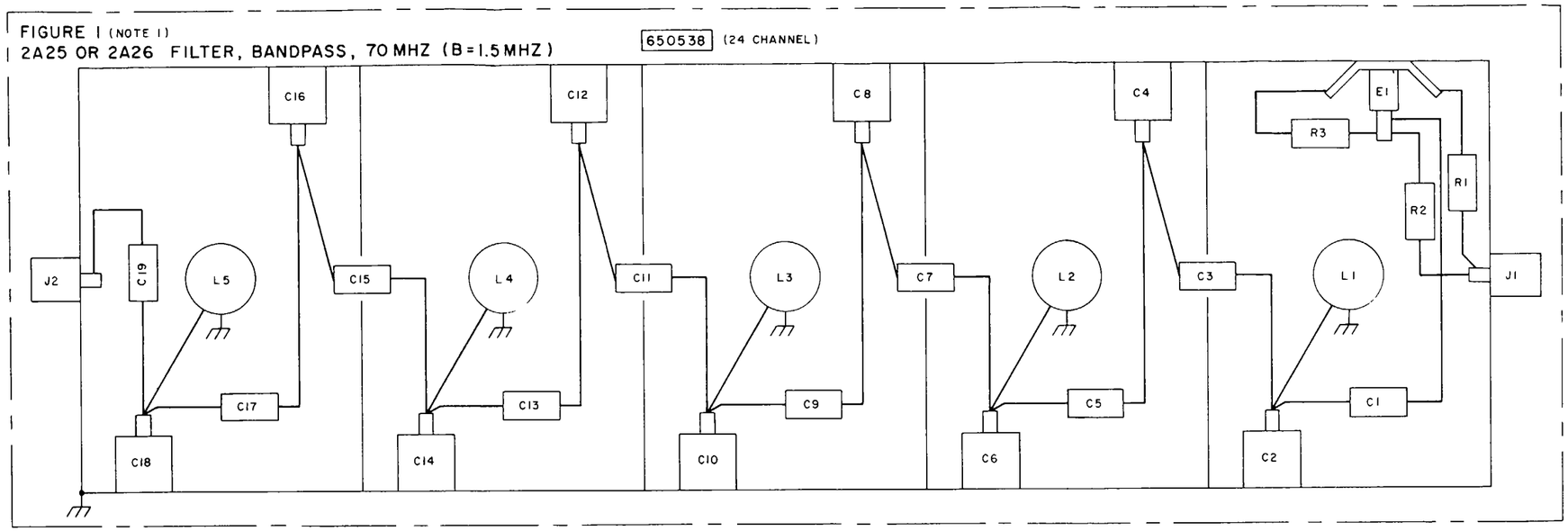


Figure 8-103. Mixer preamplifier 2A4/2A11, wiring diagram.

NOTES:

1. THIS DIAGRAM IS USED FOR BOTH FILTERS: FIGURE 1 (650538 (B=1.5MHZ) OR FIGURE 2 (650525 (B=750 KHZ)
2. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.



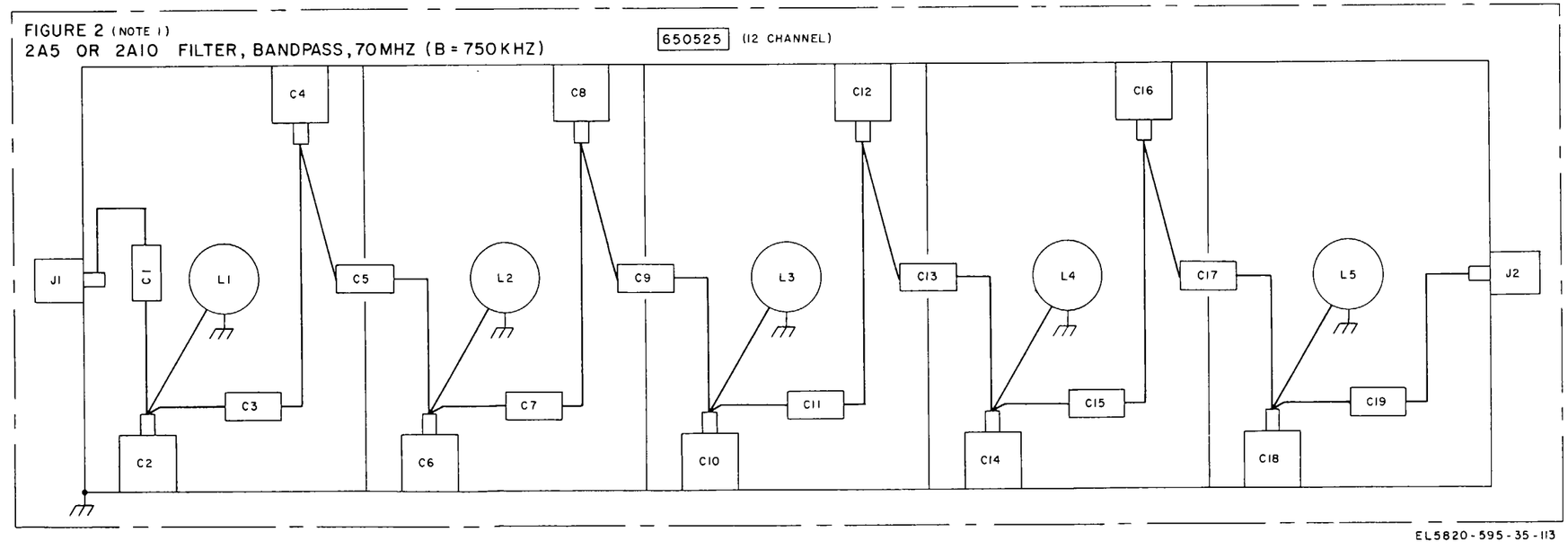


Figure 8-104. 70 MHz if filter 2A5/2A10, wiring diagram.

NOTES:

1. THIS IS A MULTIPLE USE ASSEMBLY. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 22 AWG STRANDED, TEFLON INSULATED. EXCEPT BUS WHICH IS NO 22 SOLID BARE WIRE.

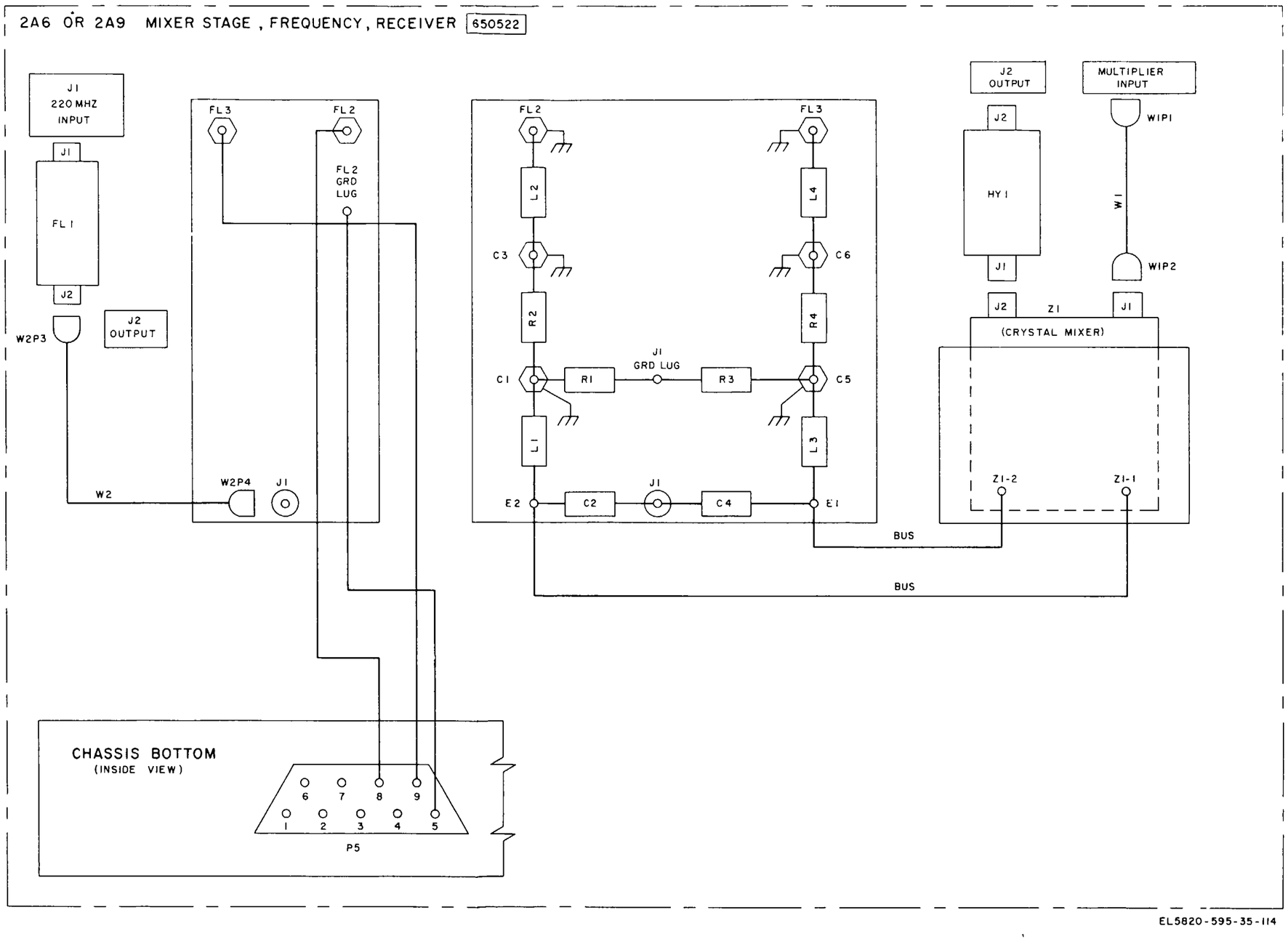


Figure 8-105. Frequency 2A6/2A9, assembly wiring diagram.

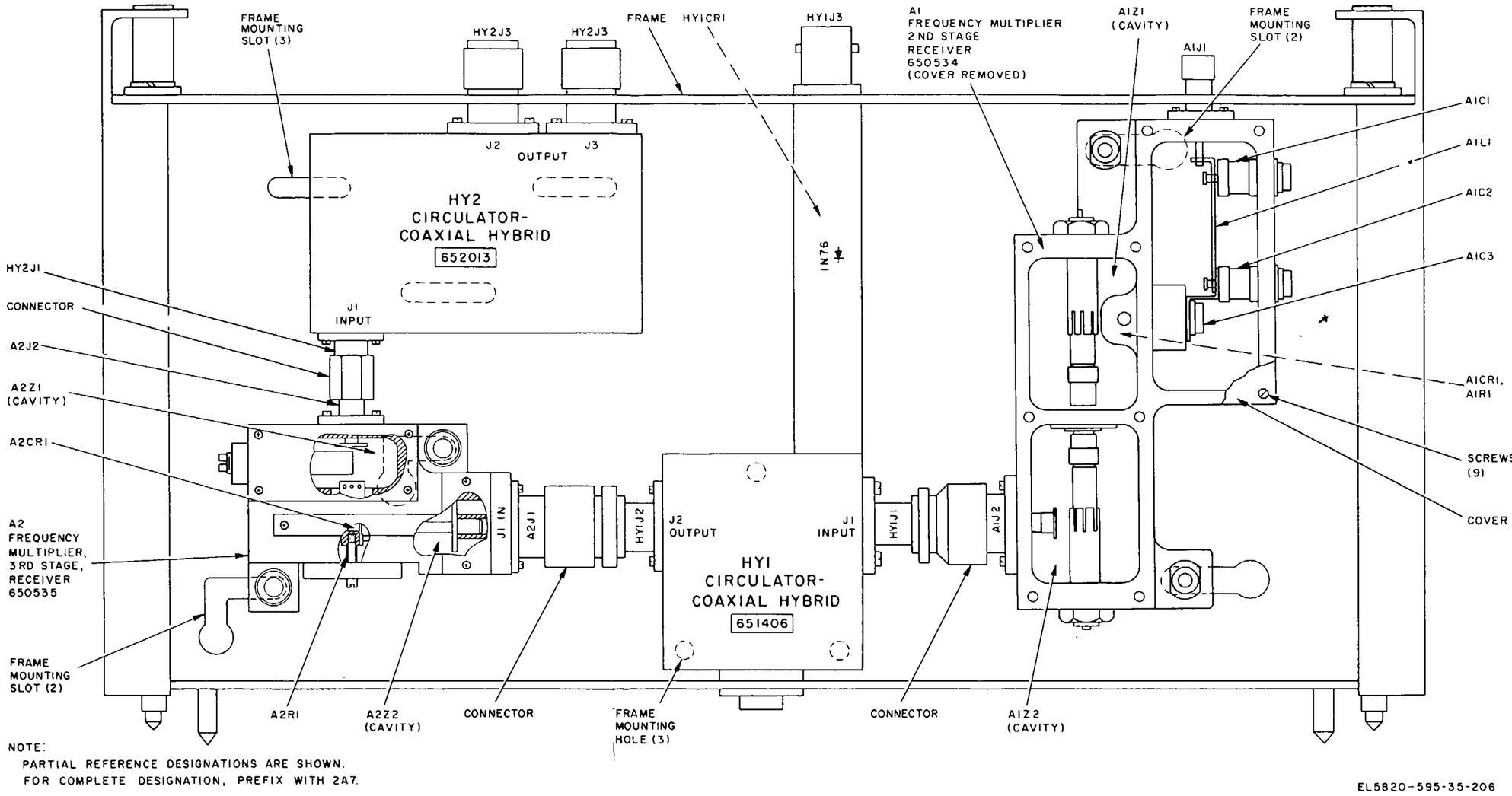


Figure 8-106. Frequency multiplier group 2A7, parts location diagram.

Notes:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION.

2. ALL WIRE IS NO 22 AWG STRANDED TEFLON INSULATED, UNLESS OTHER WISE SPECIFIED

3. WIRING TIEPOINT TERMINAL NUMBERS (WT) ARE ASSIGNED FOR IDENTIFICATION PURPOSES ONLY; THEY ARE NOT MARKED ON EQUIPMENT.

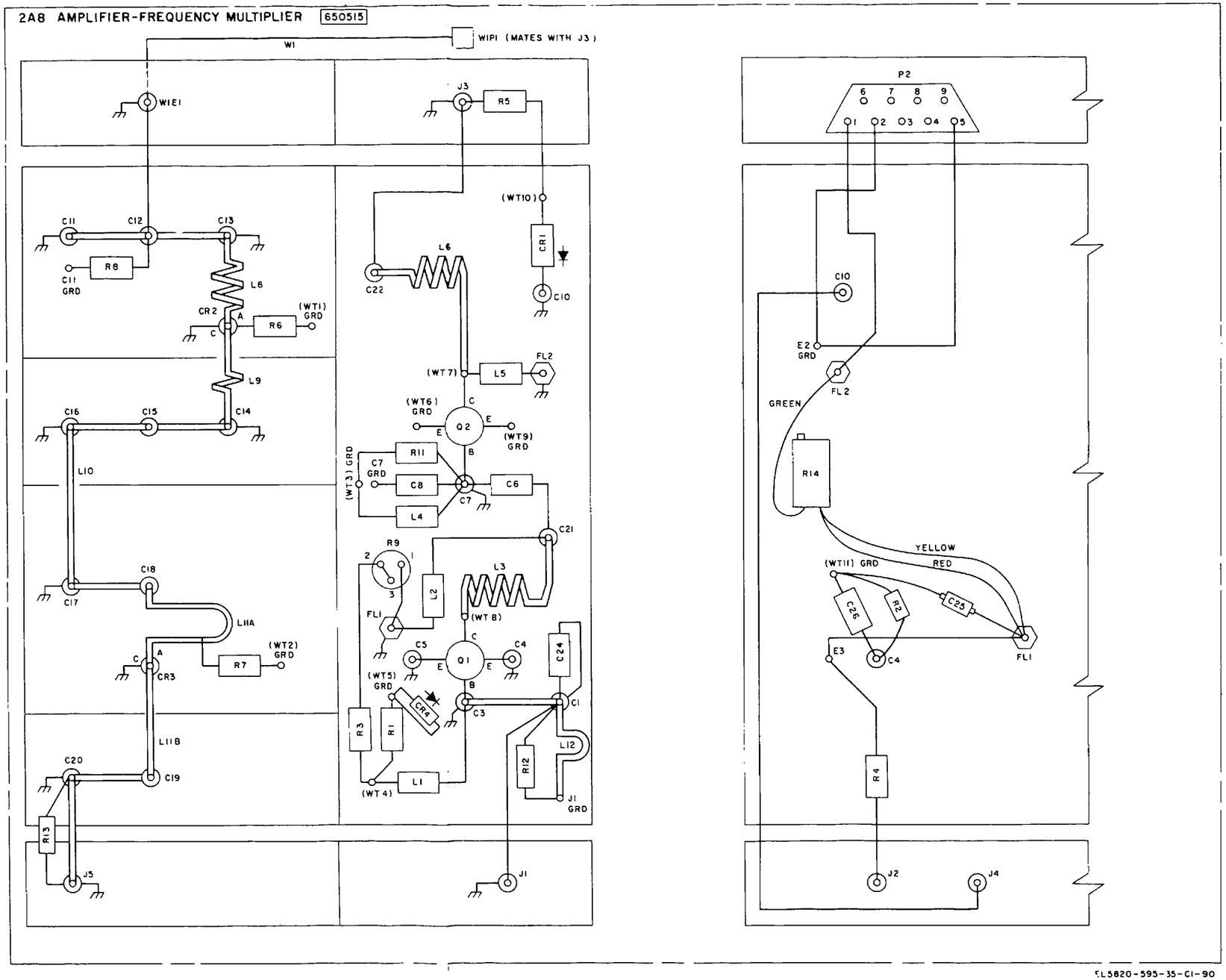
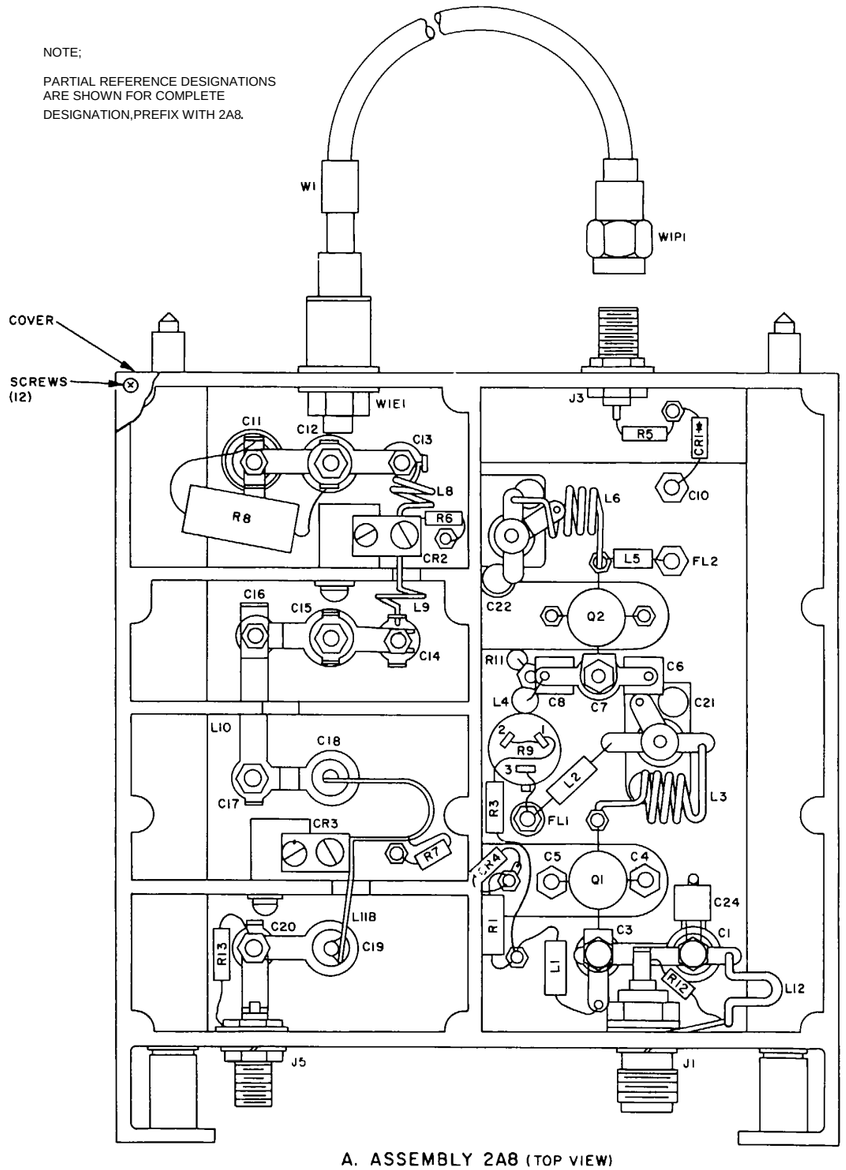


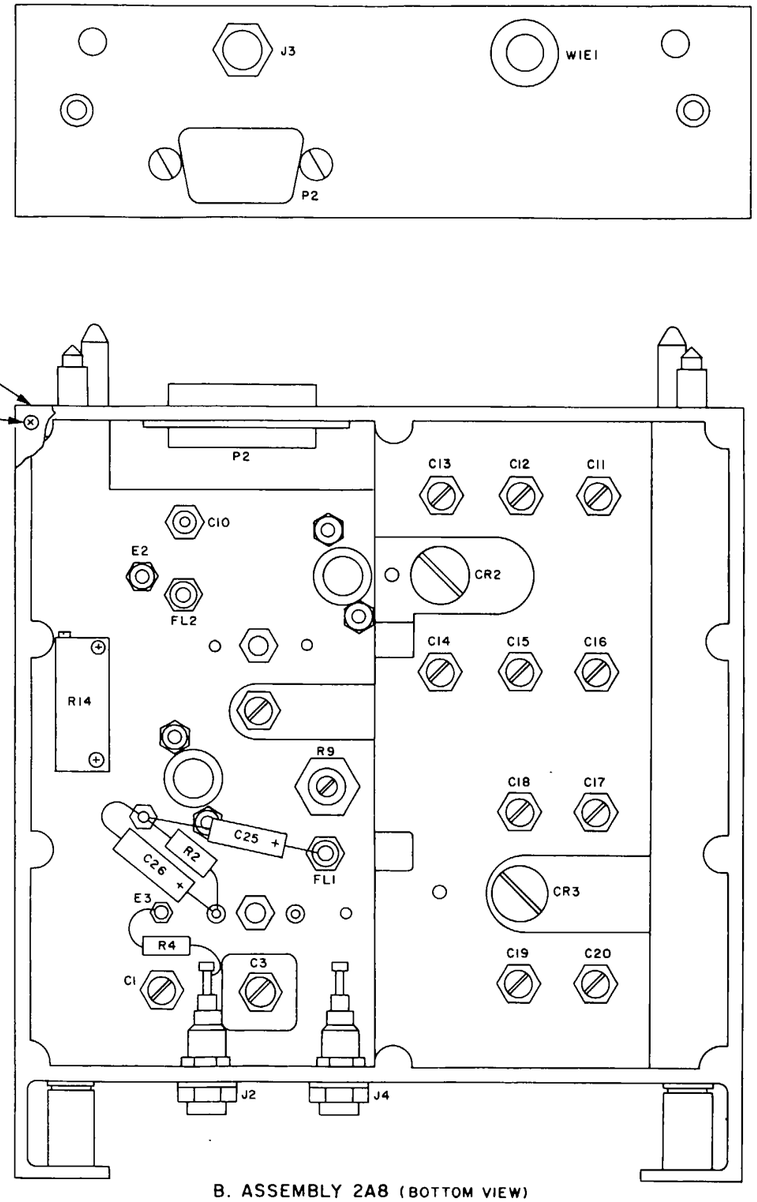
Figure 8-107. Amplifier multiplier 2A8, wiring diagrams. **Change 1**

NOTE;

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION,PREFIX WITH 2A8.



A. ASSEMBLY 2A8 (TOP VIEW)



B. ASSEMBLY 2A8 (BOTTOM VIEW)

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Figure 8-108. Amplifier multiplier 2A8, parts location diagrams. **Change 1**

NOTE:
THIS IS A MULTIPLE USE ASSEMBLY.
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 2A12
OR 2A15 AND SUBASSEMBLY DESIGNATION.

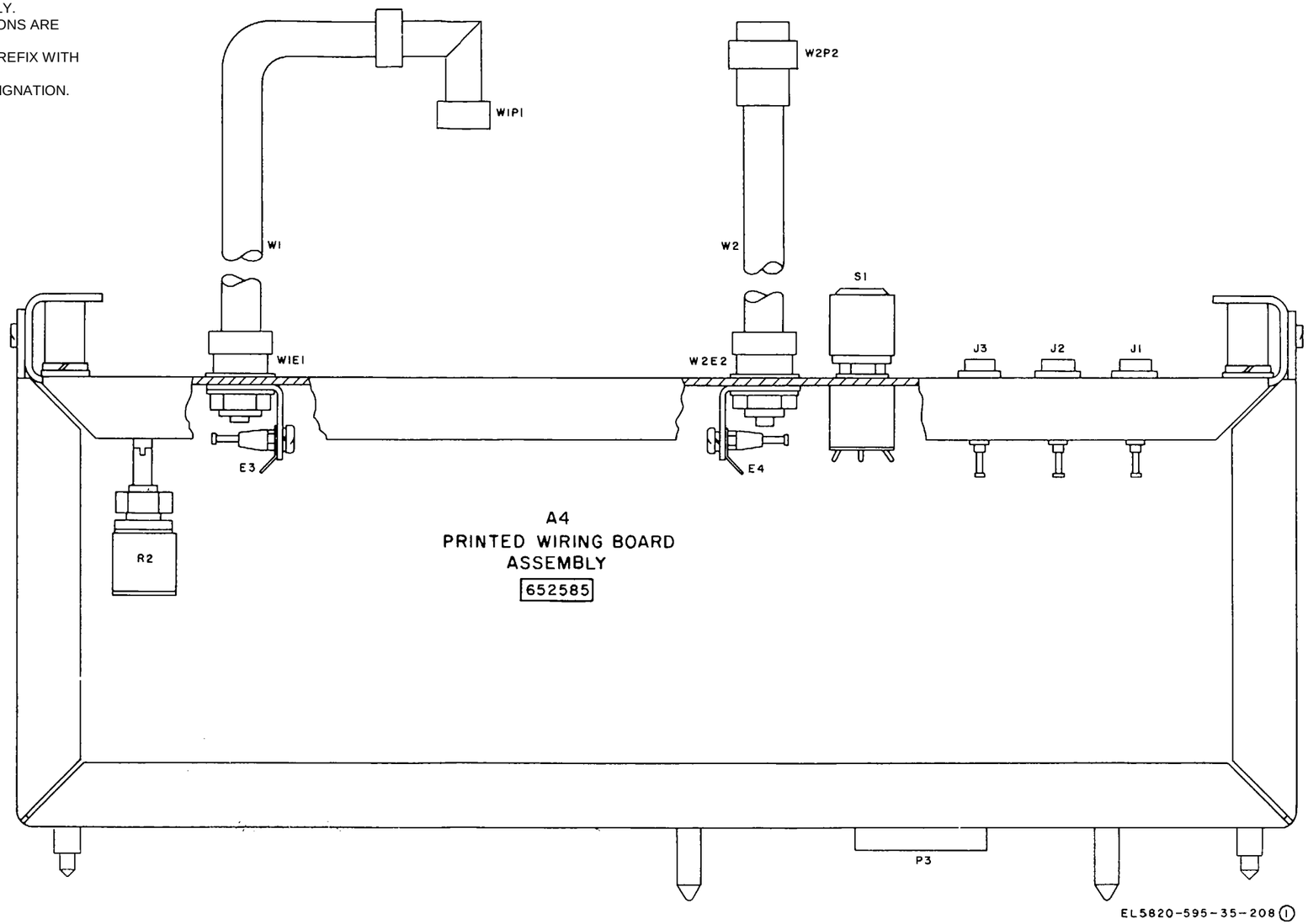
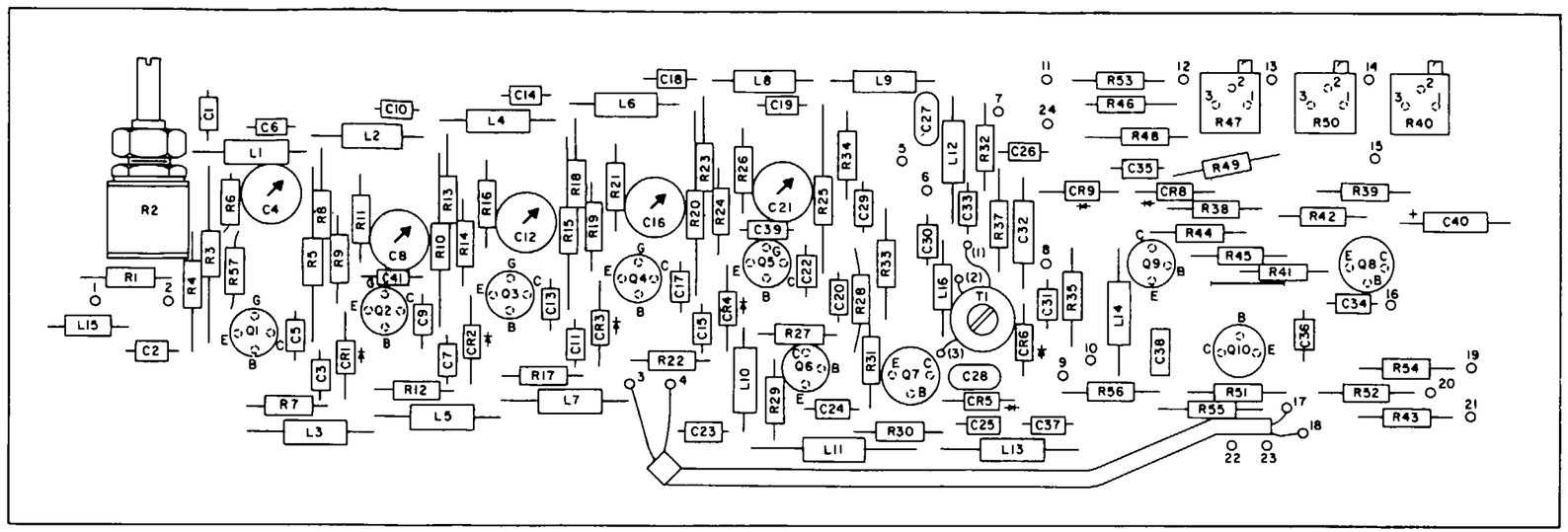
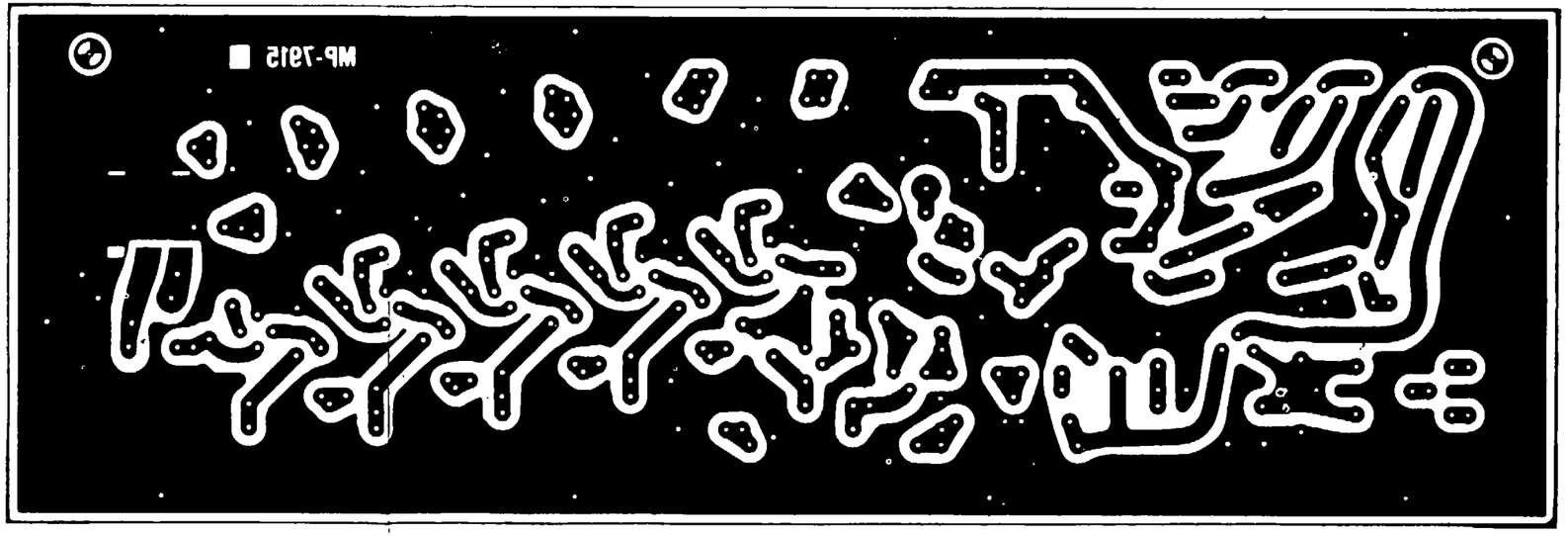


Figure 8-109.(1) If amplifier multiplier 2A12-2A15, parts location and printed wiring diagram (part 1 of 2).



A. PARTS AND WIRING ON FRONT OF BOARD A4 (652585)



B. WIRING ON BACK OF BOARD A4 (VIEWED THROUGH FRONT)

EL5820-595-35-CI-92 (2)

Figure 8-109. (2). If amplifier 2A12-2A15, parts location and printed wiring diagram (part 2 of 2). **Change 1**

NOTES:
1. PARTIAL REFERENCE DESIGNATION PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATIONS.
2. ALL WIRE IS NO.22 AWG STRANTED, TEFLON INSULATED.

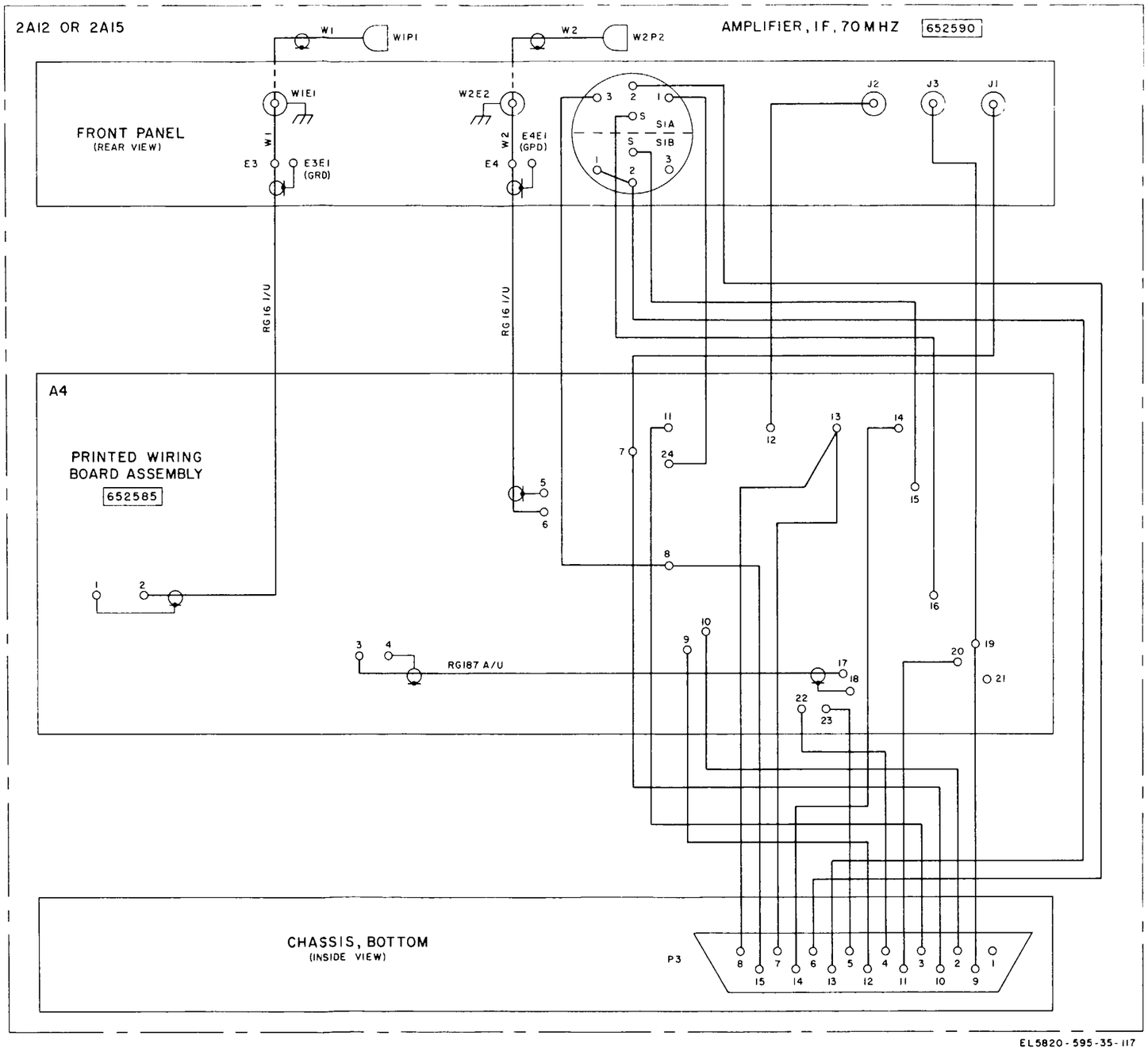
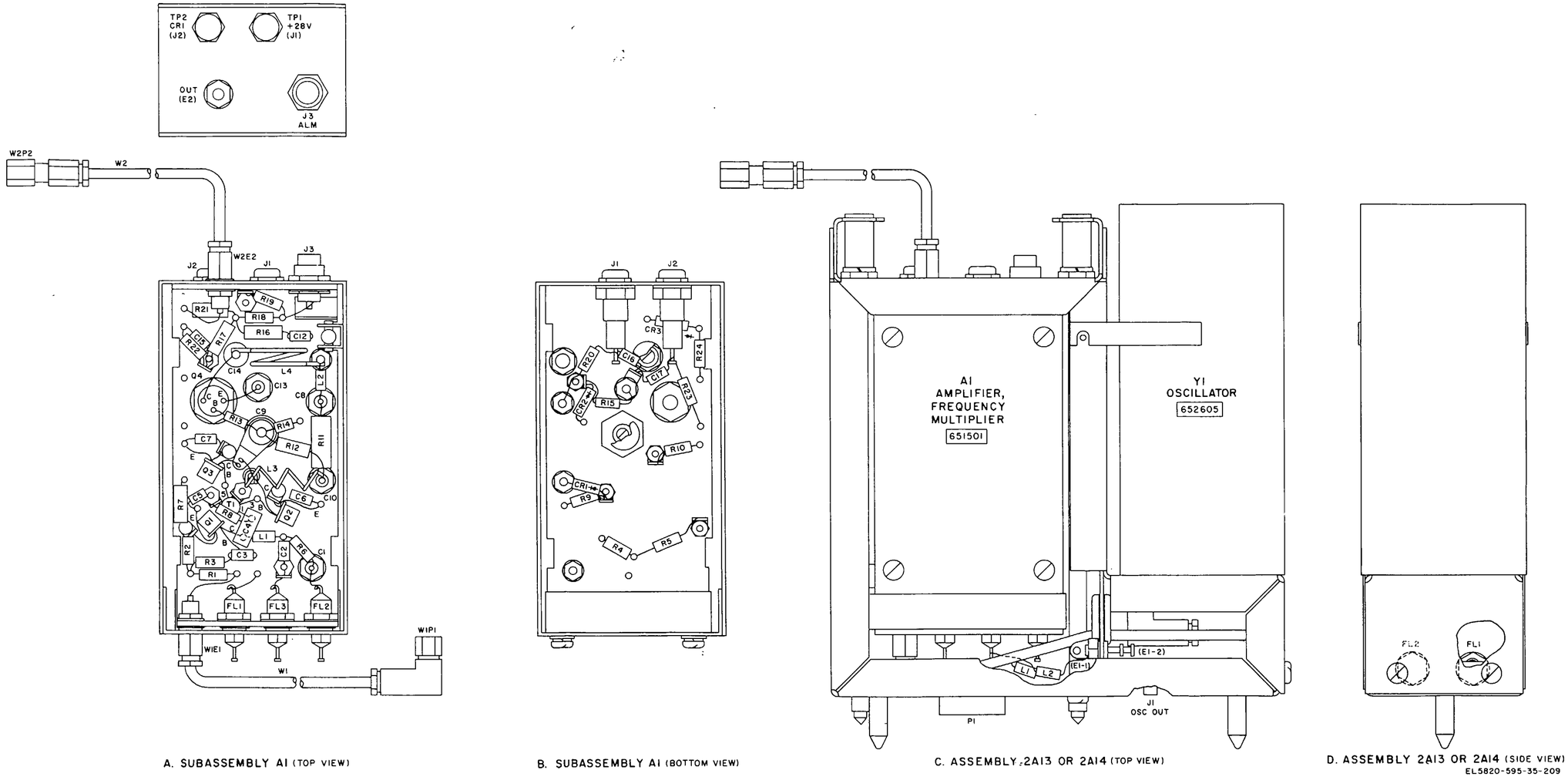


Figure 8-110. If amplifier 2A12/2A15, assembly wiring diagrams.



A. SUBASSEMBLY A1 (TOP VIEW)

B. SUBASSEMBLY A1 (BOTTOM VIEW)

C. ASSEMBLY 2A13 OR 2A14 (TOP VIEW)

D. ASSEMBLY 2A13 OR 2A14 (SIDE VIEW)

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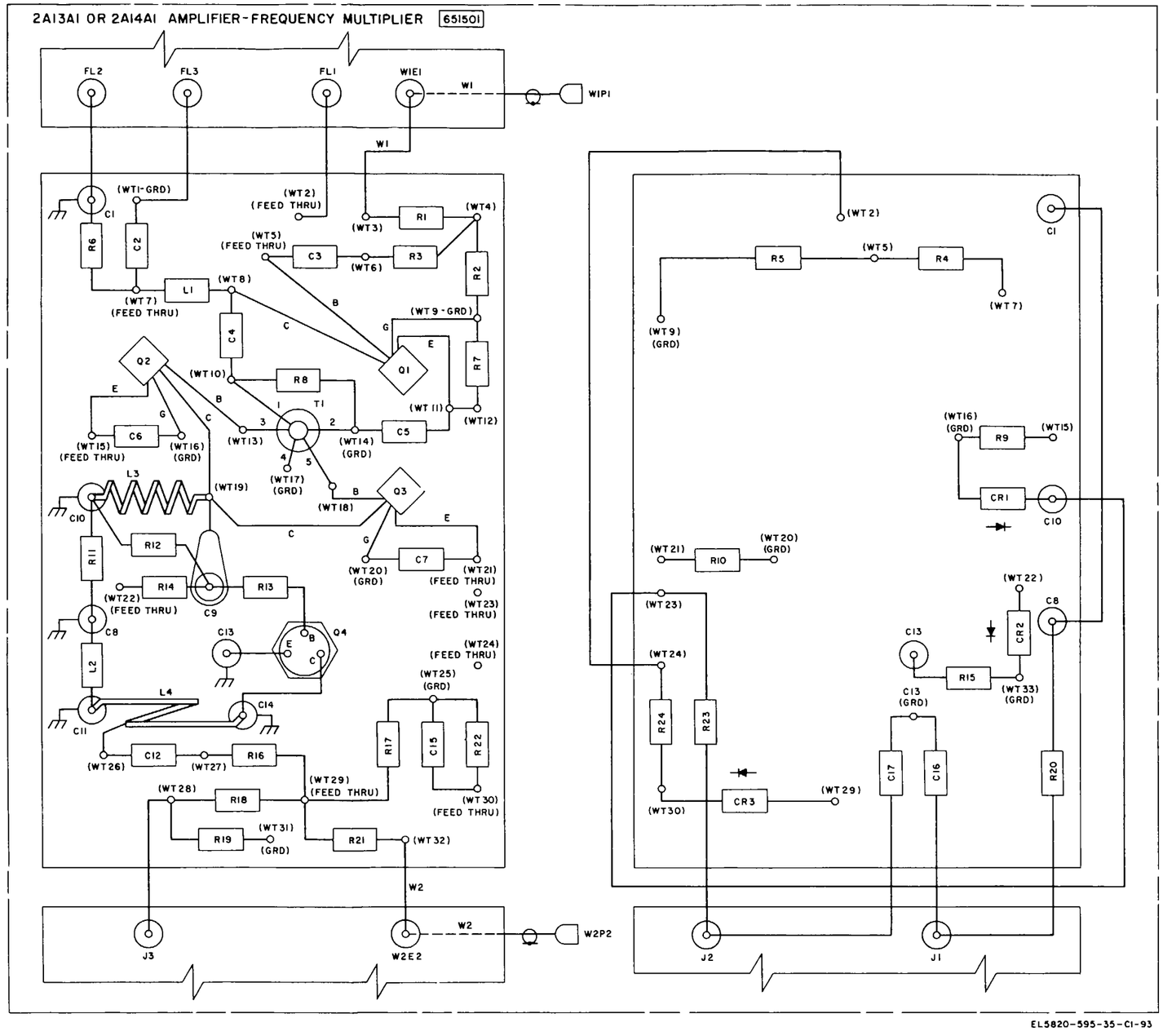
Figure 8-111. 220 MHz vco 2A13/2A14, parts location diagram.



Change 1

Figure 8-112. Frequency multiplier 2A13A1/A14A1,

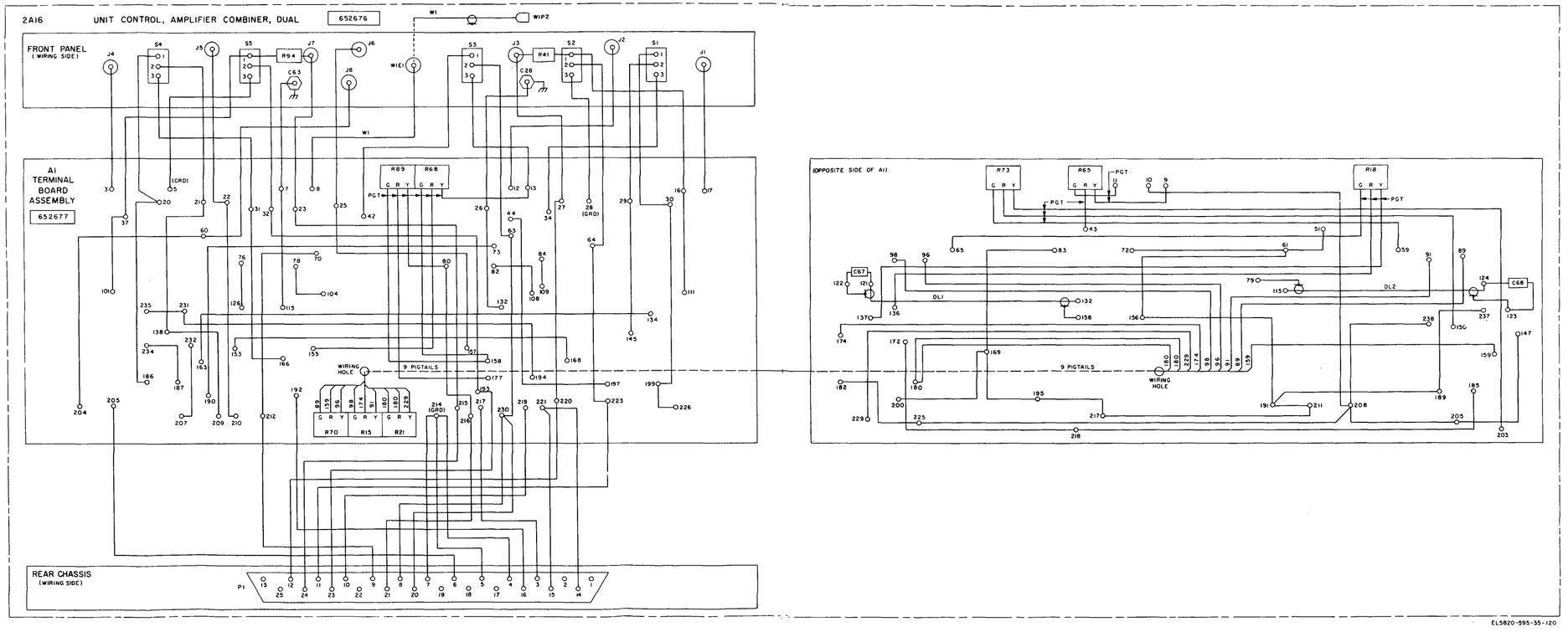
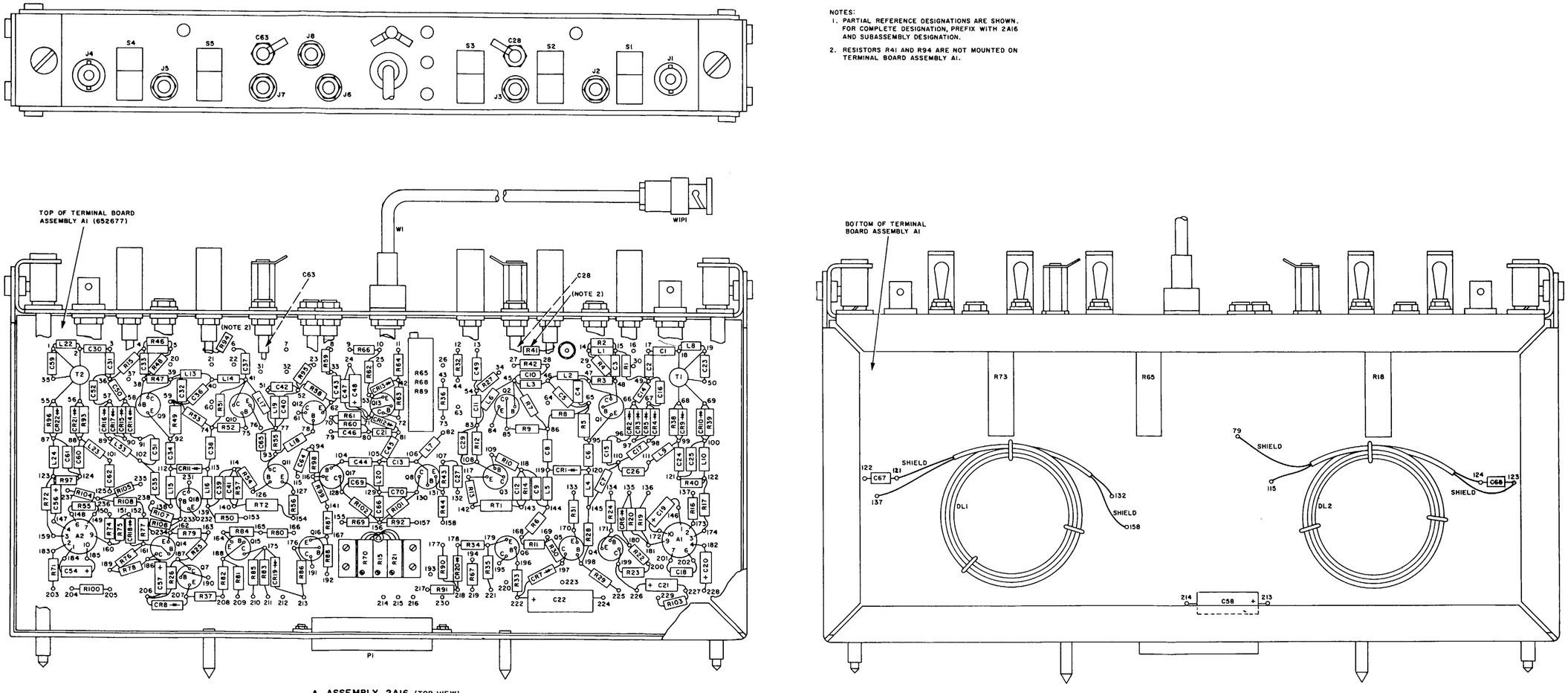


Figure 8-113. Combiner 2A16, assembly wiring diagram.



Change 1

Figure 8-114. Combiner 2A16, parts location diagram.

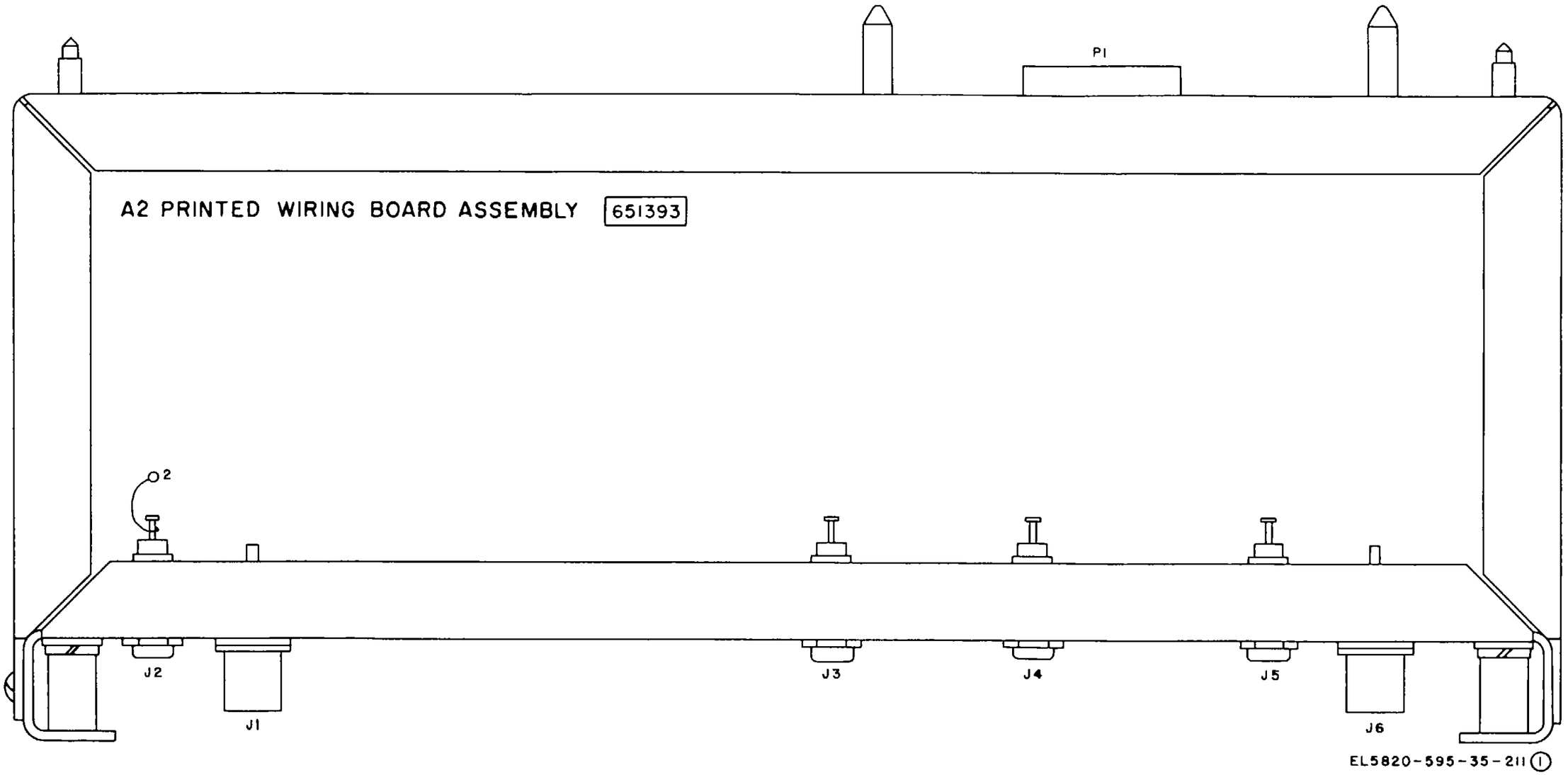


Figure 8-115 (1). Demodulator 2A17, parts location and printed wiring diagram (part 1 of 2)

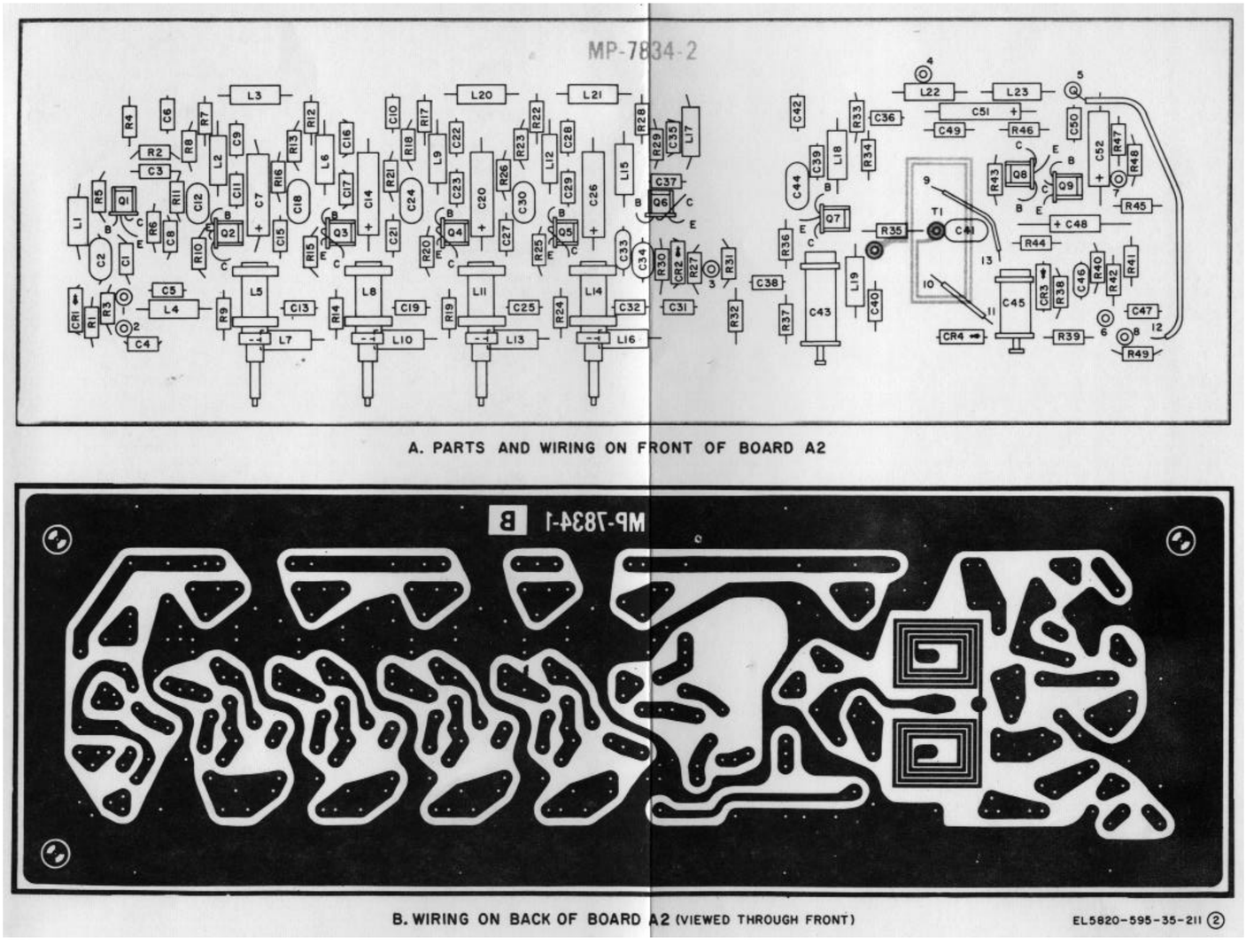


Figure 8-115 (2). Demodulator 2A17, parts location and printed wiring diagram (part 2 of 2)

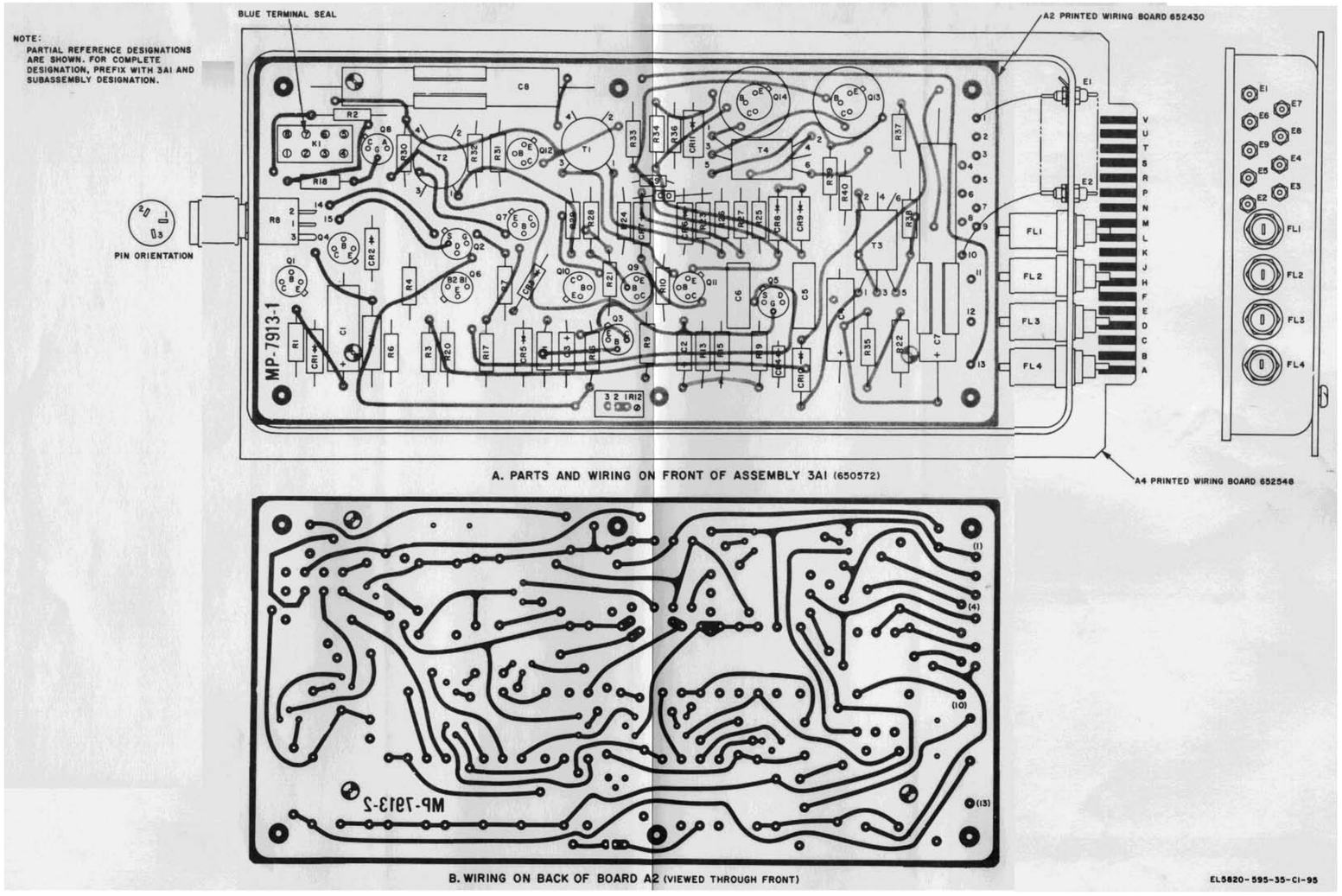


Figure 8-116. Inverter regulator control 3A1, parts location and printed wiring diagram.

Change 1

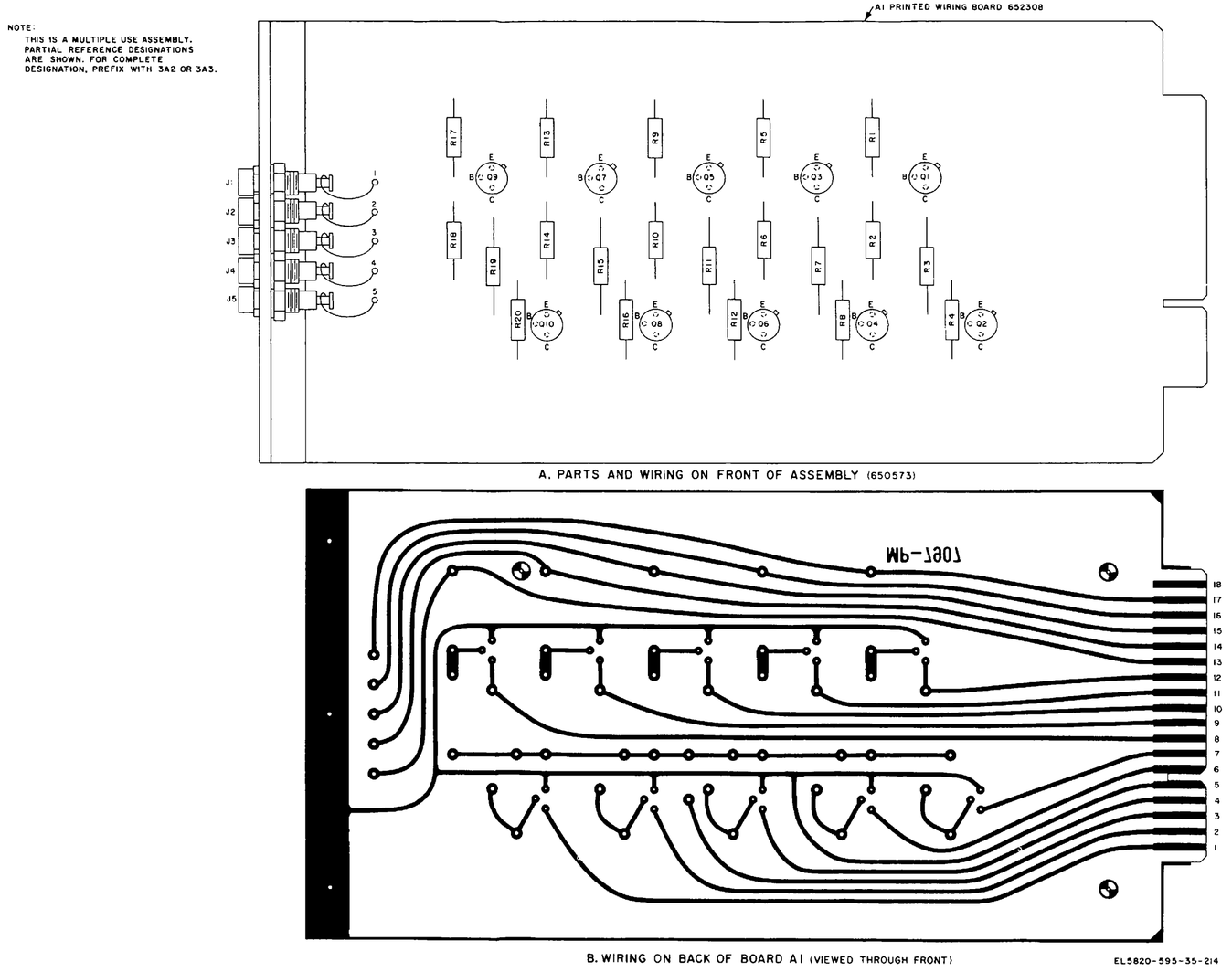


Figure 8-117. Indicator control 3A2/3A3, parts location and printed wiring diagram.

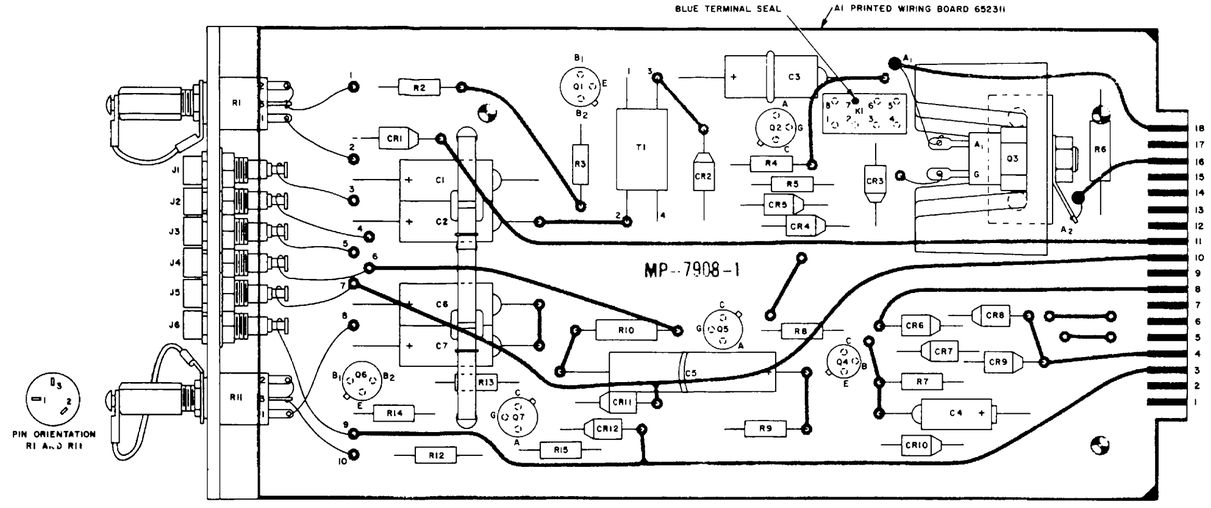


Figure 8-118. Low RF-mismatch alarm and control 3A4, parts location and printed wiring diagram.

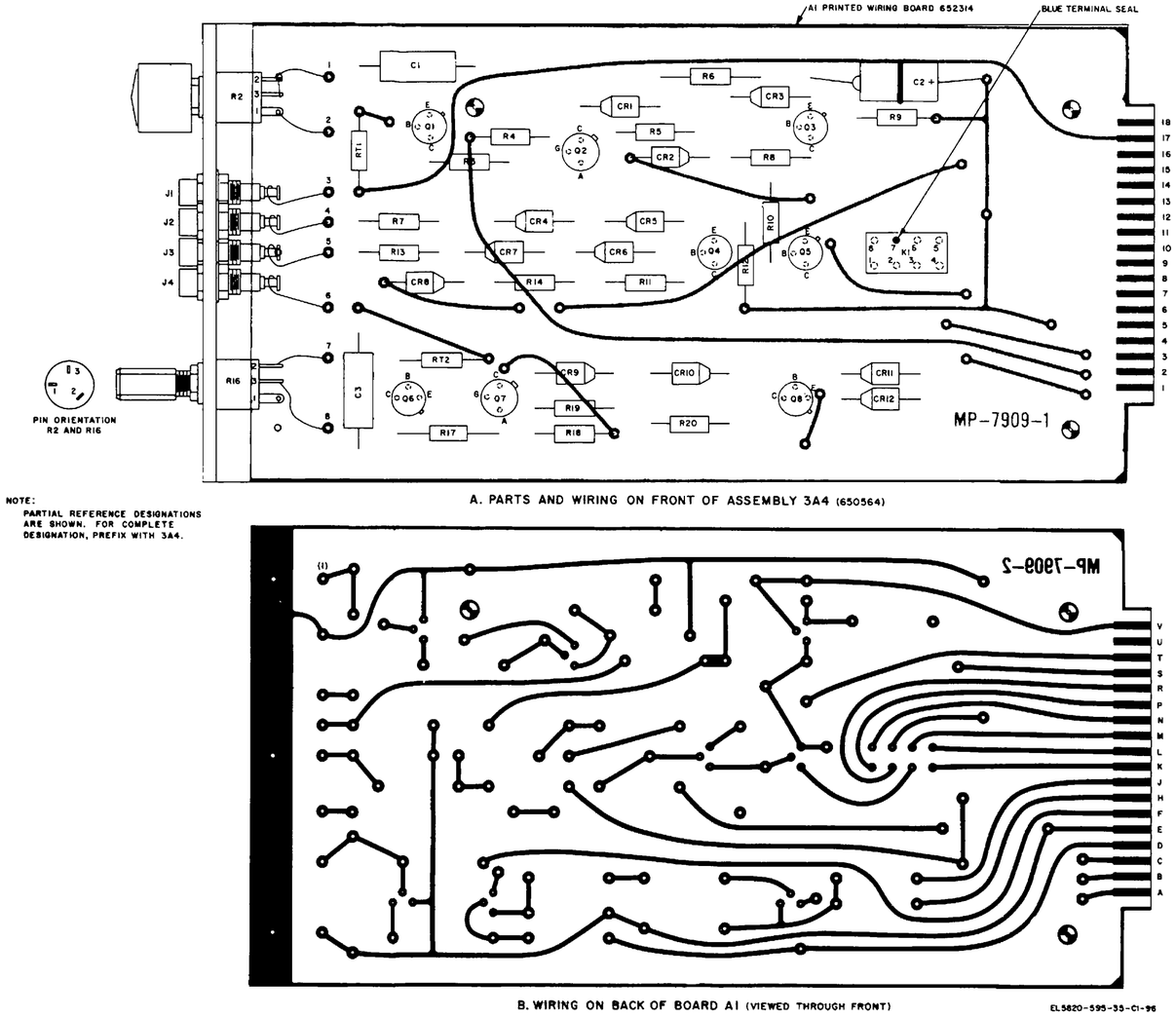


Figure 8-119. Time delay control 3A5, parts location and printed wiring diagram.

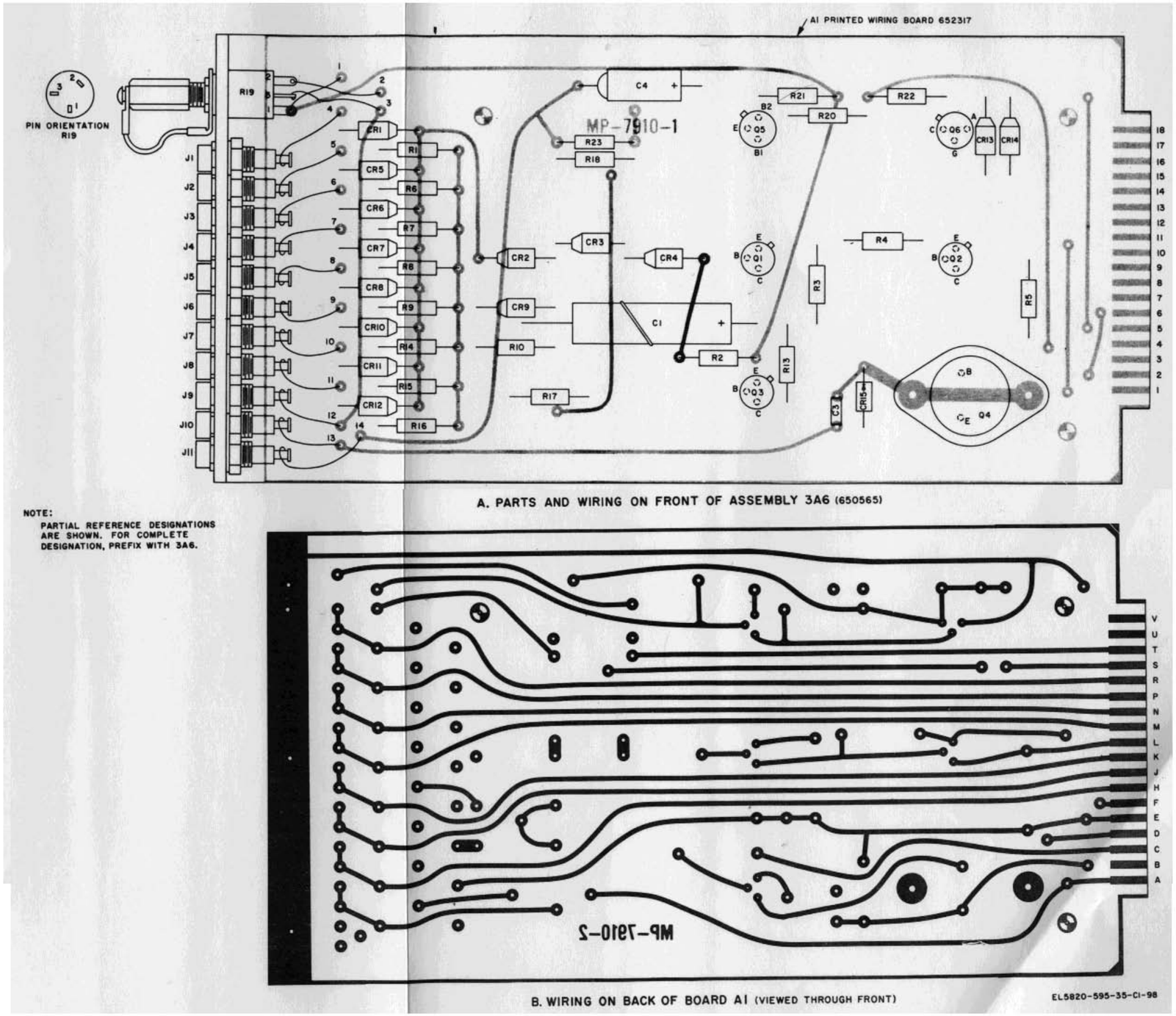


Figure 8-120. Beam gate dc-overload 3A6, parts location and printed wiring diagram.
Change 1

NOTES:

1. PARTIAL REFERENCE DESIGNATION ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO. 18 AWG STRANDED, TEFLON INSULATED, UNLESS OTHERWISE SPECIFIED.

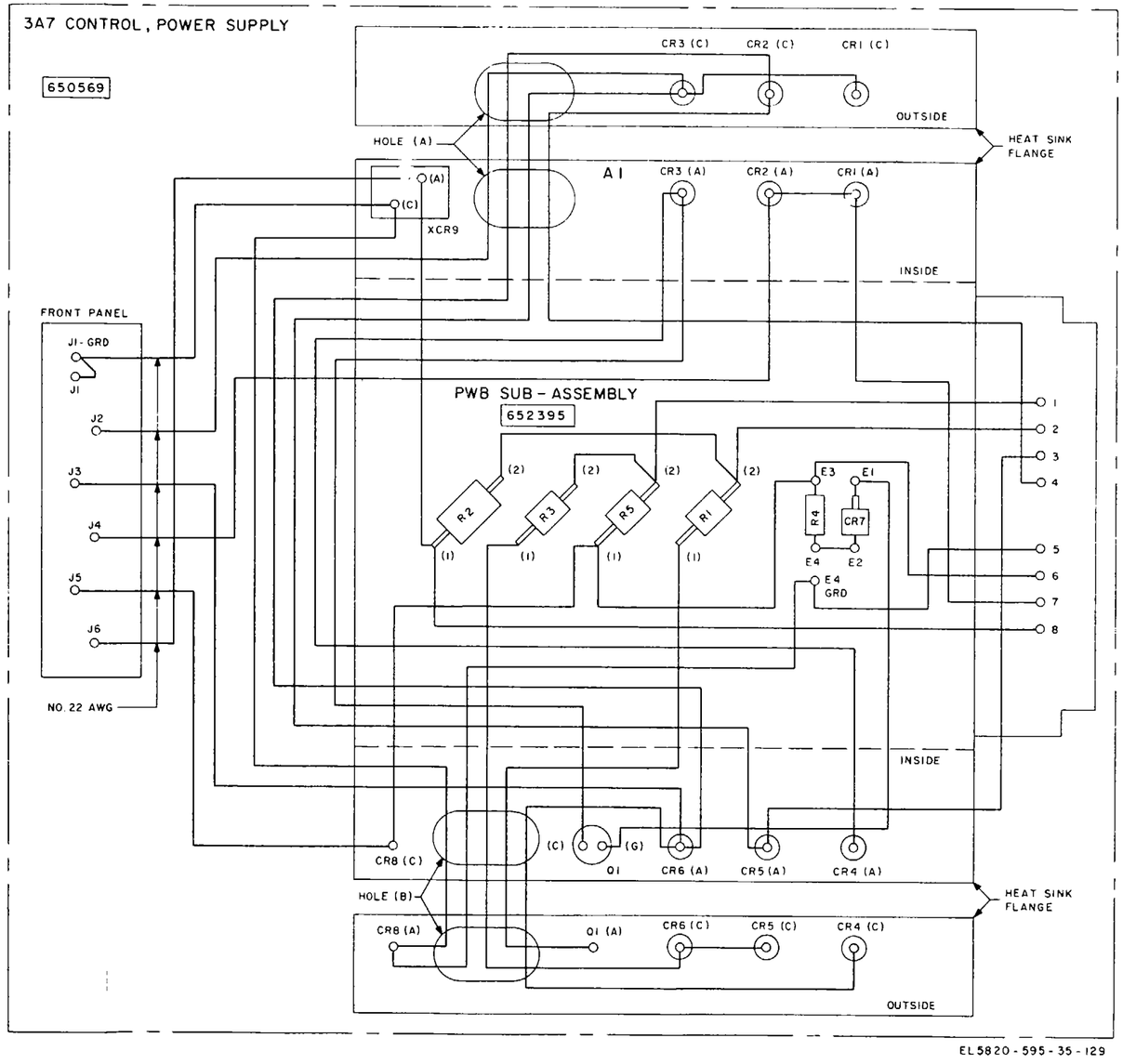
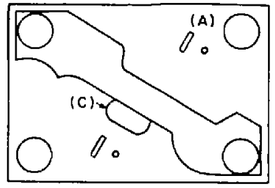
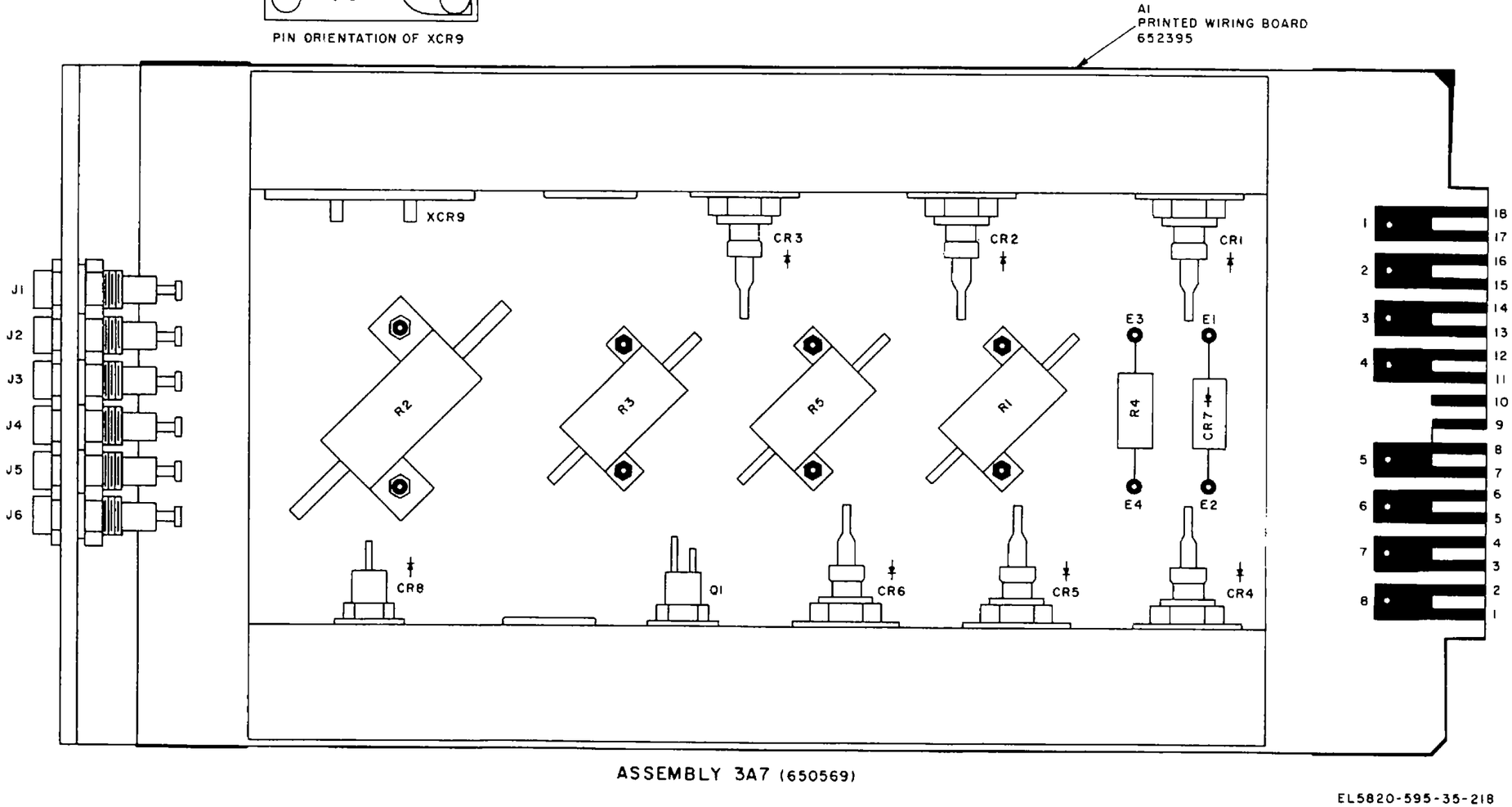


Figure 8-121. Power supply control 3A7, wiring diagram.

NOTE:
PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATION, PREFIX WITH 3A7.



PIN ORIENTATION OF XCR9



ASSEMBLY 3A7 (650569)

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Figure 8-122. Power supply control 3A7, parts location diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUB-ASSEMBLY DESIGNATION.
2. ALL WIRE IS NO.12 AWG STRANDED, TEFLON INSULATED, UNLESS OTHERWISE SPECIFIED.
3. THE FOLLOWING COMPONENTS ARE CONNECTED TOGETHER VIA HEATSINK AND BRACKETS:
   A) CR5-C, E15, CR6-A
   B) CR3-C, Q3-A, E1, Q1-A, CR1-C
   C) CR7-C, E16, CR8-A
   D) CR4-C, Q4-A
   E) Q2-A, CR2-C
4. WARNING SHIELDS OF SHIELDED PAIR WIRES ARE AT 200V POTENTIAL AND MUST BE INSULATED AT ALL JUNCTIONS. DO NOT GROUND SHIELDS.
5. LEADS OF L1 THRU L4 ARE NO.14 AWG TWIN PIGTAILS.

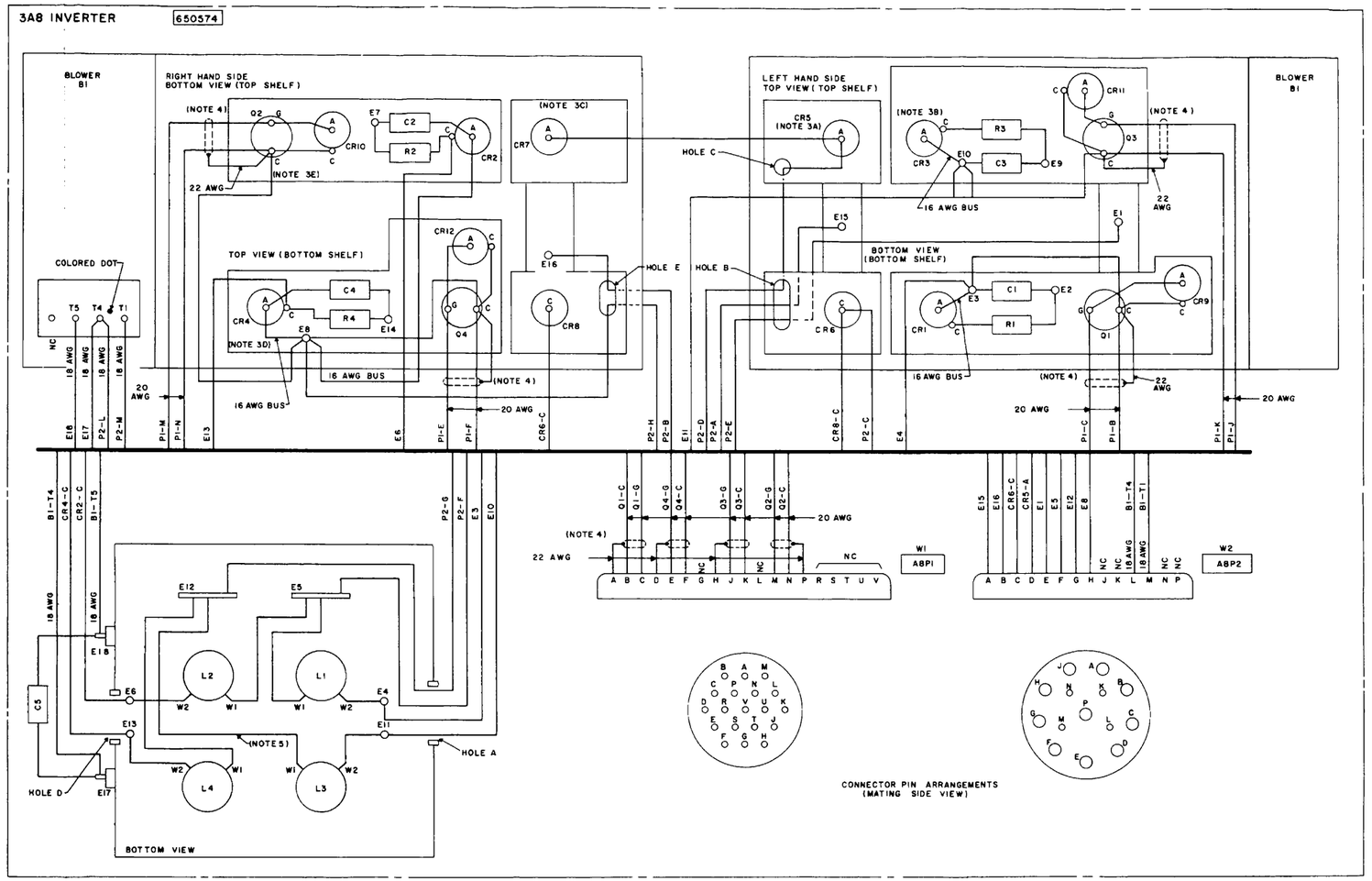

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Figure 8-123. Inverter 3A8, wiring diagram.
Change 1

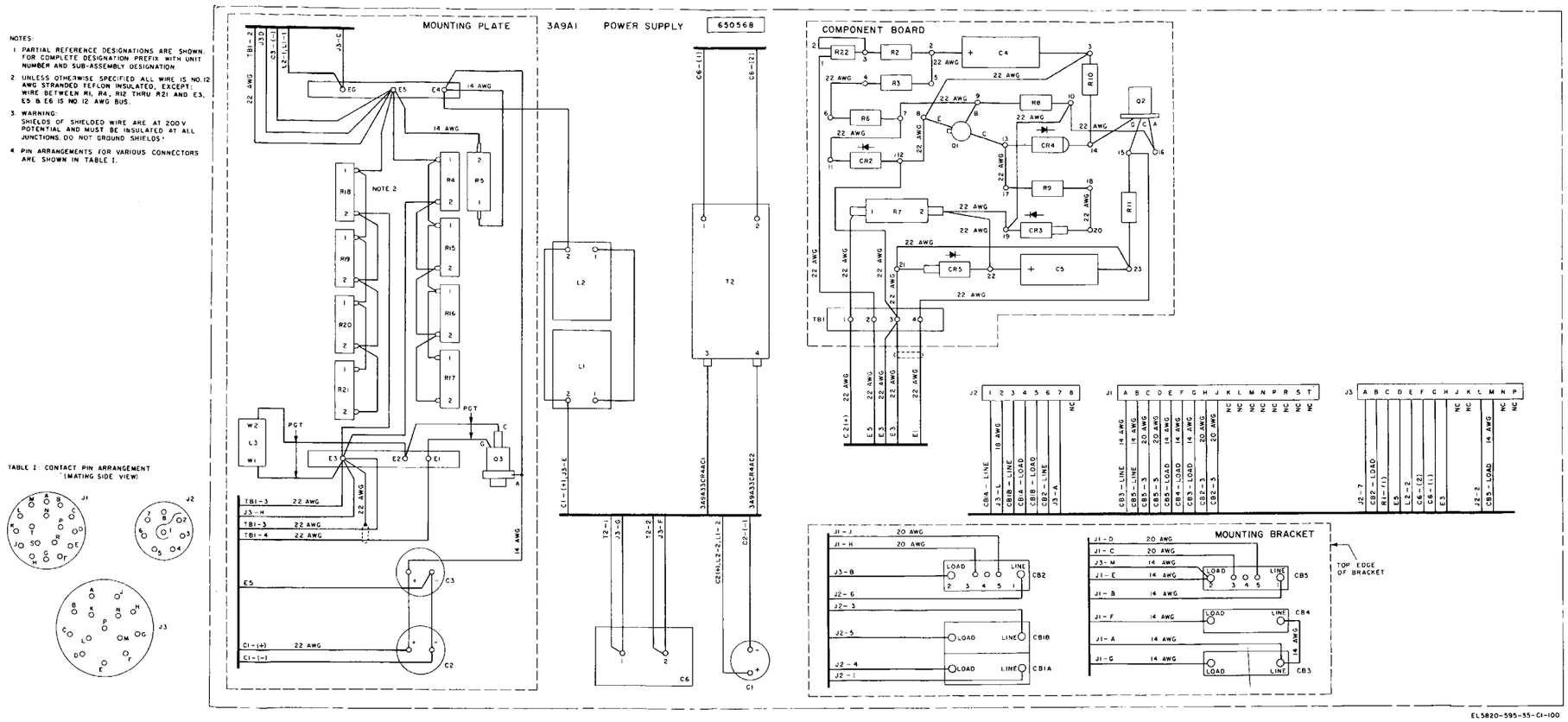

Figure 8-124. Hv power supply 3A9A1, wiring diagram.
Change 1

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The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

PIN: 015819-000